COMMUNICATION PRODUCTS
INTEGRATED CIRCUITS

silicon systems®

1990 Data Book

Silicon Systems, Inc.

Silicon Systems, Inc. specializes in the marketing, design, and manufacturing of mixed-signal (analog-digital), application-specific integrated circuits (ASICs). It offers a sophisticated line of custom and standard ICs aimed primarily at the microperipheral, communications and automotive marketplaces.

The Company was founded in 1972 and is headquartered in Tustin, California, 30 miles south of Los Angeles. At first it offered only design services, but in the mid-70s began to subcontract the manufacturing of finished products. In 1981 the Company launched its own wafer manufacturing capability, which was completed and put into production in 1982. A fully integrated assembly and test operation in Singapore was implemented in 1985. In 1988 Silicon Systems acquired its second wafer fabrication facility in Santa Cruz, California, and opened its fourth design center in San Jose, California.

Silicon Systems is committed to leadership in the development of high-performance, mixed-signal ICs (MSICs) for custom, semi-custom or standard applications, in addition to providing pure analog or digital ICs. Of approximately 60 design starts in 1989, roughly half were custom, and the remaining were standard. Design centers are located in Tustin, San Jose and Grass Valley, California, as well as in Singapore. Reliability and quality are built into our products beginning at this design stage, and through an accelerated program of statistical process control we hope to maintain the highest levels of quality for our finished products in the industry.

Silicon Systems possesses the capabilities to produce, market and deliver its ICs to a growing worldwide customer base. In support of these capabilities, and listed in the back of this publication, we offer a worldwide network of sales representatives and distributors ready to serve you.

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☐ I've got some questions. Please have a sales representative contact me:
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Discontinued Parts List

The following parts are no longer supplied or supported by Silicon Systems. Please note alternate sources.

Part #	Description	Alternate Source
SSI 22100	4 x 4 Crosspoint Switch	RCA
SSI 22101/102	4 x 4 x 2 Crosspoint Switch	RCA
SSI 22106	8 x 8 x 1 Crosspoint Switch	RCA
SSI 291	Modem Building Block	None, use SSi K-series
SSI 213	Modem Filter	None, use SSI 73M3522
SSI 169/SC01	Phoneme Speech Synthesizer	Artic Technologies*
SSI 263A	Phoneme Speech Synthesizer	Artic Technologies*
SSI 78P8050	T1 Transmitter	None
SSI 78P8060	T1 Receiver	None

*Artic Technologies
55 Park St., Suite 2
Troy, MI 48083-2753
(313) 588-7370

Silicon Systems' Communication Products Capabilities

Silicon Systems offers a broad line of standard integrated circuits aimed at providing cost effective system solutions for many mixed signal communications equipment problems. For those manufacturers that have special mixed signal requirements we offer custom or customized integrated circuit capability. The heart of Silicon Systems' efforts in the communications market is the continuous expansion of circuit technology. Our pioneering work with CMOS switched capacitor filters enabled us to develop the first integrated DTMF receiver which led to our industry standard DTMF family. This CMOS switched capacitor technology has been used in many non-DTMF filtering functions of other Silicon Systems integrated circuits, most notably, our family of modem products.

The pioneering continues as our mixed signal technology expansion has led us to develop DSP techniques to supplement traditional analog signal processing techniques. The SSI 73K224 V.22bis modem is one example of how the use of this DSP technology has been used with analog signalling processing to optimize die size so that a single IC modem solution was possible. Our highly integrated system solutions demonstrate not only technological leadership in our own semiconductor field but also the ability to anticipate the growing needs of the fast-paced communications marketplace.

Here are a few examples of custom and standard ICs that demonstrate our broad communications IC capabilities.

CMOS

Integrated Circuit Function	Application
DTMF Receiver	Decodes Touch-Tone® Telephone Signals
One-chip Modems	Data Transmission
Error Corrector	Military Radio
Remote Transmitter	Telephone Ans. Machine
Modem AFE	V.32 Data Transmission
Analog Crosspoint Switch	PBX's
Video Processor	Infrared Video System
16 Channel Switching Matrix	Bank Comm. Systems
Digital Loop Detector	Traffic Signal Control
Programmable Digital Receiver	Home Appliance Remote Control
DSP Based Filter	Programmable Filters
Satellite Descrambler	CATV Receiver
Modem AFE	19.2 Kbit/s Data Transmission
DSP-based Telemetry	Watt Hour Meter

BIPOLAR

Integrated Circuit Function	Application
Audio System Receiver	Telephone Answering Machine
VHF/UHF Gain Mixer	Radio Receiver
Digital Receiver	Remote Control
PCM Encoder/Decoder	Telecom System
Digital Correlator/Integrator	Radio Telescope
DS-1 Line Interface	T1 Channel Banks Multiplexers
LAN Transceiver	IEEE 802.3 Ethernet LAN
Modem AFE	1200 bit/s Data Transmission

PROCESSES

Three **bipolar** processes are used to optimize cost/performance. Key features include polysilicon emitter structures, base and collector plugs, double metal, fr from 3 to 7.5 GHz and metal-nitride-poly capacitors.

There are also three **CMOS** processes in production for cost/performance optimization. Key features include poly-poly capacitors, poly resistors, operating voltages from 5 to 12 volt, double poly and double metal.

PRODUCT QUALITY

At Silicon Systems, the quality program encompasses all company activities and is based on management's firm belief that quality must be "built into" all Silicon Systems products by ensuring that all employees are trained in the quality philosophy of the company. Process control provides continuous visibility of the performance of manufacturing processes. The PPM Program is aimed at achieving and maintaining "zero defects." Computer Aided Manufacturing Control is used for statistical process control and manufacturing monitoring.

CUSTOMER SERVICE

Silicon Systems provides individualized service for every customer. Our Customer Service Department is dedicated to responsive service and is staffed with personnel trained to consider our customers' needs as their most urgent requirement. Product quality and service are both viewed as cornerstones for Silicon Systems' continued growth.

Section 1

K-SERIES MODEM FAMILY

MODEM INTEGRATED CIRCUITS SELECTOR GUIDE

APPLICATIONS / MARKETS SERVED	PRODUCTS / SSI DEVICE NUMBER	OPERATING MODES: 103 0-300 Bit/s	212A 1200 Bit/s	V.21 0-300 Bit/s	V.22 600/ 1200 Bit/s	V.22 bis 1200/ 2400 Bit/s	V.23 0-1200 Bit/s	202 S/T 0-1200 Bit/s FDX	PRODUCT FEATURES
UNIVERSAL APPLICATIONS Stand-Alone or Integral Modem Designs	73K212	■	■						Fully integrated single-chip modems with easy-to-use bus interface and cost-effective features needed for intelligent modem designs. All mod/demod, DTMF dialing, and call-progress functions included on-chip.
	73K221	■	■	■	■				
	73K222	■	■	■	■	■			
	73K224	■	■	■	■	■	■		
LOW POWER APPLICATIONS • Lap Tops • Portable Terminals • Line Powered Modems • Battery-Powered Units	73K212L	■	■						High performance, single-chip modems providing low-power operation from a single +5 volt supply.
	73K221L	■	■	■	■				
	73K222L	■	■	■	■	■			
	73K224L	■	■	■	■	■	■		
DEDICATED INTEGRAL APPLICATIONS • Bus-Oriented Systems • Credit Verif. • Automatic Teller Machines • Pay Telephones • Diagnostic Equipment	73K212U	■	■						Enhanced single-chip modems with a fully integrated, high speed 16C450 UART function, and added circuitry to simplify integral designs.
	73K221U	■	■	■	■				
	73K222U	■	■	■	■	■			
VIDEOTEX AND LEASED-LINE APPLICATIONS • European multi-standard videotex modems • North American POS, SCADA, and R.F. modem uses	73K321L	■	■	■	■	■	■		Single-chip modems add V.23 or Bell 202 4W capability to standard operating modes single +5V, low power operation
	73K322L	■	■	■	■	■	■		
	73K302L	■	■					■	
	73K324L	■	■	■	■	■	■		

INTRODUCTION

Silicon Systems K-Series Family of One-Chip Modems

Silicon Systems is a leader in the design and manufacturing of CMOS VLSI modems, and has been providing innovative solutions to the communication industry for more than ten years. Currently, Silicon Systems offers the most extensive line of one-chip modem ICs available, with high-performance, cost-effective designs suitable for a wide range of applications. Silicon Systems' fully compatible modem IC family has redefined the modem IC as a universal component which can be easily integrated into any system. Designs can be upgraded to meet different standards and speeds by simply substituting one K-Series IC for another. Using a K-Series family modem IC in your application eliminates product obsolesence, and minimizes development costs.

The Silicon Systems modem IC family consists of four basic products:

1. The SSI 73K212, which provides 0-300 bit/s and 1200 bit/s operation compatible with the Bell 212A and 103 standard.

2. The SSI 73K221, allowing CCITT V.22 and V.21 operating modes at 0-300, 600, and 1200 bit/s.

3. The SSI 73K222, a multi-mode device which combines both Bell 212A/103 and V.22/V.21 capability in one chip.

4. The SSI 73K224, a major technological breakthrough which provides 2400 bit/s V.22bis operation in addition to V.22/V.21 and Bell 212A/103 modes in a single IC.

New additions to Silicon Systems' modem IC family extend the available operating modes and provide features which greatly simplify integral modem design. For European applications, the SSI 73K322 provides CCITT V.22/V.21 plus V.23 Videotex modes. The SSI 73K324 offers V.22bis, V.22/V.21 and V.23 operating modes on one chip. Products in the "U" version group add an industry standard 16C450 UART and other features to the basic K-Series operating modes. These products dramatically reduce external circuitry required for dedicated integral modem designs.

Silicon Systems' one-chip modem IC products represent technical achievements unmatched in the industry. An advanced Digital Signal Processor resides on the same chip with sophisticated analog circuitry in the SSI 73K224 and SSI 73K324 products. "U" versions of the K-Series devices integrate an industry standard UART with full modem capability on a single chip. In addition, an innovative bus structure makes a separate controller unnecessary in dedicated integral designs. All K-Series devices are available in low-power versions. This feature allows optimal performance with single +5V supply operation and is unique to Silicon Systems' products.

Silicon Systems' single-chip modem IC family is designed to be the most effective solution for a wide variety of modem applications. The products provide for a full range of communications standards and speeds up to 2400
bit/s. Moreover, features can be extended to include additional modes and higher operating speeds without impacting existing designs. Take advantage of these capabilities. Design for tomorrow's needs today by using Silicon Systems' K–Series modem IC family.

NOTES:

SSI 73K212/K212L
Bell 212A/103
Single-Chip Modem

July, 1989

1

DESCRIPTION

The SSI 73K212 is a highly integrated single-chip modem IC which provides the functions needed to construct a typical Bell 212A full–duplex modem. Using an advanced CMOS process that integrates analog, digital and switched–capacitor filter functions on a single substrate, the SSI 73K212 offers excellent performance and a high level of functional integration in a single 28- or 22-pin DIP configuration. The SSI 73K212L low power version of the SSI 73K212 provides identical performance and features, but operates from a single +5 volt supply with substantially lower power consumption.

The SSI 73K212 includes the PSK and FSK modulator/demodulator functions, call progress and handshake tone monitor test modes and a DTMF dialer. This device supports all Bell 212A modes of operation allowing both synchronous and asychronous communications.

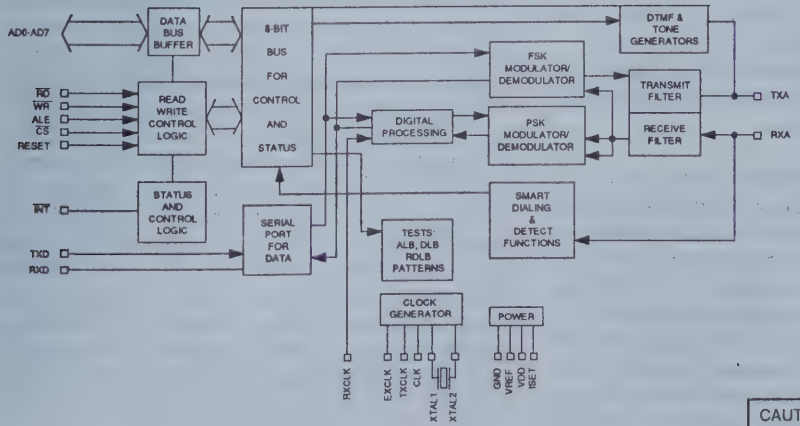
Test features such as analog loop, digital loop, and internal remote digital loopback are provided. Internal pattern generators are also included for self-testing. The SSI 73K212 is designed to appear to the systems designer as a microprocessor peripheral, and will easily interface with popular one-chip microprocessors

(Continued)

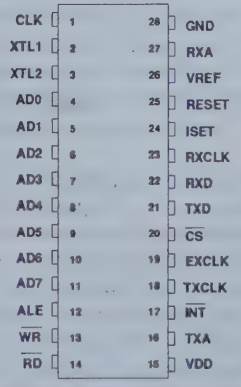
FEATURES

- One-chip Bell 212A and 103 standard compatible modem
- Full-duplex operation at 0-300 bit/s (FSK) or 1200 bit/s (DPSK)
- Pin and software compatible with other SSI K-Series 1-chip modems
- Interfaces directly with standard microprocessors (8048, 80C51 typical)
- Serial (22-pin DIP) or parallel (28-pin DIP) microprocessor bus for control
- Serial port for data transfer
- Both synchronous and asynchronous modes of operation
- Call progress, carrier, precise answer tone and long loop detectors
- DTMF generators
- Test modes available: ALB, DL, RDL, Mark, Space, Alternating bit patterns
- Precise automatic gain control allows 45 dB dynamic range
- Space efficient 22- or 28-pin DIP packages
- CMOS technology for low power consumption using 30 mW @ 5V or 180 mW @ 12V
- Single +5 volt (73K212L) or +12 volt (73K212) versions

BLOCK DIAGRAM



PIN DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

DESCRIPTION (Continued)

(80C51 typical) for control of modem functions through its 8-bit multiplexed address/data bus or via an optional serial command bus. An ALE control line simplifies address demultiplexing. Data communications occurs through a separate serial port only.

OPERATION

The SSI 73K212 is ideal for use in either free standing or integral system modem products where full-duplex 1200 bps data communications over the 2-wire switched telephone network is desired. Its high functionality, low power consumption and efficient packaging simplify design requirements and increase system reliability. A complete modem requires only the addition of the phone line interface, a control microprocessor, and RS-232 level convertor for a typical system. The SSI 73K212 is part of SSi's K-Series family of pin and function compatible single-chip modem products. These devices allow systems to be configured for higher speeds and Bell or CCITT operation with only a single component change.

ASYNCHRONOUS MODE

Data transmission for the DPSK mode requires that data ultimately be transmitted in a synchronous fashion. The SSI 73K212 includes ASYNC/SYNC and SYNC/ASYNC converters which delete or insert stop bits in order to transmit data at a regular rate. In asynchronous mode the serial data comes from the TXD pin into the ASYNC/SYNC rate converter. The ASYNC/SYNC rate converter accepts the data provided on the TXD pin which normally must be 1200 bit/s +1.0%, -2.5%. The rate converter will then insert or delete stop bits in order to output a signal which is 1200 bit/s ± .01% (± .01% is the crystal tolerance).

The serial data stream from the transmit buffer or the rate converter is passed through the data scrambler and onto the analog modulator. The data scrambler can be bypassed under processor control when unscrambled data must be transmitted. The ASYNC/SYNC rate converter and the data scrambler are bypassed in all FSK modes. If serial input data contains a break signal through one character (including start and stop bits) the break will be extended to at least 2 • N + 3 bits long (where N is the number of transmitted bits/character).

Serial data from the demodulator is passed normally first through the data descrambler and then through the SYNC/ASYNC rate converter. The SYNC/ASYNC convertor will reinsert any deleted stop bits and transmit output data at an intra-character rate (bit-to-bit timing) of no greater than 1219 bit/s. An incoming break signal (low through two characters) will be passed through without incorrectly inserting a stop bit.

Similar to the transmit side, both the SYNC/ASYNC rate converter and the data descrambler are bypassed in the FSK modes.

SYNCHRONOUS MODE

The Bell 212A standard defines synchronous operation only at 1200 bit/s. Operation is similar to that of the asynchronous mode except that data must be synchronized to a provided clock and no variation in data transfer rate is allowable. Serial input data appearing at TXD must be valid on the rising edge of TXCLK.

TXCLK is an internally derived 1200 Hz signal in internal mode and is connected internally to the RXCLK pin in slave mode. Receive data at the RXD pin is clocked out on the falling edge of RXCLK. The ASYNCH/SYNCH converter is bypassed when synchronous mode is selected and data is transmitted out at the same rate as it is input.

DPSK MODULATOR/DEMODULATOR

The SSI 73K212 modulates a serial bit stream into dibit pairs that are represented by four possible phase shifts as prescribed by the Bell 212A standard. The baseband signal is then filtered to reduce intersymbol interference on the bandlimited 2-wire telephone line. Transmission occurs on either a 1200 Hz (originate mode) or 2400 Hz carrier (answer mode). Demodulation is the reverse of the modulation process, with the incoming analog signal eventually decoded into di-bits and converted back to a serial bit stream. The demodulator also recovers the clock which was encoded into the analog signal during modulation. Demodulation occurs using either a 1200 Hz carrier (answer mode or ALB originate mode) or a 2400 Hz carrier (originate mode or ALB answer mode). The SSI 73K212 uses a phase locked loop coherent demodulation technique that offers inherently better performance than typical DPSK demodulators used by other manufacturers.

FSK MODULATOR/DEMODULATOR

The FSK modulator produces a frequency modulated analog output signal using two discrete frequencies to represent the binary data. In the Bell 103, the standard frequencies of 1270 and 1070 Hz (originate, mark and space) or 2225 and 2025 Hz (answer, mark and space) are used. V.21 mode uses 980 and 1180 Hz (originate, mark and space) or 1650 and 1850 Hz (answer, mark and space). Demodulation involves detecting the received frequencies and decoding them into the appropriate binary value. The rate converter and scrambler/descrambler are bypassed in the 103 mode.

PASSBAND FILTERS AND EQUALIZERS

A high and low band filter is included to shape the amplitude and phase response of the transmit and receive signals and provide compromise delay equalization and rejection of out-of-band signals in the receive channel. Amplitude and phase equalization are necessary to compensate for distortion of the transmission line and to reduce intersymbol interference in the bandlimited receive signal. The transmit signal filtering approximates a 75% square root of raised Cosine frequency response characteristic.

AGC

The automatic gain control maintains a signal level at the input to the demodulators which is constant to within 1 dB. It corrects quickly for increases in signal which would cause clipping and provides a total dynamic range of >45 dB.

PARALLEL BUS INTERFACE

Four 8-bit registers are provided for control, option select and status monitoring. These registers are addressed with the AD0, AD1, and AD2 multiplexed address lines (latched by ALE) and appear to a control microprocessor as four consecutive memory locations. Two control registers and the tone register are read/write memory. The status detect register is read only and cannot be modified except by modem response to monitored parameters.

SERIAL COMMAND INTERFACE

The serial command mode allows access to the SSI 73K212 control and status registers via a serial command port (22-pin version only). In this mode the A0, A1 and A2 lines provide register addresses for data passed through the data pin under control of the $\overline{RD}$ and $\overline{WR}$ lines. A read operation is initiated when the $\overline{RD}$ line is taken low. The next eight cycles of EXCLK will then transfer out eight bits of the selected address location LSB first. A write takes place by shifting in eight bits of data LSB first for eight consecutive cycles of EXCLK. $\overline{WR}$ is then pulsed low and data transferred into the selected register occurs on the rising edge of $\overline{WR}$.

SPECIAL DETECT CIRCUITRY

The special detect circuitry monitors the received analog signal to determine status or presence of carrier, call-progress tones, answer tone and weak received signal, (long loop condition). An unscrambled mark request signal is also detected when the received data out of the DPSK demodulator before the descrambler has been high for 165.5 ms ± 6.5 ms. The appropriate status bit is set when one of these conditions changes and an interrupt is generated for all purposes except long loop. The interrupts are disabled (masked) when the enable interrupt bit is set to 0.

DTMF GENERATOR

The DTMF generator will output one of 16 standard dual-tones determined by a 4-bit binary value and TX DTMF mode bit previously loaded into the tone register. Transmission of DTMF tones is initiated when the DTMF mode is selected and the transmit enable (CR0 bit D1) is changed from 0 to 1.

PIN DESCRIPTION

POWER

NAME	28-PIN	22-PIN	TYPE	DESCRIPTION
GND	28	1	I	System Ground.
VDD	15	11	I	Power supply input, 12V +10%, -20% (or 5V ±10%). Bypass with .1 and 22 µF capacitors to ground.
Vref	26	21	O	An internally generated reference voltage. Bypass with .1 µF capacitor to Ground.
Iset	24	19	I	Chip current reference. Sets bias current for op-amps. The chip current is set by connecting this pin to VDD through a 2 MΩ resistor. (Previous Data Sheets showed 4 MΩ, but 2 MΩ should be used with current production). Iset should be bypassed to GND with a .1 µF capacitor.

PARALLEL MICROPROCESSOR INTERFACE

ALE	12	-	I	Address latch enable. The falling edge of ALE latches the address on AD0-AD2 and the chip select on $\overline{CS}$.
AD0-AD7	4-11	-	I/O	Address/data bus. These bidirectional tri-state multiplexed lines carry information to and from the internal registers.
$\overline{CS}$	20	-	I	Chip select. A low on this pin allows a read cycle or a write cycle to occur. AD0-AD7 will not be driven and no registers will be written if $\overline{CS}$ (latched) is not active. $\overline{CS}$ is latched on the falling edge of ALE.
CLK	1	2	O	Output clock. This pin is selectable under processor control to be either the crystal frequency (for use as a processor clock) or 16 x the data rate for use as a baud rate clock in DPSK modes only. The pin defaults to the crystal frequency on reset.
$\overline{INT}$	17	13	O	Interrupt. This open drain output signal is used to inform the processor that a detect flag has occurred. The processor must then read the detect register to determine which detect triggered the interrupt. $\overline{INT}$ will stay active until the processor reads the detect register or does a full reset.
$\overline{RD}$	14	-	I	Read. A "low" requests a read of the SSI 73K212 internal registers. Data cannot be output unless both $\overline{RD}$ and the latched $\overline{CS}$ are active or "low."
RESET	25	20	I	Reset. An active signal "high" on this pin will put the chip into an inactive state. All control register bits (CR0, CR1, Tone) will be reset. The output of the CLK pin will be set to the crystal frequency. An internal pull down resistor permits power on reset using a capacitor to VDD.

PARALLEL MICROPROCESSOR INTERFACE (Continued)

NAME	28-PIN	22-PIN	TYPE	DESCRIPTION
$\overline{WR}$	13	-	I	Write. A "low" on this informs the SSI 73K212 that data is available on AD0-AD7 for writing into an internal register. Data is latched on the rising edge of $\overline{WR}$. No data is written unless both $\overline{WR}$ and the latched $\overline{CS}$ are active ("low").

SERIAL MICROPROCESSOR INTERFACE

A0-A2	-	5-7	I	Register Address Selection. These lines carry register addresses and should be valid during any read or write operation.
DATA	-	8	I/O	Serial Control Data. Data for a read/write operation is clocked in or out on the falling edge of the EXCLK pin. The direction of data flow is controlled by the $\overline{RD}$ pin. $\overline{RD}$ low outputs data. $\overline{RD}$ high inputs data.
$\overline{RD}$	-	10	I	Read. A "low" on this input informs the SSI 73K212 that data or status information is being read by the processor. The falling edge of the $\overline{RD}$ signal will initiate a read from the addressed register. The $\overline{RD}$ signal must continue for eight falling edges of EXCLK in order to read all eight bits of the referenced register. Read data is provided LSB first. Data will not be output unless the $\overline{RD}$ signal is active.
$\overline{WR}$	-	9	I	Write. A "low" on this input informs the SSI 73K212 that data or status information has been shifted in through the DATA pin and is available for writing to an internal register. The normal procedure for a write is to shift in data LSB first on the DATA pin for eight consecutive falling edges of EXCLK and then to pulse $\overline{WR}$ low. Data is written on the rising edge of $\overline{WR}$.

Note: In the serial, 22-pin version, the pins AD0-AD7, ALE and $\overline{CS}$ are removed and replaced with the pins; A0, A1, A2, DATA, and an unconnected pin. Also, the $\overline{RD}$ and $\overline{WR}$ controls are used differently.

The serial control mode is provided in the 28-pin version by tying ALE high and $\overline{CS}$ low. In this configuration AD7 becomes DATA and AD0, AD1 and AD2 become A0, A1 and A2, respectively.

RS-232 INTERFACE

NAME	28-PIN	22-PIN	TYPE	DESCRIPTION
EXCLK	19	15	I	External Clock. This signal is used in synchronous transmission when the external timing option has been selected. In the external timing mode the rising edge of EXCLK is used to strobe synchronous DPSK transmit data available on the TXD pin. Also used for serial control interface.
RXCLK	23	18	O	Receive Clock. The falling edge of this clock output is coincident with the transitions in the serial received data output. The rising edge of RXCLK can be used to latch the valid output data. RXCLK will be valid as long as a carrier is present.
RXD	22	17	O	Received Digital Data Output. Serial receive data is available on this pin. The data is always valid on the rising edge of RXCLK when in synchronous mode. RXD will output constant marks if no carrier is detected.
TXCLK	18	14	O	Transmit Clock. This signal is used in synchronous transmission to latch serial input data on the TXD pin. Data must be provided so that valid data is available on the rising edge of the TXCLK. The transmit clock is derived from different sources depending upon the synchronization mode selection. In Internal Mode the clock is generated internally. In External Mode TXCLK is phase locked to the EXCLK pin. In Slave Mode TXCLK is phase locked to the RXCLK pin. TXCLK is always active.
TXD	21	16	I	Transmit Digital Data Input. Serial data for transmission is input on this pin. In synchronous modes, the data must be valid on the rising edge of the TXCLK clock. In asynchronous modes (1200 bit/s or 300 baud) no clocking is necessary. DPSK data must be 1200 bit/s +1%, -2.5%.

ANALOG INTERFACE

RXA	27	22	I	Received modulated analog signal input from the phone line.
TXA	16	12	O	Transmit analog output to the phone line.
XTAL1 XTAL2	2 3	3 4	I I	These pins are for the internal crystal oscillator requiring a 11.0592 MHz parallel mode crystal and two load capacitors to Ground. Consult crystal manufacturer for proper valves. XTAL2 can also be driven from an external clock.

REGISTER DESCRIPTIONS

Four 8-bit internal registers are accessible for control and status monitoring. The registers are accessed in read or write operations by addressing the A0, A1 and A2 address lines in serial mode, or the AD0, AD1 and AD2 lines in parallel mode. The address lines are latched by ALE. Register CR0 controls the method by which data is transferred over the phone line. CR1 controls the interface between the microprocessor and the SSI 73K212 internal state. DR is a detect register which provides an indication of monitored modem status conditions. TR, the tone control register, controls the DTMF generator, answer and guard tones and RXD output gate used in the modem initial connect sequence. All registers are read/write except for DR which is read only. Register control and status bits are identified below:

REGISTER BIT SUMMARY

	ADDRESS	DATA BIT NUMBER							
REGISTER	AD2 - AD0	D7	D6	D5	D4	D3	D2	D1	D0
CONTROL REGISTER 0 CR0	000			TRANSMIT MODE 3	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ANSWER/ ORIGINATE
CONTROL REGISTER 1 CR1	001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTERRUPT	BYPASS SCRAMBLER	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0
DETECT REGISTER DR	010			RECEIVE DATA	UNSCR. MARKS	CARRIER DETECT	ANSWER TONE	CALL PROGRESS	LONG LOOP
TONE CONTROL REGISTER TR	011	RXD OUTPUT CONTROL		TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF3	DTMF2	DTMF1	DTMF0
CONTROL REGISTER 2 CR2	100				THESE REGISTER LOCATIONS ARE RESERVED FOR				
CONTROL REGISTER 3 CR3	101				USE WITH OTHER K-SERIES FAMILY MEMBERS				
ID REGISTER ID	110	0	0						

NOTE: When a register containing reserved control bits is written into, the reserved bits must be programmed as 0's.

REGISTER ADDRESS TABLE

REGISTER	ADDRESS AD2 - AD0	DATA BIT NUMBER D7	D6	D5	D4	D3	D2	D1	D0
CONTROL REGISTER 0 CR0	000			TRANSMIT MODE 3	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ORIGINATE/ ANSWER
				0000=PWR DOWN 0001=INT SYNCH 0010=EXT SYNCH 0011=SLAVE SYNCH 0100=ASYNCH 8 BITS/CHAR 0101=ASYNCH 9 BITS/CHAR 0110=ASYNCH 10 BITS/CHAR 0111=ASYNCH 11 BITS/CHAR 1100=FSK				0=SQUELCH ANALOG 1=ENABLE ANALOG	0=ANSWER 1=ORIGINATE
CONTROL REGISTER 1 CR1	001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTERRUPT	BYPASS SCRAMBLER	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0
		00=TX DATA 01=TX ALTERNATE 10=TX MARK 11=TX SPACE		0=OFF 1=ON	0=NORMAL 1=BYPASS SCRAMBLER	0=XTAL 1=16 X DATA RATE OUTPUT AT CLK PIN IN DPSK MODE ONLY	0=NORMAL 1=RESET	00=NORMAL 01=ANALOG LOOPBACK 10=REMOTE DIGITAL LOOPBACK 11=LOCAL DIGITAL LOOPBACK	
DETECT REGISTER DR	010			RECEIVE DATA	UNSCR. MARKS	CARRIER DETECT	ANSWER TONE	CALL PROGRESS	LONG LOOP
				OUTPUTS RECEIVED DATA STREAM	0=CONDITION NOT DETECTED 1=CONDITION DETECTED				
TONE CONTROL REGISTER TR	011	RXD OUTPUT CONTROL		TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF3	DTMF2	DTMF1	DTMF0
		RXD PIN 0=NORMAL 1=TRI STATE		0=OFF 1=ON	0=DATA 1=TX DTMF	4 BIT CODE FOR 1 OF 16 DUAL TONE COMBINATIONS.			
ID REGISTER ID	110	ID BIT 1	ID BIT 0						
		00=73K212 or 73K322 01=73K221 or 73K302L 10=73K222 11=73K224							

CONTROL REGISTER 0

	D7	D6	D5	D4	D3	D2	D1	D0
CR0 000			TRANSMIT MODE 3	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ANSWER/ ORIGINATE

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	Answer/ Originate	0	Selects answer mode (transmit in high band, receive in low band).
		1	Selects originate mode (transmit in low band, receive in high band).
D1	Transmit Enable	0	Disables transmit output at TXA.
		1	Enables transmit output at TXA.
			Note: Answer tone and DTMF TX control require TX enable.
D5, D4, D3, D2	Transmit Mode	D5 D4 D3 D2	
		0 0 0 0	Selects power down mode. All functions disabled except digital interface.
		0 0 0 1	Internal synchronous mode. In this mode TXCLK is an internally derived 1200 Hz signal. Serial input data appearing at TXD must be valid on the rising edge of TXCLK. Receive data is clocked out of RXD on the falling edge of RXCLK.
		0 0 1 0	External synchronous mode. Operation is identical to internal synchronous, but TXCLK is connected internally to EXCLK pin, and a 1200 Hz clock must be supplied externally.
		0 0 1 1	Slave synchronous mode. Same operation as other synchronous modes. TXCLK is connected internally to the RXCLK pin in this mode.
		0 1 0 0	Selects PSK asynchronous mode - 8 bits/character (1 start bit, 6 data bits, 1 stop bit).
		0 1 0 1	Selects PSK asynchronous mode - 9 bits/character (1 start bit, 7 data bits, 1 stop bit).
		0 1 1 0	Selects PSK asynchronous mode - 10 bits/character (1 start bit, 8 data bits, 1 stop bit).
		0 1 1 1	Selects PSK asynchronous mode - 11 bits/character (1 start bit, 8 data bits, Parity and/or 1 or 2 stop bits).
		1 1 0 0	Selects FSK operation.
D6		0	Not used, must be written as "0."

CONTROL REGISTER 1

	D7	D6	D5	D4	D3	D2	D1	D0
CR1 001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTER.	BYPASS SCRAMB	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0

BIT NO.	NAME	CONDITION	DESCRIPTION
D1, D0	Test Mode	D1 D0	
		0 0	Selects normal operating mode.
		0 1	Analog loopback mode. Loops the transmitted analog signal back to the receiver, and causes the receiver to use the same center frequency as the transmitter. To squelch the TXA pin, transmit enable bit must be low.
		1 0	Selects remote digital loopback. Received data is looped back to transmit data internally, and RXD is forced to a mark. Data on TXD is ignored.
		1 1	Selects local digital loopback. Internally loops TXD back to RXD and continues to transmit data carrier at the TXA pin.
D2	Reset	0	Selects normal operation.
		1	Resets modem to power down state. All control register bits (CR0, CR1, Tone) are reset to zero. The output of the clock pin will be set to the crystal frequency on reset.
D3	CLK Control (Clock Control)	0	Selects 11.0592 MHz crystal echo output at CLK pin.
		1	Selects 16 X the data rate, output at CLK pin in DPSK modes only.
D4	Bypass Scrambler	0	Selects normal operation. DPSK transmit data is passed through scrambler.
		1	Selects Scrambler Bypass. Bypass DPSK data is routed around scrambler in the transmit path.
D5	Enable Detect Interrupt	0	Disables interrupt at $\overline{INT}$ pin. All interrupts are normally disabled in power down modes.
		1	Enables $\overline{INT}$ output. An interrupts will be generated with a change in status of DR bits D1-D4. The answer tone and call progress detect interrupts are masked when the TX enable bit is set. Carrier detect is masked when TX DTMF is activated. All interrupts will be disabled if the device is in power down mode.

CONTROL REGISTER 1 (Continued)

	D7	D6	D5	D4	D3	D2	D1	D0
CR1 001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTER.	BYPASS SCRAMB	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0

BIT NO.	NAME	CONDITION	DESCRIPTION
D7, D6	Transmit Pattern	D7 D6	
		0 0	Selects normal data transmission as controlled by the state of the TXD pin.
		0 1	Selects an alternating mark/space transmit pattern for modem testing.
		1 0	Selects a constant mark transmit pattern.
		1 1	Selects a constant space transmit pattern.

DETECT REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
DR 010			RECEIVE DATA	UNSCR. MARK	CARR. DETECT	ANSWER TONE	CALL PROG.	LONG LOOP

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	Long Loop	0	Indicates normal received signal.
		1	Indicates low received signal.
D1	Call Progress Detect	0	No call progress tone detected.
		1	Indicates presence of call progress tones. The call progress detection circuitry is activated by energy in the 350 to 620 Hz call progress bandwidth.
D2	Answer Tone Received	0	No answer tone detected.
		1	Indicates detection of 2225 Hz answer tone. The device must be in originate mode for detection of answer tone in normal operation.
D3	Carrier Detect	0	No carrier detected in the receive channel.
		1	Indicated carrier has been detected in the received channel.
D4	Unscr. Mark (Unscrambled Mark)	0	No unscrambled mark.
		1	Indicates detection of unscrambled marks in the received data. A valid indication requires that unscrambled marks be received for > 165.5 ± 6.5 ms.

DETECT REGISTER (Continued)

	D7	D6	D5	D4	D3	D2	D1	D0
DR 010			RECEIVE DATA	UNSCR. MARK	CARR. DETECT	ANSWER TONE	CALL PROG.	LONG LOOP

BIT NO.	NAME	CONDITION	DESCRIPTION
D5	Receive Data		Continuously outputs the received data stream. This data is the same as that output on the RXD pin, but it is not disabled when RXD is tri-stated.
D6, D7			Not used.

TONE REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
TR 011	RXD OUTPUT CONTR.		TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF 3	DTMF 2	DTMF 1	DTMF 0

BIT NO.	NAME	CONDITION	DESCRIPTION
D3, D2, D1, D0	DTMF	D3 D2 D1 D0 0 0 0 0 - 1 1 1 1	Programs 1 of 16 DTMF tone pairs that will be transmitted when TX DTMF and TX enable bit (CR0, bit D1) is set. Tone encoding is shown below:

KEYBOARD EQUIVALENT	DTMF CODE D3 D2 D1 D0	TONES LOW HIGH
1	0 0 0 1	697 1209
2	0 0 1 0	697 1336
3	0 0 1 1	697 1477
4	0 1 0 0	770 1209
5	0 1 0 1	770 1336
6	0 1 1 0	770 1477
7	0 1 1 1	852 1209
8	1 0 0 0	852 1336
9	1 0 0 1	852 1477
0	1 0 1 0	941 1336
*	1 0 1 1	941 1209
#	1 1 0 0	941 1477
A	1 1 0 1	697 1633
B	1 1 1 0	770 1633
C	1 1 1 1	852 1633
D	0 0 0 0	941 1633

TONE REGISTER (Continued)

	D7	D6	D5	D4	D3	D2	D1	D0
TR 011	RXD OUTPUT CONTR.		TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF 3	DTMF 2	DTMF 1	DTMF 0

BIT NO.	NAME	CONDITION	DESCRIPTION
D4	TX DTMF (Transmit DTMF)	0	Disabled DTMF.
		1	Activates DTMF. The selected DTMF tones are transmitted continuously when this bit is high (with Transmit Enable, CR0-D1). TX DTMF overrides all other transmit functions.
D5	TX ANS (Transmit Answer tone)	0	Disables answer tone generator.
		1	Enables answer tone generator. A 2225 Hz answer tone will be transmitted continuously when the Transmit Enable bit is set in CR0. The device must be in answer mode.
D7	RXD Output Control	0	Enables RXD pin. Receive data will be output on RXD.
		1	Disables RXD pin. The RXD pin reverts to a high impedance with internal, weak pull-up resistor.

ID REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
ID 110	ID 1	ID 0						

BIT NO.	NAME	CONDITION	DESCRIPTION
D7, D6	Device Identification Signature	D7 D6	Indicates Device:
		0 0	SSI 73K212(L) or 73K322L
		0 1	SSI 73K221(L) or 73K302L
		1 0	SSI 73K222(L)
		1 1	SSI 73K224(L)

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
VDD Supply Voltage	14	V
Storage Temperature	-65 to 150	°C
Soldering Temperature (10 sec.)	260	°C
Applied Voltage	-0.3 to VDD+0.3	V

Note: All inputs and outputs are protected from static charge using built-in, industry standard protection devices and all outputs are short-circuit protected.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
VDD Supply Voltage					
5V Version (73K212L)		4.5	5	5.5	V
12V Version (73K212)		9.6	12	13.2	V
Digital Inputs					
VIH, Input High Voltage					
Reset, XTAL1, XTAL2		3.0		VDD	V
All other inputs		2.0		VDD	V
VIL, Input Low Voltage		0		0.8	V
IOH, Output High Current		-0.4			mA
IOL, Output Low Current				1.6	mA
TA, Operating Free-Air Temperature		-40		+85	°C
External Component (Refer to Application section for placement.)					
VREF Bypass capacitor	(VREF to GND)	0.1			µF
Bias setting resistor	(Placed between VDD and ISET pins)	1.8	2	2.2	MΩ
ISET Bypass capacitor	(ISET pin to GND)	0.1			µF
VDD Bypass capacitor 1	(VDD to GND)	0.1			µF
VDD Bypass capacitor 2	(VDD to GND)	22			µF
Clock Variation	(11.0592 MHz) Crystal or external clock	-0.01		+0.01	%

ELECTRICAL SPECIFICATIONS (Continued)

DC ELECTRICAL CHARACTERISTICS

(TA = -40°C to 85°C, VDD = recommended range unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
IDD, Supply Current	CLK = 11.0592 MHz				
5V Version	ISET Resistor = 2 MΩ				
IDDA, Active			6	9	mA
IDD1, Power-down	CLK = 11.0592 MHz			4	mA
IDD2, Power-down	CLK = 19.200 KHz			3	mA
12V Version	CLK = 11.0592 MHz				
IDDA, Active	ISET Resistor = 2 MΩ		15	25	mA
IDD1, Power-down	CLK = 11.0592 MHz		6	12.5	mA
IDD2, Power-down	CLK = 19.200 KHz		5	12.5	mA
Digital Inputs					
IIH, Input High Current	VI = VIH MAX			100	µA
IIL, Input Low Current	VI = VIL MIN	-200			µA
Reset Pull-down Current	Reset = VDD	1		50	µA
Digital Outputs					
VOH, Output High Voltage					
5V Version (73K212L)	IO = IOH MIN	2.4		VDD	V
12V Version (73K212)	IO = IOH MIN	2.4			V
VOL, Output Low Voltage	IO = IOL MAX			0.4	V
VOL, CLK Output	IO = 3.6 mA			0.6	V
RXD Tri-State Pull-up Curr.	RXD = GND	-1		-50	µA
Capacitance					
Inputs	Capacitance, all Digital Input pins			10	pF
XTAL1, 2 Load Capacitors	Depends on crystal	15		60	pF
CLK	Maximum Capacitive Load			15	pF

ELECTRICAL SPECIFICATION (Continued)

DYNAMIC CHARACTERISTICS AND TIMING

(TA = -40°C to + 85°C, VDD = recommended range unless otherwise noted.)

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNITS
PSK Modulator					
Carrier Suppression	Measured at TXA	55			dB
Output Amplitude	TX scrambled marks	-11	-10.0	-9	dBm0
FSK Mod/Demod					
Output Freq. Error	CLK = 11.0592 MHz	-0.35		+.35	%
Transmit Level	Transmit Dotting Pattern	-11	-10.0	-9	dBm0
Harmonic Distortion in 700-2900 Hz band	THD in the alternate band DPSK or FSK		-60	-50	dB
Output Bias Distortion	Transmit Dotting Pattern In ALB @ RXD		±8		%
Total Output Jitter	Random Input in ALB @ RXD	-15		+15	%
DTMF Generator					
Freq. Accuracy		-.25		+.25	%
Output Amplitude	Low-Band, DPSK Mode	-10	-9	-8	dBm0
Output Amplitude	High-Band, DPSK Mode	-8	-7	-6	dBm0
Twist	High-Band to Low-Band	1.0	2.0	3.0	dB
Long Loop Detect	DPSK or FSK	-38		-28	dBm0
Dynamic Range	Refer to Performance Curves		45		dB
Call Progress Detector					
Detect Level	2-Tones in 350-600 Hz band	-34		0	dBm0
Reject Level	2-Tones in 350-600 Hz band			-41	dBm0
Delay Time	-70 dBm0 to -30 dBm0 STEP	27		80	ms
Hold Time	-30 dBm0 to -70 dBm0 STEP	27		80	ms
Hysteresis		2			dB

Note: Parameters expressed in dBm0 refer to the following definition:

12V Version
- 10 dB loss in the Transmit path to the line.
- 9 dB gain in the Receive path from the line.

5V Version
- 0 dB loss in the Transmit path to the line.
- 2 dB gain in the Receive path from the line.

Refer to the Basic Box Modem diagram in the Applications section for the DAA design.

ELECTRICAL SPECIFICATION (Continued)

DYNAMIC CHARACTERISTICS AND TIMING (Continued)

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNITS
Carrier Detect					
Threshold	DPSK or FSK receive data	-49		-42	dBm0
Delay Time	-70 dBm0 to -30 dBm0 STEP	15		45	ms
Hysteresis	Single tone detected	2	3		dB
Hold Time	-30 dBm0 to -70 dBm0 STEP	10		24	ms
Answer Tone Detector					
Detect Level	In FSK mode	-49		-42	dBm0
Delay Time	-70 dBm0 to -30 dBm0 STEP	20		45	ms
Hold Time	-30 dBm0 to -70 dBm0 STEP	10		30	ms
Detect Freq. Range		-2.5		+2.5	%
Output Smoothing Filter					
Output Impedance	TXA pin		200	300	Ω
Output load	TXA pin; FSK Single	10			KΩ
	Tone out for THD = -50 db in .3 to 3.4 KHz			50	pF
Spurious Freq. Comp.	Frequency = 76.8 KHz			-39	dBm0
	Frequency = 153.6 KHz			-45	dBm0
Clock Noise	TXA pin; 76.8 KHz				
5V Version (73K212L)				1.0	mVrms
12V Version (73K212)				2	mVrms
Carrier VCO					
Capture Range	Originate or Answer	-10		+10	Hz
Capture Time	-10 Hz to +10 Hz Carrier Freq. Change Assum.		40	100	ms
Recovered Clock					
Capture Range	% of frequency center frequency (center at 1200 Hz)	-625		+625	ppm
Data Delay Time	Analog data in at RXA pin to receive data valid at RXD pin		30	50	ms

ELECTRICAL SPECIFICATION (Continued)

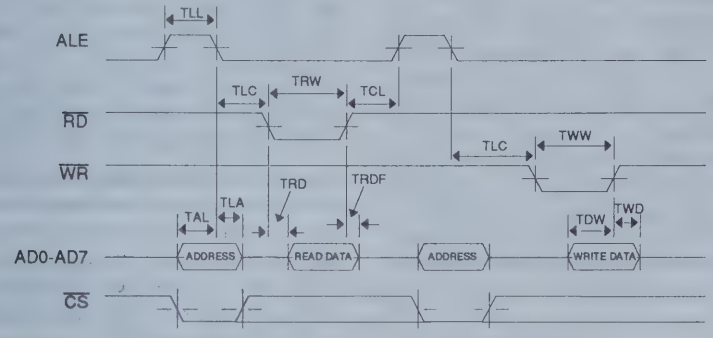
DYNAMIC CHARACTERISTICS AND TIMING (Continued)

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNITS
Timing (Refer to Timing Diagrams)					
TAL	$\overline{CS}$/Addr. setup before ALE	30			ns
TLA	$\overline{CS}$/Addr. Hold after latch	20			ns
TLC	Latch to $\overline{RD}$/$\overline{WR}$ control	40			ns
TCL	$\overline{RD}$/$\overline{WR}$ Control to Latch	10			ns
TRD	Data out from $\overline{RD}$	0		160	ns
TLL	ALE width	60			ns
TRDF	Data float after READ	0		80	ns
TRW	READ width	200		25000	ns
TWW	WRITE width	140		25000	ns
TDW	Data setup before WRITE	150			ns
TWD	Data hold after WRITE	20			ns
TCKD	Data out after CLK			200	ns
TCKW	WRITE after CLK	150			ns
TDCK	Data setup before CLK	150			ns
TAC	Address setup before control [1]	50			ns
TCA	Address hold after control [1]	50			ns

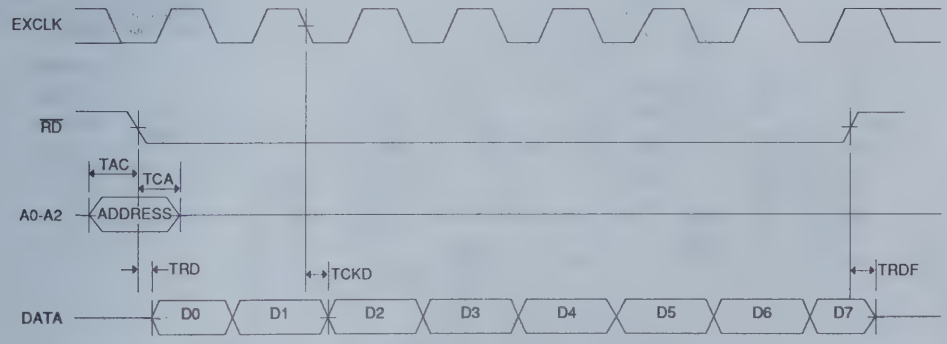
1: Control for setup is the falling edge of $\overline{RD}$ or $\overline{WR}$.
Control for hold is the falling edge of $\overline{RD}$ or the rising edge of $\overline{WR}$.

TIMING DIAGRAMS

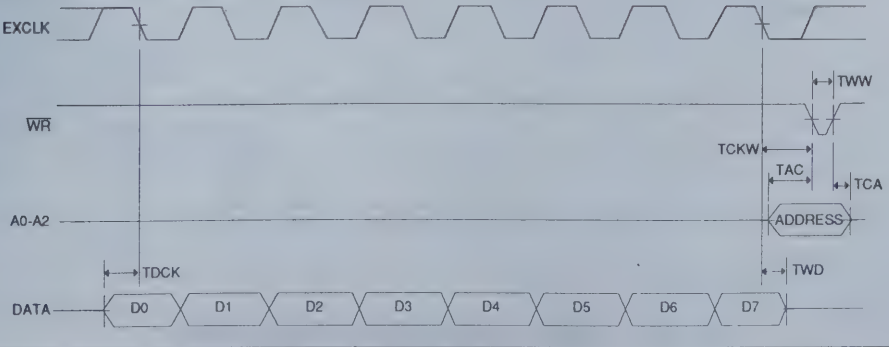
BUS TIMING DIAGRAM (PARALLEL VERSION)



READ TIMING DIAGRAM (SERIAL VERSION)



WRITE TIMING DIAGRAM (SERIAL VERSION)



APPLICATIONS INFORMATION

GENERAL CONSIDERATIONS

Figures 1 and 2 show the basic circuit diagram for K–Series modem integrated circuits. K-Series products are designed to be used in conjunction with a control processor, a UART or RS-232 serial data interface, and a DAA phone line interface to function as a typical intelligent modem. The K-Series ICs interface directly with Intel 8048 and 80C51 microprocessors for control and status monitoring purposes. Two typical DAA arrangements are shown: one for a split ±5 or ±12 volt design and one for a single 5 volt design. These diagrams are for reference only and do not represent production-ready modem designs.

K-Series devices are available in two control interface versions: one for a parallel multiplexed address/data interface, and one for a serial interface. The parallel version is intended for use with 8039/48 or 8031/51 microcontrollers from Intel or many other manufacturers. The serial interface 22-pin version can be used with other microcontrollers or in applications where only a limited number of port lines are available. The parallel versions may also be used in the serial mode, as explained in the data sheet pin description.

In most applications the controller will monitor the serial data for commands from the DTE and the received data for break signals from the far end modem. In this way, command data to the modem is sent over the same data line as the transmitted data. In other applications the RS-232 interface handshake lines are used for modem control.

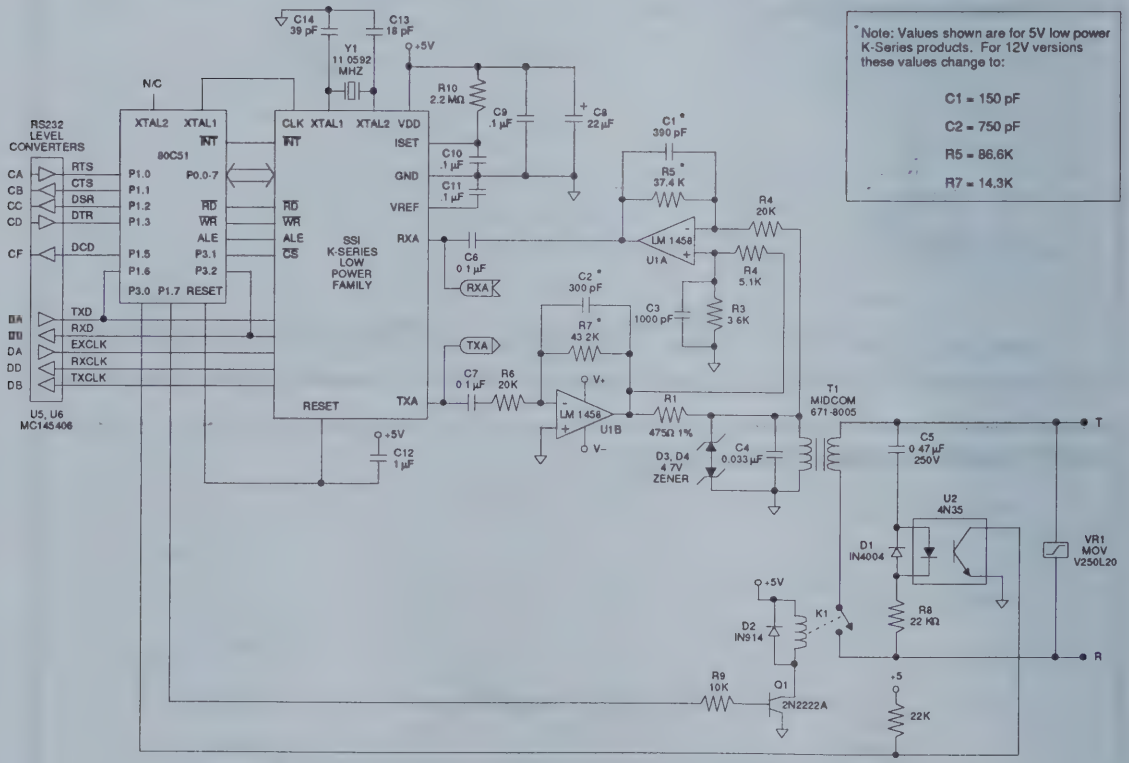


FIGURE 1: Basic Box Modem with Dual-Supply DAA

DIRECT ACCESS ARRANGEMENT (DAA)

The DAAs shown are two examples of how the "hybrid" may be implemented. The split supply design (Figure 1) is a typical two op-amp hybrid. The receive op-amp serves two purposes. It supplies gain to amplify the receive signal to the proper level for the modem's detectors and demodulator, and it removes the transmitted signal from the receive signal present at the transformer. This is done by supplying a portion of the transmitted signal to the non-inverting input of the receive op-amp at the same amplitude as the signal appearing at the transformer, making the transmit signal common mode.

The single-supply DAA is more complex than the dual-supply version described above, but its use eliminates the need for a second power supply. This DAA (Figure 2) uses a bridged drive to allow undistorted signals to be sent with a single 5 volt supply. Because DTMF tones utilize a higher amplitude than data, these signals will clip if a single-ended drive approach is used. The bridged driver uses an extra op-amp (U1A) to invert the signal coming from the gain setting op-amp (U1B) before sending it to the other leg of the transformer. Each op-amp then supplies half the drive signal to the transformer. The receive amplifier (op-amp C) picks off its signal at the junction of the impedance matching resistor and the transformer. Because the bottom leg of the transformer is being driven in one direction by U1A and the resistor is driven in the opposite direction at the same time by U1B, the summing point of the transformer and resistor remains relatively constant and the receive signal is unaffected.

DESIGN CONSIDERATIONS

Silicon Systems 1-chip modem products include all basic modem functions on a single IC, accessible from a standard bus interface. This makes these devices adaptable for use in a variety of applications, and as easy to control as conventional digital bus peripherals.

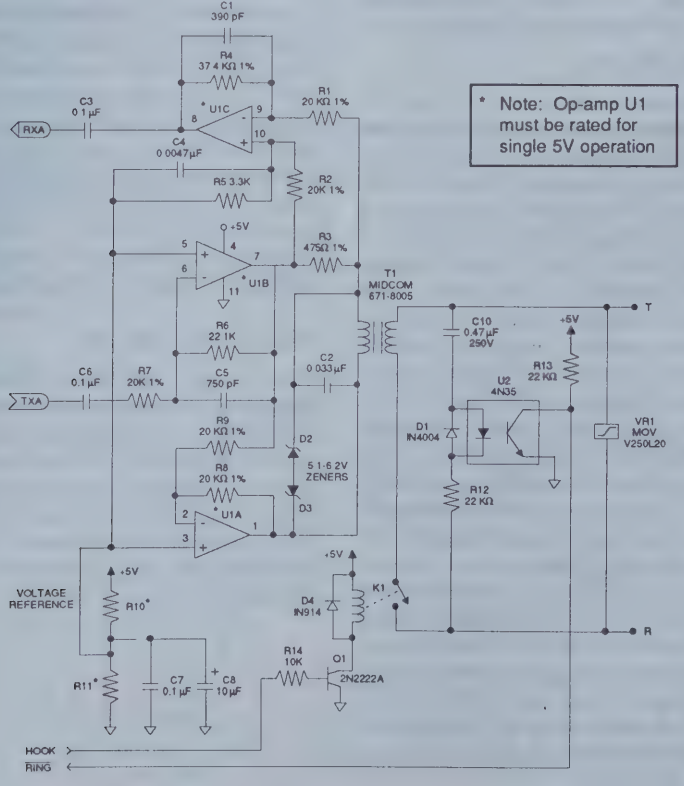


FIGURE 2: Single 5V DAA Version

Unlike digital logic circuitry, however, modem designs must properly contend with precise frequency tolerances, and very low level analog signals, to insure acceptable performance. Using good analog circuit design practices will generally result in a sound design. Folllowing are additional recommendations which should be taken into consideration when starting new designs.

CRYSTAL OSCILLATOR

The K-Series crystal oscillator requires a parallel mode (antiresonant) crystal which operates at 11.0592 MHz. It is important that this precise frequency be maintained to within ±.01% accuracy.

In order for a parallel mode crystal to operate correctly and to specification, it must have a load capacitor connected to the junction of each of the crystal and internal inverter connections, terminated to ground. The values of these capacitors depend primarily on the crystal's characteristics, and to a lesser degree on the internal inverter circuit. The values used affect the accuracy and start up characteristics of the oscillator.

LAYOUT CONSIDERATIONS

Good analog/digital design rules must be used to control system noise in order to obtain highest performance in modem designs. The more digital circuitry present on the PC board, the more this attention to noise control is needed. The modem should be treated as a high impedance analog device. A 22 µF electrolytic capacitor in parallel with a 0.1 µF ceramic capacitor between VDD and ground is recommended. Liberal use of ground planes and larger traces on power and ground are also highly favored. High speed digital circuits tend to generate a significant amount of EMI (Electro-Magnetic Interference) which must be minimized in order to meet regulatory agency limitations. To accomplish this, high speed digital devices should be locally bypassed, and the DAA and K-Series device should be located close to each other near the area of the board where the phone line connection is accessed. To avoid problems, power supply and ground traces should be routed separately to the analog and digital functions on the board, and digital signals should not be routed near low level or high impedance analog traces. The analog and digital grounds should only connect at one point near the analog supplies to avoid ground loops. The K–Series modem IC's should have both high frequency and low frequency bypassing as near to the package as possible.

MODEM PERFORMANCE CHARACTERISTICS

The curves presented here define modem IC performance under a variety of line conditions while inducing disturbances that are typical of those encountered during data transmission on public service telephone lines. Test data was taken using an AEA Electronics' "Autotest I" modem test set and line simulator, operating under computer control. All tests were run full-duplex, using a Concord Data Systems 224 as the reference modem. A 511 pseudo-random-bit pattern was used with $1X10^6$ bits transmitted for each data point. Noise was C-message weighted and all signal-to-noise (S/N) ratios reflect total power measurements similar to the CCITT V.56 measurement specification. The individual tests are defined as follows.

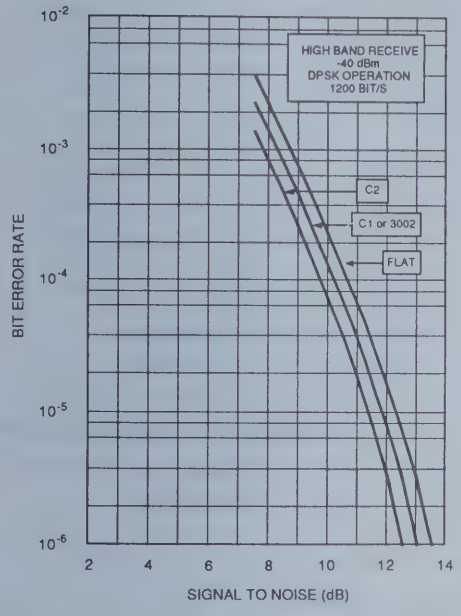
BER vs.S/N

This test measures the ability of the modem to operate over noisy lines with a minimum of data-transfer errors. Since some noise is generated in the best of dial-up lines, the modem must operate with the lowest S/N ratio possible. Optimum modem performance is indicated by test curves that are closest to the zero axis. A narrow spread between curves representing the four line parameters indicates minimal variation in performance while operating over a range of aberrant operating conditions. Typically, a PSK modem will exhibit better BER-performance test curves operating in the highband range than in the lowband.

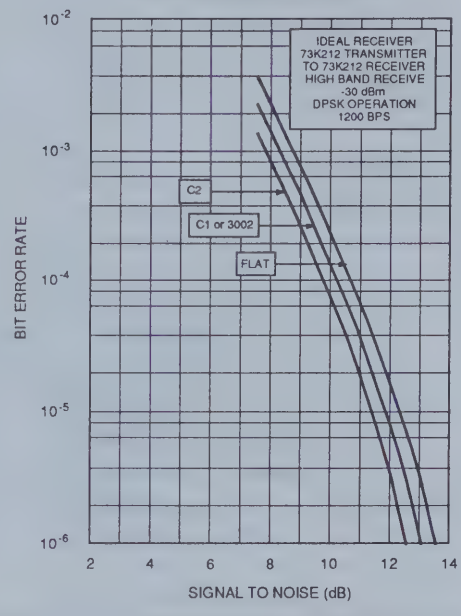
BER vs. Receive Level

This test measures the dynamic range of the modem. Because signal levels vary widely over dial-up lines, the widest possible dynamic range is desirable. The minimum Bell specification calls for 36 dB of dynamic range. S/N ratios are held constant at the indicated values while the receive level is lowered from a very high to very low signal levels. The width of the "bowl" of these curves, taken at the BER point, is the measure of dynamic range.

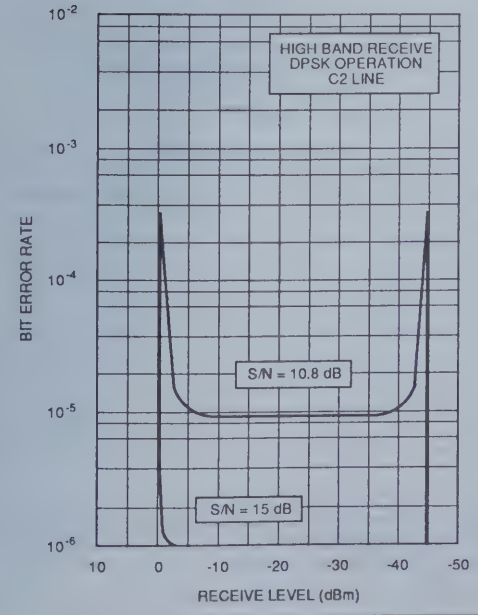
SSI 73K212, 73K212L
BER vs S/N



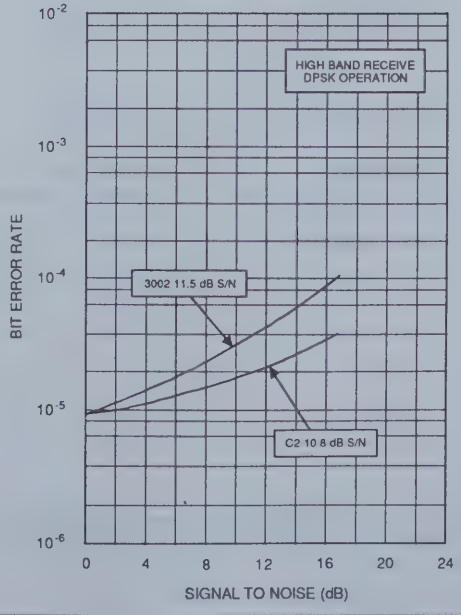
SSI 73K212, 73K212L
BER vs IDEAL RECEIVER

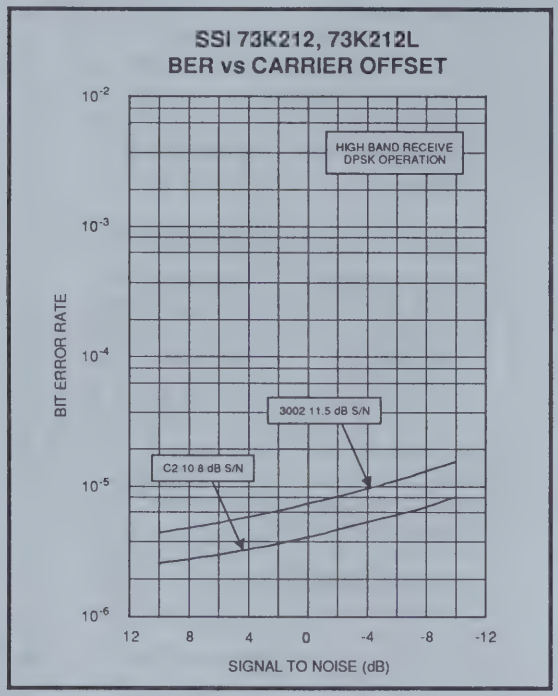


SSI 73K212, 73K212L
BER vs RECEIVE LEVEL

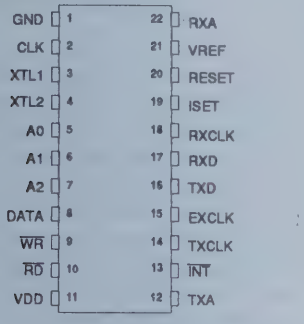


SSI 73K212, 73K212L
BER vs PHASE JITTER

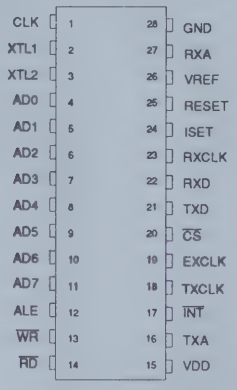



SSI 73K212, 73K212L
BER vs CARRIER OFFSET
HIGH BAND RECEIVE
DPSK OPERATION
3002 11.5 dB S/N
C2 10.8 dB S/N
BIT ERROR RATE
10-2
10-3
10-4
10-5
10-6
12
8
4
0
-4
-8
-12
SIGNAL TO NOISE (dB)

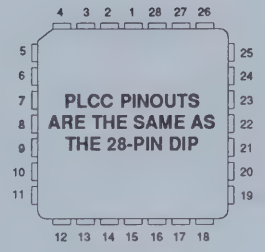
PACKAGE PIN DESIGNATIONS
(TOP VIEW)



400-Mil
22-Pin DIP



600-Mil
28-Pin DIP



28-Lead
PLCC

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 73K212 with Parallel Bus Interface		
28-Pin 12 Volt Supply		
Plastic Dual-In-Line	73K212 – IP	SSI 73K212 – IP
Plastic Leaded Chip Carrier	73K212 – IH	SSI 73K212 – IH
28-Pin 5 Volt Supply		
Plastic Dual-In-Line	73K212L – IP	SSI 73K212L – IP
Plastic Leaded Chip Carrier	73K212L – IH	SSI 73K212L – IH
SSI 73K212 with Serial Interface		
22-Pin 12 Volt Supply		
Plastic Dual-In-Line	73K212S – IP	SSI 73K212S – IP
22-Pin 5 Volt Supply		
Plastic Dual-In-Line	73K212SL – IP	SSI 73K212SL – IP

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NOTES:

SSI 73K221/K221L
CCITT V.22, V.21
Single-Chip Modem

July, 1989

1

DESCRIPTION

The SSI 73K221 is a highly integrated single-chip modem IC which provides the functions needed to construct a CCITT V.22 and V.21 compatible modem, capable of 1200 or 0-300 bit/s full-duplex operation over dial-up lines. The SSI 73K221 is an enhancement of the SSI 73K212 single-chip modem with performance characteristics suitable for European and Asian telephone systems. The SSI 73K221 produces either 550 or 1800 Hz guard tone, recognizes and generates a 2100 Hz answer tone, and allows V.21 fallback for 300 Hz FSK operation. The SSI 73K221 integrates analog, digital, and switched-capacitor array functions on a single substrate, offering excellent performance and a high level of functional integration in a single 28- or 22-pin DIP configuration. The SSI 73K221L, low power version of the SSI 73K221 provides identical performance and features, but operates from a single +5 volt supply with substantially lower power consumption.

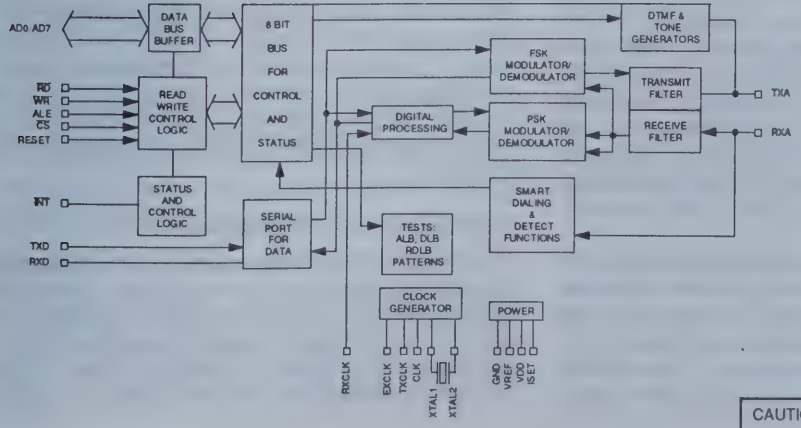
The SSI 73K221 includes the DPSK and FSK modulator/demodulator functions, call progress and handshake tone monitor test modes, and a tone generator capable of producing DTMF, answer and 550 or 1800 Hz guard tone. This device supports V.22 (except mode v) and V. 21 modes of operation, allowing

(Continued)

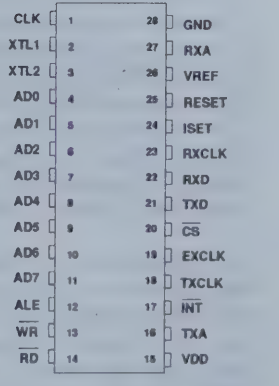
FEATURES

- One-chip CCITT V.22 and V.21 standard compatible modem
- Full-duplex Operation at 0-300 bit/s (FSK) or 600 and 1200 bit/s (DPSK)
- Pin and software compatible with other SSI K–Series 1-chip modems
- Interfaces directly with standard microprocessors (8048, 80C51 typical)
- Serial (22-pin DIP) or parallel (28-pin DIP) microprocessor bus for control
- Serial port for data transfer
- Both synchronous and asynchronous modes of operation
- Call progress, carrier, precise answer tone (2100 Hz), and long loop detectors
- DTMF, and 550 or 1800 Hz guard tone generators
- Test modes available: ALB, DL, RDL, Mark, Space, Alternating bit patterns
- Precise automatic gain control allows 45 dB dynamic range
- Space efficient 22- or 28-pin DIP packages
- CMOS technology for low power consumption using 30 mW @ 5V or 180 mW @ 12V
- Single +5 volt (73K221L) or +12 volt (73K221) versions

BLOCK DIAGRAM



PIN DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

DESCRIPTION (Continued)

both synchronous and asynchronous communications. The SSI 73K221 is designed to appear to the systems designer as a microprocessor peripheral, and will easily interface with popular one-chip microprocessors (80C51 typical) for control of modem functions through its 8-bit multiplexed address/data bus or via an optional serial command bus. An ALE control line simplifies address demultiplexing. Data communications occurs through a separate serial port only.

OPERATION

The SSI 73K221 is ideal for use in either free standing or integral system modem products where full-duplex 1200 bps data communications over the 2-wire switched telephone network is desired. Its high functionality, low power consumption and efficient packaging simplify design requirements and increase system reliability. A complete modem requires only the addition of the phone line interface, a control microprocessor, and RS-232 level converter for a typical system. The SSI 73K221 is part of SSi's K-Series family of pin and function compatible single-chip modem products. These devices allow systems to be configured for higher speeds and Bell or CCITT operation with only a single component change.

ASYNCHRONOUS MODE

Data transmission for the DPSK mode requires that data ultimately be transmitted in a synchronous fashion, The SSI 73K221 includes ASYNC/SYNC and SYNC/ASYNC converters which delete or insert stop bits in order to transmit data at a regular rate. In asynchronous mode the serial data comes from the TXD pin into the ASYNC/SYNC rate converter. The ASYNC/SYNC rate converter accepts the data provided on the TXD pin which normally must be 1200 or 600 bit/s +1.0%, - 2.5%. The rate converter will then insert or delete stop bits in order to output a signal which is 1200 or 600 bit/s ± .01% (± .01% is the crystal tolerance).

The serial data stream from the transmit buffer or the rate converter is passed through the data scrambler and onto the analog modulator. The data scrambler can be bypassed under processor control when unscrambled data must be transmitted. The ASYNC/SYNC rate converter and the data scrambler are bypassed in all FSK modes. If serial input data contains a break signal through one character (including start and stop bits) the break will be extended to at least 2 • N + 3 bits long (where N is the number of transmitted bits/character).

Serial data from the demodulator is passed normally first through the data descrambler and then through the SYNC/ASYNC rate converter. The SYNC/ASYNC convertor will reinsert any deleted stop bits and transmit output data at an intra-character rate (bit-to-bit timing) of no greater than 1219 bit/s. An incoming break signal (low through two characters) will be passed through without incorrectly inserting a stop bit.

The SYNC/ASYNC converter also has an overspeed mode which allows selection of an output overspeed range of either +1% or +2.3%. In the overspeed mode, some stop bits are output at 7/8 the normal width.

Similar to the transmit side, both the SYNC/ASYNC rate converter and the data descrambler are bypassed in the FSK modes.

SYNCHRONOUS MODE

The CCITT V.22 standard defines synchronous operation at 600 and 1200 bit/s. The Bell 212A standard defines synchronous operation only at 1200 bit/s. Operation is similar to that of the asynchronous mode except that data must be synchronized to a provided clock and no variation in data transfer rate is allowable. Serial input data appearing at TXD must be valid on the rising edge of TXCLK.

TXCLK is an internally derived signal in internal mode and is connected internally to the RXCLK pin in slave mode. Receive data at the RXD pin is clocked out on the falling edge of RXCLK. The ASYNCH/SYNCH converter is bypassed when synchronous mode is selected and data is transmitted out at the same rate as it is input.

DPSK MODULATOR/DEMODULATOR

The SSI 73K221 modulates a serial bit stream into dibit pairs that are represented by four possible phase shifts as prescribed by the V.22 standard. The baseband signal is then filtered to reduce intersymbol interference on the bandlimited 2-wire telephone line. Transmission occurs on either a 1200 Hz (originate mode) or

2400 Hz carrier (answer mode). Demodulation is the reverse of the modulation process, with the incoming analog signal eventually decoded into di-bits and converted back to a serial bit stream. The demodulator also recovers the clock which was encoded into the analog signal during modulation. Demodulation occurs using either a 1200 Hz carrier (answer mode or ALB originate mode) or a 2400 Hz carrier (originate mode or ALB answer mode). The SSI 73K221 uses a phase locked loop coherent demodulation technique that offers inherently better performance than typical DPSK demodulators used by other manufacturers.

FSK MODULATOR/DEMODULATOR

The FSK modulator produces a frequency modulated analog output signal using two discrete frequencies to represent the binary data. V.21 mode uses 980 and 1180 Hz (originate, mark and space) or 1650 and 1850 Hz (answer, mark and space). Demodulation involves detecting the received frequencies and decoding them into the appropriate binary value. The rate converter and scrambler/descrambler are bypassed in the V.21 mode.

PASSBAND FILTERS AND EQUALIZERS

A high and low band filter is included to shape the amplitude and phase response of the transmit and receive signals and provide compromise delay equalization and rejection of out-of-band signals in the receive channel. Amplitude and phase equalization are necessary to compensate for distortion of the transmission line and to reduce intersymbol interference in the bandlimited receive signal. The transmit signal filtering approximates a 75% square root of raised Cosine frequency response characteristic.

AGC

The automatic gain control maintains a signal level at the input to the demodulators which is constant to within 1 dB. It corrects quickly for increases in signal which would cause clipping and provides a total dynamic range of >45 dB.

PARALLEL BUS INTERFACE

Four 8-bit registers are provided for control, optionselect and status monitoring. These registers are addressed with the AD0, AD1, and AD2 multiplexed address lines (latched by ALE) and appear to a control microprocessor as four consecutive memory locations. Two control registers and the tone register are read/write memory. The status detect register is read only and cannot be modified except by modem response to monitored parameters.

SERIAL COMMAND INTERFACE

The serial command mode allows access to the SSI 73K221 control and status registers via a serial command port (22-pin version only). In this mode the A0 , A1 and A2 lines provide register addresses for data passed through the data pin under control of the $\overline{RD}$ and $\overline{WR}$ lines. A read operation is initiated when the $\overline{RD}$ line is taken low. The next eight cycles of EXCLK will then transfer out eight bits of the selected address location LSB first. A write takes place by shifting in eight bits of data LSB first for eight consecutive cycles of EXCLK. $\overline{WR}$ is then pulsed low and data transferred into the selected register occurs on the rising edge of $\overline{WR}$.

SPECIAL DETECT CIRCUITRY

The special detect circuitry monitors the received analog signal to determine status or presence of carrier, call-progress tones, answer tone and weak received signal (long loop condition). An unscrambled mark request signal is also detected when the received data out of the DPSK demodulator before the descrambler has been high for 165.5 ms ± 6.5 ms. The appropriate status bit is set when one of these conditions changes and an interrupt is generated for all purposes except long loop. The interrupts are disabled (masked) when the enable interrupt bit is set to 0.

DTMF GENERATOR

The DTMF generator will output one of 16 standard dual-tones determined by a 4-bit binary value and TX DTMF mode bit previously loaded into the tone register. Transmission of DTMF tones is initiated when the DTMF mode is selected and the transmit enable (CR0 bit D1) is changed from 0 to 1.

PIN DESCRIPTION

POWER

NAME	28-PIN	22-PIN	TYPE	DESCRIPTION
GND	28	1	I	System Ground.
VDD	15	11	I	Power supply input, 12V +10%, -20% (or 5V ±10%). Bypass with .1 and 22 µF capacitors to ground.
Vref	26	21	O	An internally generated reference voltage. Bypass with .1 µF capacitor to ground.
Iset	24	19	I	Chip current reference. Sets bias current for op-amps. The chip current is set by connecting this pin to VDD through a 2 MΩ resistor. Iset should be bypassed to GND with a .1 µF capacitor.

PARALLEL MICROPROCESSOR INTERFACE

ALE	12	-	I	Address latch enable. The falling edge of ALE latches the address on AD0-AD2 and the chip select on $\overline{CS}$.
AD0-AD7	4-11	-	I/O	Address/data bus. These bidirectional tri-state multiplexed lines carry information to and from the internal registers.
$\overline{CS}$	20	-	I	Chip select. A low on this pin allows a read cycle or a write cycle to occur. AD0-AD7 will not be driven and no registers will be written if $\overline{CS}$ (latched) is not active. $\overline{CS}$ is latched on the falling edge of ALE.
CLK	1	2	O	Output clock. This pin is selectable under processor control to be either the crystal frequency (for use as a processor clock) or 16 x the data rate for use as a baud rate clock in DPSK modes only. The pin defaults to the crystal frequency on reset.
$\overline{INT}$	17	13	O	Interrupt. This open drain output signal is used to inform the processor that a detect flag has occurred. The processor must then read the detect register to determine which detect triggered the interrupt. $\overline{INT}$ will stay active until the processor reads the detect register or does a full reset.
$\overline{RD}$	14	-	I	Read. A "low" requests a read of the SSI 73K221 internal registers. Data cannot be output unless both $\overline{RD}$ and the latched $\overline{CS}$ are active or "low."
RESET	25	20	I	Reset. An active signal "high" on this pin will put the chip into an inactive state. All control register bits (CR0, CR1, Tone) will be reset. The output of the CLK pin will be set to the crystal frequency. An internal pull down resistor permits power on reset using a capacitor to VDD.

PIN DESCRIPTION (Continued)

PARALLEL MICROPROCESSOR INTERFACE (Continued)

NAME	28-PIN	22-PIN	TYPE	DESCRIPTION
$\overline{WR}$	13	-	I	Write. A "low" on this informs the SSI 73K221 that data is available on AD0-AD7 for writing into an internal register. Data is latched on the rising edge of $\overline{WR}$. No data is written unless both $\overline{WR}$ and the latched $\overline{CS}$ are active ("low").

SERIAL MICROPROCESSOR INTERFACE

A0-A2	-	5-7	I	Register Address Selection. These lines carry register addresses and should be valid during any read or write operation.
DATA	-	8	I/O	Serial Control Data. Data for a read/write operation is clocked in or out on the falling edge of the EXCLK pin. The direction of data flow is controlled by the $\overline{RD}$ pin. $\overline{RD}$ low outputs data. $\overline{RD}$ high inputs data.
$\overline{RD}$	-	10	I	Read. A "low" on this input informs the SSI 73K221 that data or status information is being read by the processor. The falling edge of the $\overline{RD}$ signal will initiate a read from the addressed register. The $\overline{RD}$ signal must continue for eight falling edges of EXCLK in order to read all eight bits of the referenced register. Read data is provided LSB first. Data will not be output unless the $\overline{RD}$ signal is active.
$\overline{WR}$	-	9	I	Write. A "low" on this input informs the SSI 73K221 that data or status information has been shifted in through the DATA pin and is available for writing to an internal register. The normal procedure for a write is to shift in data LSB first on the DATA pin for eight consecutive falling edges of EXCLK and then to pulse $\overline{WR}$ low. Data is written on the rising edge of $\overline{WR}$.

Note: In the serial, 22-pin version, the pins AD0-AD7, ALE and $\overline{CS}$ are removed and replaced with the pins; A0, A1, A2, DATA, and an unconnected pin. Also, the $\overline{RD}$ and $\overline{WR}$ controls are used differently.

The serial control mode is provided in the 28-pin version by tying ALE high and $\overline{CS}$ low. In this configuration AD7 becomes DATA and AD0, AD1 and AD2 become A0, A1 and A2, respectively.

PIN DESCRIPTION (Continued)

RS-232 INTERFACE

NAME	28-PIN	22-PIN	TYPE	DESCRIPTION
EXCLK	19	15	I	External Clock. This signal is used in synchronous transmission when the external timing option has been selected. In the external timing mode the rising edge of EXCLK is used to strobe synchronous DPSK transmit data available on the TXD pin. Also used for serial control interface.
RXCLK	23	18	O	Receive Clock. The falling edge of this clock output is coincident with the transitions in the serial received data output. The rising edge of RXCLK can be used to latch the valid output data. RXCLK will be valid as long as a carrier is present.
RXD	22	17	O	Received Digital Data Output. Serial receive data is available on this pin. The data is always valid on the rising edge of RXCLK when in synchronous mode. RXD will output constant marks if no carrier is detected.
TXCLK	18	14	O	Transmit Clock. This signal is used in synchronous transmission to latch serial input data on the TXD pin. Data must be provided so that valid data is available on the rising edge of the TXCLK. The transmit clock is derived from different sources depending upon the synchronization mode selection. In Internal Mode the clock is generated internally. In External Mode TXCLK is phase locked to the EXCLK pin. In Slave Mode TXCLK is phase locked to the RXCLK pin. TXCLK is always active.
TXD	21	16	I	Transmit Digital Data Input. Serial data for transmission is input on this pin. In synchronous modes, the data must be valid on the rising edge of the TXCLK. In asynchronous modes (1200/600 bit/s or 300 baud) no clocking is necessary. DPSK data must be 1200/600 bit/s +1%, -2.5% or +2.3%, -2.5 % in overspeed mode.

ANALOG INTERFACE

RXA	27	22	I	Received modulated analog signal input from the phone line.
TXA	16	12	O	Transmit analog output to the phone line.
XTAL1 XTAL2	2 3	3 4	I I	These pins are for the internal crystal oscillator requiring an 11.0592 MHz parallel mode crystal. Load capacitors should be connected from XTAL1 and XTAL2 to Ground. XTAL2 can also be driven from an external clock.

REGISTER DESCRIPTIONS

Four 8-bit internal registers are accessible for control and status monitoring. The registers are accessed in read or write operations by addressing the A0 and A1 address lines in serial mode, or the AD0 and AD1 lines in parallel mode. The AD0 and AD1 lines are latched by ALE. Register CR0 controls the method by which data is transferred over the phone line. CR1 controls the interface between the microprocessor and the SSI 73K221 internal state. DR is a detect register which provides an indication of monitored modem status conditions. TR, the tone control register, controls the DTMF generator, answer and guard tones and RX output gate used in the modem initial connect sequence. All registers are read/write except for DR which is read only. Register control and status bits are identified below:

REGISTER BIT SUMMARY

	ADDRESS	DATA BIT NUMBER							
REGISTER	AD2 - AD0	D7	D6	D5	D4	D3	D2	D1	D0
CONTROL REGISTER 0 CR0	000	MODULATION OPTION		TRANSMIT MODE 3	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ANSWER/ ORIGINATE
CONTROL REGISTER 1 CR1	001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTERRUPT	BYPASS SCRAMBLER	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0
DETECT REGISTER DR	010			RECEIVE DATA	UNSCR. MARKS	CARRIER DETECT	ANSWER TONE	CALL PROGRESS	LONG LOOP
TONE CONTROL REGISTER TR	011	RXD OUTPUT CONTROL	TRANSMIT GUARD TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF3	DTMF2	DTMF1/ OVERSPEED	DTMF0/ GUARD/
CONTROL REGISTER 2 CR2	100				THESE REGISTER LOCATIONS ARE RESERVED FOR				
CONTROL REGISTER 3 CR3	101				USE WITH OTHER K-SERIES FAMILY MEMBERS				
ID REGISTER ID	110	0	1						

NOTE: When a register containing reserved control bits is written into, the reserved bits must be programmed as 0's.

REGISTER ADDRESS TABLE

REGISTER	ADDRESS AD2 - AD0	DATA BIT NUMBER D7	D6	D5	D4	D3	D2	D1	D0
CONTROL REGISTER 0 CR0	000	MODULATION OPTION		TRANSMIT MODE 3	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ORIGINATE/ ANSWER
		0=1200 BIT/S DPSK 1=600 BIT/S DPSK		0000=PWR DOWN 0001=INT SYNCH 0010=EXT SYNCH 0011=SLAVE SYNCH 0100=ASYNCH 8 BITS/CHAR 0101=ASYNCH 9 BITS/CHAR 0110=ASYNCH 10 BITS/CHAR 0111=ASYNCH 11 BITS/CHAR 1100=FSK				0=SQUELCH ANALOG 1=ENABLE ANALOG	0=ANSWER 1=ORIGINATE
CONTROL REGISTER 1 CR1	001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTERRUPT	BYPASS SCRAMBLER	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0
		00=TX DATA 01=TX ALTERNATE 10=TX MARK 11=TX SPACE		0=OFF 1=ON	0=NORMAL 1=BYPASS SCRAMBLER	0=XTAL 1=16 X DATA RATE OUTPUT AT CLK PIN IN DPSK MODE ONLY	0=NORMAL 1=RESET	00=NORMAL 01=ANALOG LOOPBACK 10=REMOTE DIGITAL LOOPBACK 11=LOCAL DIGITAL LOOPBACK	
DETECT REGISTER DR	010			RECEIVE DATA	UNSCR. MARKS	CARRIER DETECT	ANSWER TONE	CALL PROGRESS	LONG LOOP
				OUTPUTS RECEIVED DATA STREAM	0=CONDITION NOT DETECTED 1=CONDITION DETECTED				
TONE CONTROL REGISTER TR	011	RXD OUTPUT CONTROL	TRANSMIT GUARD/ TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF3	DTMF2	DTMF1/ OVERSPEED	DTMF0/ GUARD/ TONE
		RXD PIN 0=NORMAL 1=TRI STATE	0=OFF 1=ON	0=OFF 1=ON	0=DATA 1=TX DTMF	4 BIT CODE FOR 1 OF 16 DUAL TONE COMBINATIONS. OVERIDES OTHER TRANSMIT MODES			0=1800 Hz G.T. 1=550 Hz G.T.
ID REGISTER ID	110	ID BIT 1	ID BIT 0						
		00=73K212 or 73K322 01=73K221 or 73K302L 10=73K222 11=73K224							

CONTROL REGISTER 0

	D7	D6	D5	D4	D3	D2	D1	D0
CR0 000	MODUL. OPTION		TRANSMIT MODE 3	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ANSWER/ ORIGINATE

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	Answer/ Originate	0	Selects answer mode (transmit in high band, receive in low band).
		1	Selects originate mode (transmit in low band, receive in high band).
D1	Transmit Enable	0	Disables transmit output at TXA.
		1	Enables transmit output at TXA. Note: TX Enable must be set to 1 to activate Answer Tone and DTMF transmit.
D5, D4, D3, D2	Transmit Mode	D5 D4 D3 D2	
		0 0 0 0	Selects power down mode. All functions disabled except digital interface.
		0 0 0 1	Internal synchronous mode. In this mode TXCLK is an internally derived 1200 Hz signal. Serial input data appearing at TXD must be valid on the rising edge of TXCLK. Receive data is clocked out of RXD on the falling edge of RXCLK.
		0 0 1 0	External synchronous mode. Operation is identical to internal synchronous, but TXCLK is connected internally to EXCLK pin, and a 1200 Hz clock must be supplied externally.
		0 0 1 1	Slave synchronous mode. Same operation as other synchronous modes. TXCLK is connected internally to the RXCLK pin in this mode.
		0 1 0 0	Selects PSK asynchronous mode - 8 bits/character (1 start bit, 6 data bits, 1 stop bit).
		0 1 0 1	Selects PSK asynchronous mode - 9 bits/character (1 start bit, 7 data bits, 1 stop bit).
		0 1 1 0	Selects PSK asynchronous mode - 10 bits/character (1 start bit, 8 data bits, 1 stop bit).
		0 1 1 1	Selects PSK asynchronous mode - 11 bits/character (1 start bit, 8 data bits, Parity and/or 1 or 2 stop bits).
		1 1 0 0	Selects FSK operation.
D6		0	Not used; must be written as a "0."

CONTROL REGISTER 0 (Continued)

	D7	D6	D5	D4	D3	D2	D1	D0
CR0 000	MODUL. OPTION		TRANSMIT MODE 3	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ANSWER/ ORIGINATE

BIT NO.	NAME	CONDITION	DESCRIPTION
D7	Modulation Option	D7 D5 D4	Selects:
		0 0 X	PSK mode at 1200 bit/s.
		1 0 X	PSK mode at 600 bit/s. X = Don't care

CONTROL REGISTER 1

	D7	D6	D5	D4	D3	D2	D1	D0
CR1 001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTER.	BYPASS SCRAMB	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0

BIT NO.	NAME	CONDITION	DESCRIPTION
D1, D0	Test Mode	D1 D0	
		0 0	Selects normal operating mode.
		0 1	Analog loopback mode. Loops the transmitted analog signal back to the receiver, and causes the receiver to use the same center frequency as the transmitter. To squelch the TXA pin, transmit enable must be forced low.
		1 0	Selects remote digital loopback. Received data is looped back to transmit data internally, and RXD is forced to a mark. Data on TXD is ignored.
		1 1	Selects local digital loopback. Internall loops TXD back to RXD and continues to transmit data from TXA pin.
D2	Reset	0	Selects normal operation.
		1	Resets modem to power down state. All control register bits (CR0, CR1, Tone) are reset to zero. The output of the clock pin will be set to the crystal frequency.
D3	CLK Control (Clock Control)	0	Selects 11.0592 MHz crystal echo output at CLK pin.
		1	Selects 16 X the data rate, output at CLK pin in DPSK modes only.

CONTROL REGISTER 1 (Continued)

	D7	D6	D5	D4	D3	D2	D1	D0
CR1 001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTER.	BYPASS SCRAMB	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0

BIT NO.	NAME	CONDITION	DESCRIPTION
D4	Bypass Scrambler	0	Selects normal operation. DPSK data is passed through scrambler.
		1	Selects Scrambler Bypass. Bypass DPSK data is routed around scrambler in the transmit path.
D5	Enable Detect Interrupt	0	Disables interrupt at $\overline{INT}$ pin. All interrupts are normally disabled in power down modes.
		1	Enables $\overline{INT}$ output. An interrupts will be generated with a change in status of DR bits D1-D4. The answer tone and call progress detect interrupts are masked when the TX enable bit is set. Carrier detect is masked when TX DTMF is activated. All interrupts will be disabled if the device is in power down mode.
D7, D6	Transmit Pattern	D7 D6	
		0 0	Selects normal data transmission as controlled by the state of the TXD pin.
		0 1	Selects an alternating mark/space transmit pattern for modem testing.
		1 0	Selects a constant mark transmit pattern.
		1 1	Selects a constant space transmit pattern.

DETECT REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
DR 010			RECEIVE DATA	UNSCR. MARK	CARR. DETECT	ANSWER TONE	CALL PROG.	LONG LOOP

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	Long Loop	0	Indicates normal received signal.
		1	Indicates low received signal level.
D1	Call Progress Detect	0	No call progress tone detected.
		1	Indicates presence of call progress tones. The call progress detection circuitry is activated by energy in the 350 to 620 Hz call progress bandwidth.

DETECT REGISTER (Continued)

	D7	D6	D5	D4	D3	D2	D1	D0
DR 010			RECEIVE DATA	UNSCR. MARK	CARR. DETECT	ANSWER TONE	CALL PROG.	LONG LOOP

BIT NO.	NAME	CONDITION	DESCRIPTION
D2	Answer Tone Received	0	No answer tone detected.
		1	Indicates detection of 2100 Hz answer tone. The device must be in originate mode for detection of answer tone in normal operation.
D3	Carrier Detect	0	No carrier detected in the receive channel.
		1	Indicates carrier has been detected in the received channel.
D4	Unscr. Mark (Unscrambled Mark)	0	No unscrambled mark.
		1	Indicates detection of unscrambled marks in the received data. This may be used in the V.22 connect sequence or for requesting a remote modem to configure itself for remote digital loopback. A valid indication requires that unscrambled marks be received for > 165.5 ± 6.5 ms.
D5	Receive Data		Continuously outputs the received data stream. This data is the same as that output on the RXD pin, but it is not disabled when RXD is tri-stated.
D6, D7			Not used.

TONE REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
TR 011	RXD OUTPUT CONTR.	TRANSMIT GUARD TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF 3	DTMF 2	DTMF 1/ OVER-SPEED	DTMF 0/ GUARD

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	DTMF 0/ Guard Tone	D6 D4 D0	D0 interacts with bits D6, D5, and D4 as shown.
		X 1 X	Transmit DTMF tones.
		X 0 0	Transmits 1800 Hz guard tone.
		X 0 1	Transmits 550 Hz guard tone.
D1	DTMF 1/	D4 D1	D1 interacts with D4 as shown.
		0 0	Asynchronous PSK 1200 or 600 bit/s +1.0% - 2.5%
		0 1	Asynchronous PSK 1200 or 600 bit/s +2.3% -2.5%.

TONE REGISTER (Continued)

	D7	D6	D5	D4	D3	D2	D1	D0
TR 011	RXD OUTPUT CONTR.	TRANSMIT GUARD TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF 3	DTMF 2	DTMF 1/ OVER-SPEED	DTMF 0/ GUARD

BIT NO.	NAME	CONDITION	DESCRIPTION
D3, D2, D1, D0	DTMF 3, 2, 1, 0	D3 D2 D1 D0 0 0 0 0 - 1 1 1 1	Programs 1 of 16 DTMF tone pairs that will be transmitted when TX DTMF and TX enable bit (CR0, bit D1) is set. Tone encoding is shown below:

KEYBOARD EQUIVALENT	DTMF CODE D3	D2	D1	D0	TONES LOW	HIGH
1	0	0	0	1	697	1209
2	0	0	1	0	697	1336
3	0	0	1	1	697	1477
4	0	1	0	0	770	1209
5	0	1	0	1	770	1336
6	0	1	1	0	770	1477
7	0	1	1	1	852	1209
8	1	0	0	0	852	1336
9	1	0	0	1	852	1477
0	1	0	1	0	941	1336
*	1	0	1	1	941	1209
#	1	1	0	0	941	1477
A	1	1	0	1	697	1633
B	1	1	1	0	770	1633
C	1	1	1	1	852	1633
D	0	0	0	0	941	1633

D4	TX DTMF (Transmit DTMF)	0	Disabled DTMF.
		1	Activates DTMF. The selected DTMF tones are transmitted continuously when this bit is high. TX DTMF overrides all other transmit functions.
D5	TX ANS (Transmit Answer tone)	0	Disables answer tone generator.
		1	Enables answer tone generator. A 2100 Hz answer tone will be transmitted continuously when the Transmit Enable bit is set in CR0. The device must be in answer mode.

TONE REGISTER (Continued)

	D7	D6	D5	D4	D3	D2	D1	D0
TR 011	RXD OUTPUT CONTR.	TRANSMIT GUARD TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF 3	DTMF 2	DTMF 1/ OVER-SPEED	DTMF 0/ GUARD

BIT NO.	NAME	CONDITION	DESCRIPTION
D6	TX Guard (Transmit Guard Tone)	0	Disables guard tone generator.
		1	Enables guard tone generator (See D0 for selection of guard tones).
D7	RXD Output Control	0	Enables RXD pin. Receive data will be output on RXD.
		1	Disables RXD pin. The RXD pin reverts to a high impedance with internal weak pull-up resistor.

ID REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
ID 110	ID 1	ID 0						

BIT NO.	NAME	CONDITION	DESCRIPTION
D7, D6	Device Identification Signature	D7 D6	Indicates Device:
		0 0	SSI 73K212(L) or 73K322L
		0 1	SSI 73K221(L) or 73K302L
		1 0	SSI 73K222(L)
		1 1	SSI 73K224L

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
VDD Supply Voltage	14	V
Storage Temperature	-65 to 150	°C
Soldering Temperature (10 sec.)	260	°C
Applied Voltage	-0.3 to VDD+0.3	V

Note: All inputs and outputs are protected from static charge using built-in, industry standard protection devices and all outputs are short-circuit protected.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
VDD Supply Voltage					
5V Version (73K221L)		4.5	5	5.5	V
12V Version (73K221)		9.6	12	13.2	V
Digital Pins					
VIH, Input High Voltage					
Reset, XTAL1, XTAL2		3.0		VDD	V
All other inputs		2.0		VDD	V
VIL, Input Low Voltage		0		0.8	V
IOH, Output High Current		-0.4			mA
IOL, Output Low Current				1.6	mA
TA, Operating Free-Air Temperature		-40		+85	°C
External Component (Refer to Application section for placement.)					
VREF Bypass capacitor	(External to GND)	0.1			µF
Bias setting resistor	(Placed between VDD and ISET pins)	1.8	2	2.2	MΩ
ISET Bypass capacitor	(ISET pin to GND)	0.1			µF
VDD Bypass capacitor 1	(External to GND)	0.1			µF
VDD Bypass capacitor 2	(External to GND)	22			µF
Clock Variation	(11.0592 MHz) Crystal or external clock	-0.01		+0.01	%

ELECTRICAL SPECIFICATIONS

DC ELECTRICAL CHARACTERISTICS

(TA = -40°C to 85°C, VDD = recommended range unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
IDD, Supply Current	CLK = 11.0592 MHz				
5V Version (73K221L)	ISET Resistor = 2 MΩ				
IDDA, Active			6	9	mA
IDD1, Power-down	CLK = 11.0592 MHz			4	mA
IDD2, Power-down	CLK = 19.200 KHz			3	mA
12V Version (73K221)	CLK = 11.0592 MHz				
IDDA, Active	ISET Resistor = 2 MΩ		15	25	mA
IDD1, Power-down	CLK = 11.0592 MHz		6	12.5	mA
IDD2, Power-down	CLK = 19.200 KHz		5	12.5	mA
Digital Inputs					
IIH, Input High Current	VI = VIH MAX			100	µA
IIL, Input Low Current	VI = VIL MIN	-200			µA
Reset Pull-down Current	Reset = VDD	1		50	µA
Digital Outputs					
VOH, Output High Voltage					
5V Version (73K221L)	IO = IOH MIN	2.4		VDD	V
12V Version (73K221)	IO = IOH MIN	2.4			V
VOL, Output Low Voltage	IO = IOL MAX			0.4	V
VOL, CLK Output	IO = 3.6 mA			0.6	V
RXD Tri-State Pull-up Curr.	RXD = GND	-1		-50	µA
Capacitance					
Inputs	Capacitance, all Digital Input pins			10	pF
XTAL1, 2 Load Capacitors	Depends on crystal	15		60	pF
CLK	Maximum Capacitive Load			15	pF

ELECTRICAL SPECIFICATIONS (Continued)

DYNAMIC CHARACTERISTICS AND TIMING

(TA = -40°C to +85°C, VDD = recommended range unless otherwise noted.)

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNITS
PSK Modulator					
Carrier Suppression	Measured at TXA	55			dB
Output Amplitude	TX scrambled marks	-11	-10	-9	dBm0
FSK Mod/Demod					
Output Freq. Error	CLK = 11.0592 MHz	-0.35		+.35	%
Transmit Level	Transmit Dotting Pattern	-11	-10	-9	dBm0
Harmonic Distortion in 700-2900 Hz band	THD in the alternate band DPSK or FSK		-60	-50	dB
Output Bias Distortion	Transmit Dotting Pattern In ALB @ RXD		±8		%
Total Output Jitter	Random Input in ALB @ RXD	-15		+15	%
DTMF Generator					
Freq. Accuracy		-.25		+.25	%
Output Amplitude	Low Band, DPSK Mode	-10	-9	-8	dBm0
Output Amplitude	High Band, DPSK Mode	-8	-7	-6	dBm0
Twist	High-Band to Low-Band	1.0	2.0	3.0	dB
Long Loop Detect	DPSK or FSK	-38		-28	dBm0
Dynamic Range	Refer to Performance Curves		45		dB
Call Progress Detector					
Detect Level	2-Tones in 350-600 Hz band	-34		0	dBm0
Reject Level	2-Tones in 350-600 Hz band			-41	dBm0
Delay Time	-70 dBm0 to -30 dBm0 STEP	27		80	ms
Hold Time	-30 dBm0 to -70 dBm0 STEP	27		80	ms
Hysteresis		2			dB

Note: Parameters expressed in dBm0 refer to the following definition:

12V Version
- 10 dB loss in the Transmit path to the line.
- 9 dB gain in the Receive path from the line.

5V Version
- 0 dB loss in the Transmit path to the line.
- 2 dB gain in the Receive path from the line.

Refer to the Basic Box Modem diagram in the Applications section for the DAA design.

ELECTRICAL SPECIFICATIONS (Continued)

DYNAMIC CHARACTERISTICS AND TIMING (Continued)

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNITS
Carrier Detect					
Threshold	DPSK or FSK receive data	-49		-42	dBm0
Delay Time	-70 dBm0 to -30 dBm0 STEP	15		45	ms
Hysteresis	Single tone detected	2	3.0		dB
Hold Time	-30 dBm0 to -70 dBm0 STEP	10		24	ms
Answer Tone Detector					
Detect Level	In FSK mode	-49.5		-42	dBm0
Delay Time	-70 dBm0 to -30 dBm0 STEP	20		45	ms
Hold Time	-30 dBm0 to -70 dBm0 STEP	10		30	ms
Detect Freq. Range		-2.5		+2.5	%
Output Smoothing Filter					
Output load	TXA pin; FSK Single	10			KΩ
	Tone out for THD = -50 db in .3 to 3.4 KHz			50	pF
Spurious Freq. Comp.	Frequency = 76.8 KHz			-39	dBm0
	Frequency = 153.6 KHz			-45	dBm0
Output Impedance	TXA pin		200	300	Ω
Clock Noise	TXA pin; 76.8 KHz				
5V Version (73K221L)				1.0	mVrms
12V Version (73K221)				2	mVrms
Carrier VCO					
Capture Range	Originate or Answer	-10		+10	Hz
Capture Time	-10 Hz to +10 Hz Carrier Freq. Change Assum.		40	100	ms
Recovered Clock					
Capture Range	% of frequency center frequency (center at 1200 Hz)	-625		+625	ppm
Data Delay Time	Analog data in at RXA pin to receive data valid at RXD pin		30	50	ms

ELECTRICAL SPECIFICATIONS (Continued)

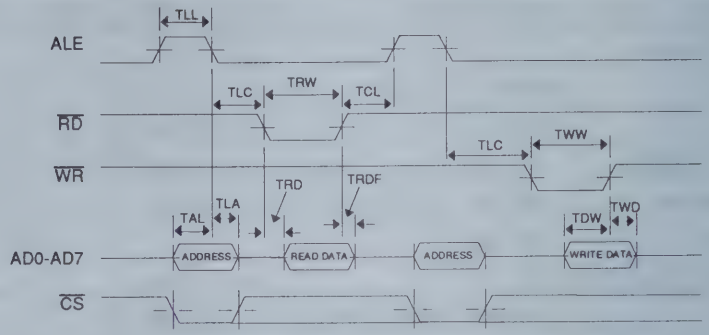
DYNAMIC CHARACTERISTICS AND TIMING (Continued)

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNITS
Guard Tone Generator					
Tone Accuracy	550 or 1800 Hz	-20		+20	Hz
Tone Level	550 Hz	-4.0	-3.0	-2.0	dB
(Below DPSK Output)	1800 Hz	-7.0	-6.0	-5.0	dB
Harmonic Distortion	550 Hz			-50	dB
700 to 2900 Hz	1800 Hz			-60	dB
Timing (Refer to Timing Diagrams)					
TAL	$\overline{CS}$/Addr. setup before ALE	30			ns
TLA	$\overline{CS}$/Addr. Hold after latch	20			ns
TLC	Latch to $\overline{RD}$/$\overline{WR}$ control	40			ns
TCL	$\overline{RD}$/$\overline{WR}$ Control to Latch	10			ns
TRD	Data out from $\overline{RD}$	0		160	ns
TLL	ALE width	60			ns
TRDF	Data float after READ	0		80	ns
TRW	READ width	200		25000	ns
TWW	WRITE width	140		25000	ns
TDW	Data setup before WRITE	150			ns
TWD	Data hold after WRITE	20			ns
TCKD	Data out after CLK			200	ns
TCKW	WRITE after CLK	150			ns
TDCK	Data setup before CLK	150			ns
TAC	Address setup before control [1]	50			ns
TCA	Address hold after control [1]	50			ns

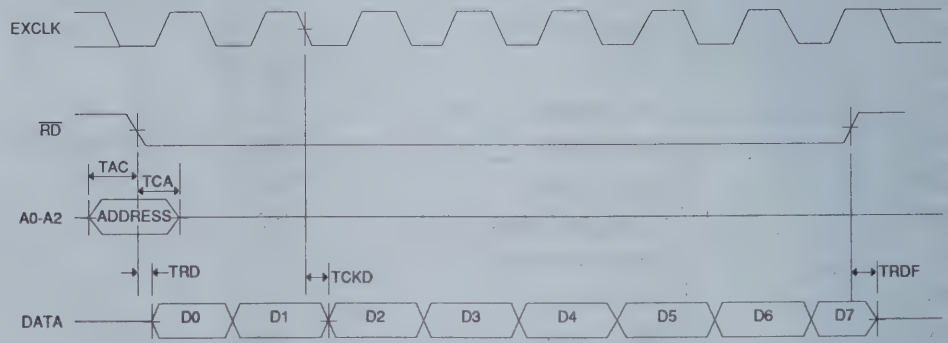
1: Control for setup is the falling edge of $\overline{RD}$ or $\overline{WR}$.
Control for hold is the falling edge of $\overline{RD}$ or the rising edge of $\overline{WR}$.

TIMING DIAGRAMS

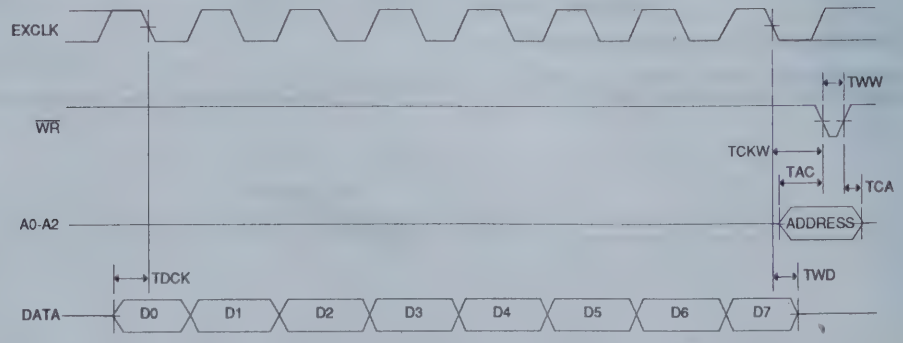
BUS TIMING DIAGRAM (PARALLEL VERSION)



READ TIMING DIAGRAM (SERIAL VERSION)



WRITE TIMING DIAGRAM (SERIAL VERSION)



APPLICATIONS INFORMATION

GENERAL CONSIDERATIONS

Figures 1 and 2 show the basic circuit diagram for K–Series modem integrated circuits. K-Series products are designed to be used in conjunction with a control processor, a UART or RS-232 serial data interface, and a DAA phone line interface to function as a typical intelligent modem. The K-Series ICs interface directly with Intel 8048 and 80C51 microprocessors for control and status monitoring purposes. Two typical DAA arrangements are shown: one for a split ±5 or ±12 volt design and one for a single 5 volt design. These diagrams are for reference only and do not represent production-ready modem designs.

K-Series devices are available in two control interface versions: one for a parallel multiplexed address/data interface, and one for a serial interface. The parallel version is intended for use with 8039/48 or 8031/51 microcontrollers from Intel or many other manufacturers. The serial interface 22-pin version can be used with other microcontrollers or in applications where only a limited number of port lines are available. The parallel versions may also be used in the serial mode, as explained in the data sheet pin description.

In most applications the controller will monitor the serial data for commands from the DTE and the received data for break signals from the far end modem. In this way, command data to the modem is sent over the same data line as the transmitted data. In other applications the RS-232 interface handshake lines are used for modem control.

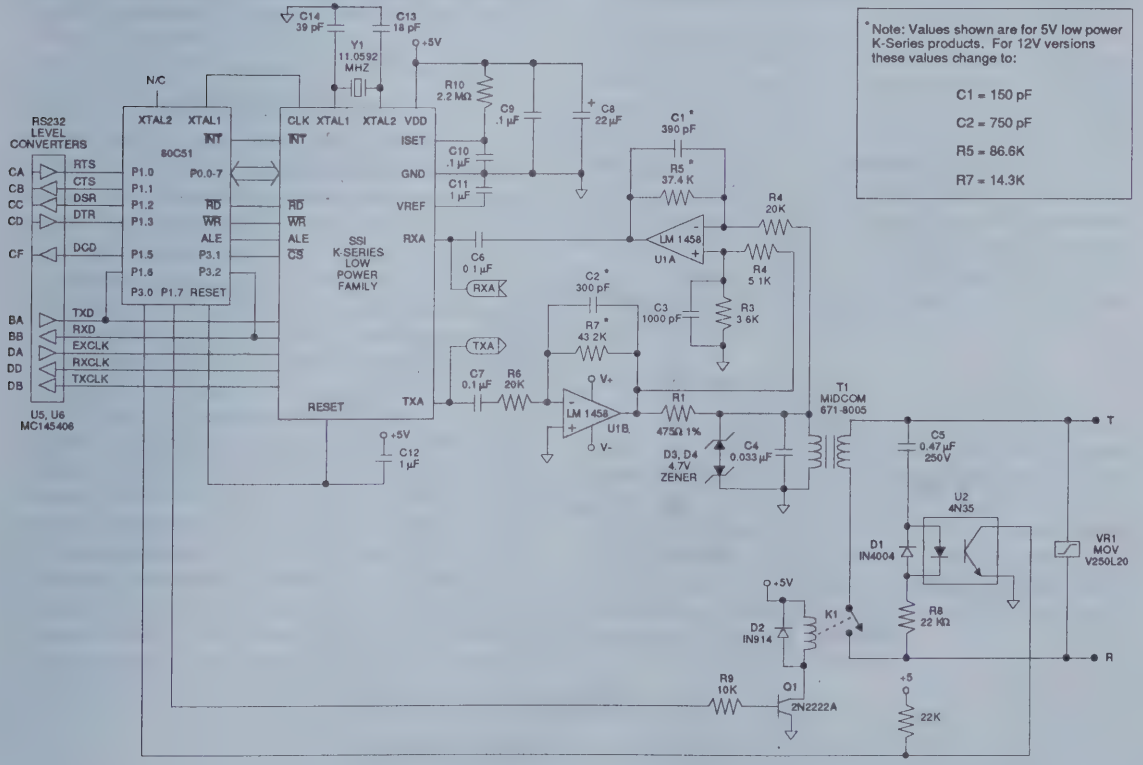


FIGURE 1: Basic Box Modem with Dual-Supply DAA

DIRECT ACCESS ARRANGEMENT (DAA)

The DAAs shown are two examples of how the "hybrid" may be implemented. The split supply design (Figure 1) is a typical two op-amp hybrid. The receive op-amp serves two purposes. It supplies gain to amplify the receive signal to the proper level for the modem's detectors and demodulator, and it removes the transmitted signal from the receive signal present at the transformer. This is done by supplying a portion of the transmitted signal to the non-inverting input of the receive op-amp at the same amplitude as the signal appearing at the transformer, making the transmit signal common mode.

The single-supply DAA is more complex than the dual-supply version described above, but its use eliminates the need for a second power supply. This DAA (Figure 2) uses a bridged drive to allow undistorted signals to be sent with a single 5 volt supply. Because DTMF tones utilize a higher amplitude than data, these signals will clip if a single-ended drive approach is used. The bridged driver uses an extra op-amp (U1A) to invert the signal coming from the gain setting op-amp (U1B) before sending it to the other leg of the transformer. Each op-amp then supplies half the drive signal to the transformer. The receive amplifier (op-amp C) picks off its signal at the junction of the impedance matching resistor and the transformer. Because the bottom leg of the transformer is being driven in one direction by U1A and the resistor is driven in the opposite direction at the same time by U1B, the summing point of the transformer and resistor remains relatively constant and the receive signal is unaffected.

DESIGN CONSIDERATIONS

Silicon Systems 1-chip modem products include all basic modem functions on a single IC, accessible from a standard bus interface. This makes these devices adaptable for use in a variety of applications, and as easy to control as conventional digital bus peripherals.

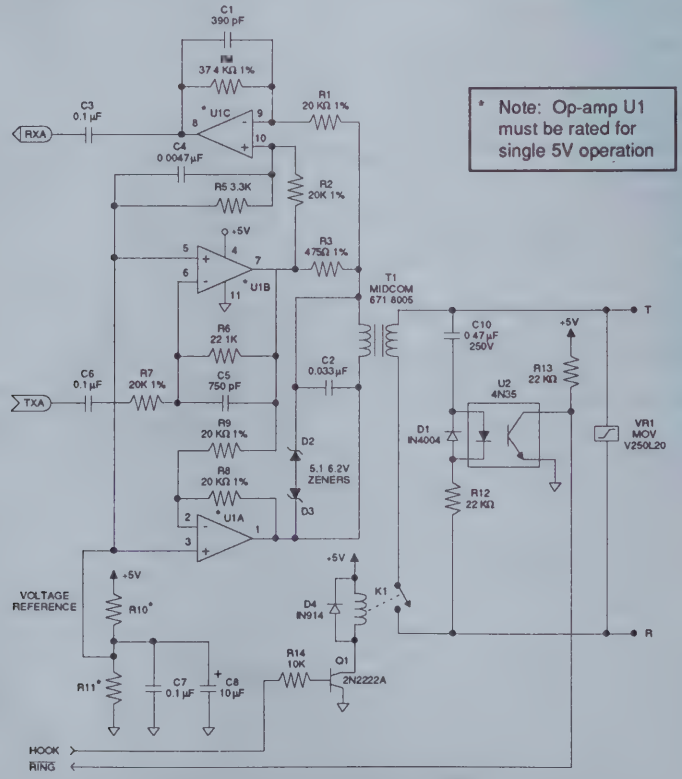


FIGURE 2: Single 5V DAA Version

Unlike digital logic circuitry, however, modem designs must properly contend with precise frequency tolerances, and very low level analog signals, to insure acceptable performance. Using good analog circuit design practices will generally result in a sound design. Folllowing are additional recommendations which should be taken into consideration when starting new designs.

CRYSTAL OSCILLATOR

The K-Series crystal oscillator requires a parallel mode (antiresonant) crystal which operates at 11.0592 MHz. It is important that this precise frequency be maintained to within ±.01% accuracy.

In order for a parallel mode crystal to operate correctly and to specification, it must have a load capacitor connected to the junction of each of the crystal and internal inverter connections, terminated to ground. The values of these capacitors depend primarily on the crystal's characteristics, and to a lesser degree on the internal inverter circuit. The values used affect the accuracy and start up characteristics of the oscillator.

LAYOUT CONSIDERATIONS

Good analog/digital design rules must be used to control system noise in order to obtain highest performance in modem designs. The more digital circuitry present on the PC board, the more this attention to noise control is needed. The modem should be treated as a high impedance analog device. A 22 µF electrolytic capacitor in parallel with a 0.1 µF ceramic capacitor between VDD and ground is recommended. Liberal use of ground planes and larger traces on power and ground are also highly favored. High speed digital circuits tend to generate a significant amount of EMI (Electro-Magnetic Interference) which must be minimized in order to meet regulatory agency limitations. To accomplish this, high speed digital devices should be locally bypassed, and the DAA and K-Series device should be located close to each other near the area of the board where the phone line connection is accessed. To avoid problems, power supply and ground traces should be routed separately to the analog and digital functions on the board, and digital signals should not be routed near low level or high impedance analog traces. The analog and digital grounds should only connect at one point near the analog supplies to avoid ground loops. The K–Series modem IC's should have both high frequency and low frequency bypassing as near to the package as possible.

MODEM PERFORMANCE CHARACTERISTICS

The curves presented here define modem IC performance under a variety of line conditions while inducing disturbances that are typical of those encountered during data transmission on public service telephone lines. Test data was taken using an AEA Electronics' "Autotest I" modem test set and line simulator, operating under computer control. All tests were run full-duplex, using a Concord Data Systems 224 as the reference modem. A 511 pseudo-random-bit pattern was used with $1X10^6$ bits transmitted for each data point. Noise was C-message weighted and all signal-to-noise (S/N) ratios reflect total power measurements similar to the CCITT V.56 measurement specification. The individual tests are defined as follows.

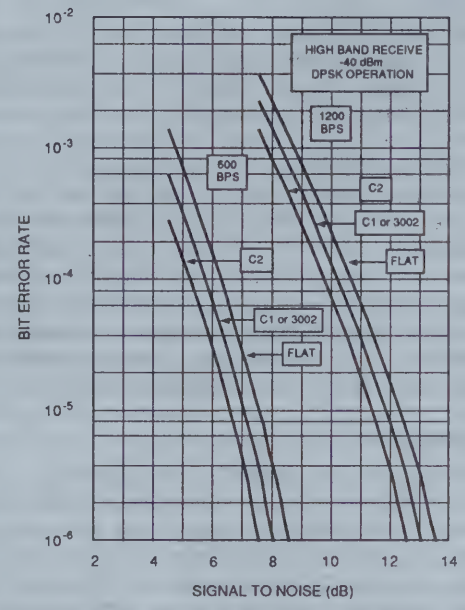
BER vs.S/N

This test measures the ability of the modem to operate over noisy lines with a minimum of data-transfer errors. Since some noise is generated in the best of dial-up lines, the modem must operate with the lowest S/N ratio possible. Optimum modem performance is indicated by test curves that are closest to the zero axis. A narrow spread between curves representing the four line parameters indicates minimal variation in performance while operating over a range of aberrant operating conditions. Typically, a PSK modem will exhibit better BER-performance test curves operating in the highband range than in the lowband.

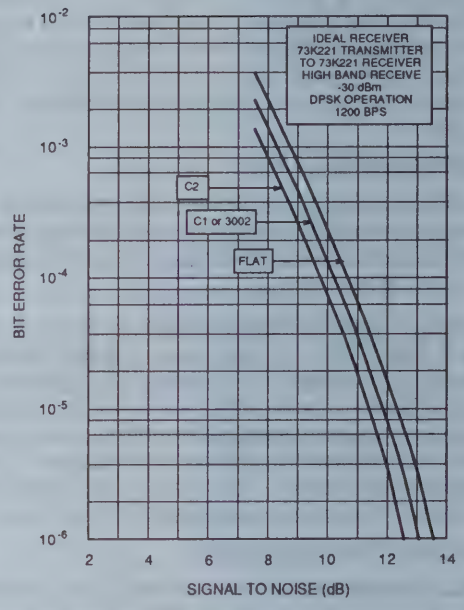
BER vs. Receive Level

This test measures the dynamic range of the modem. Because signal levels vary widely over dial-up lines, the widest possible dynamic range is desirable. The minimum Bell specification calls for 36 dB of dynamic range. S/N ratios are held constant at the indicated values while the receive level is lowered from a very high to very low signal levels. The width of the "bowl" of these curves, taken at the BER point, is the measure of dynamic range.

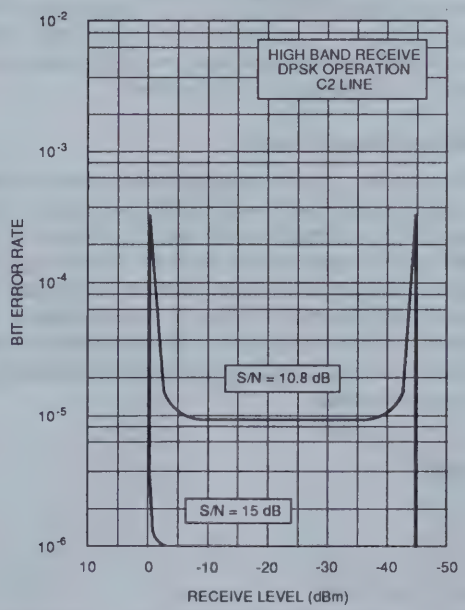
SSI 73K221, 73K221L
BER vs S/N



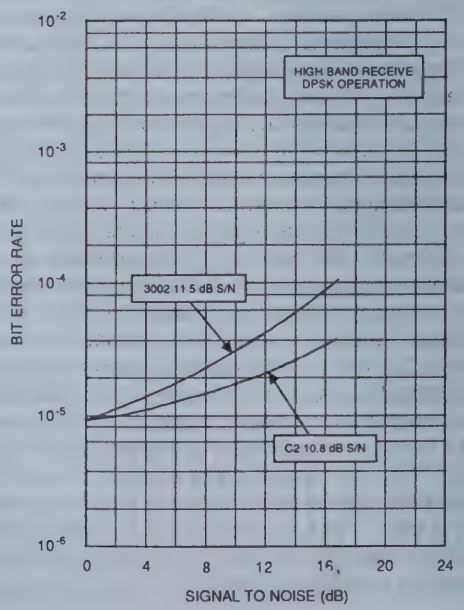
SSI 73K221, 73K221L
BER vs IDEAL RECEIVER

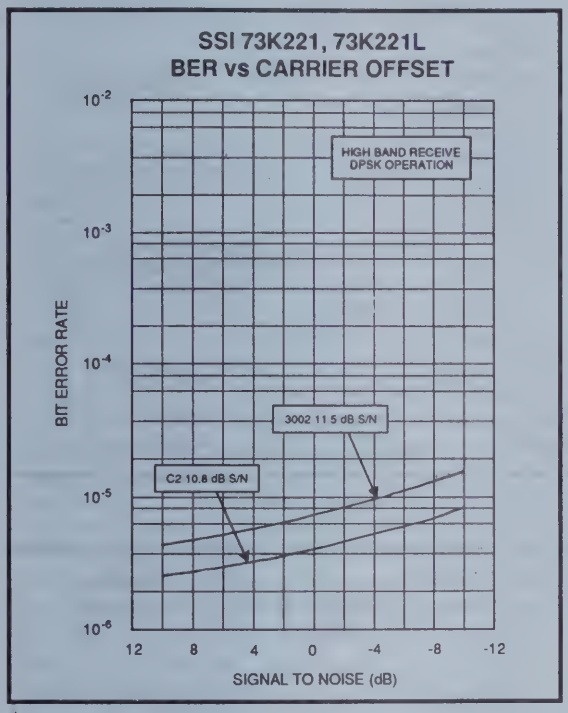


SSI 73K221, 73K221L
BER vs RECEIVE LEVEL



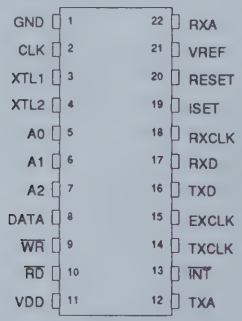
SSI 73K221, 73K221L
BER vs PHASE JITTER



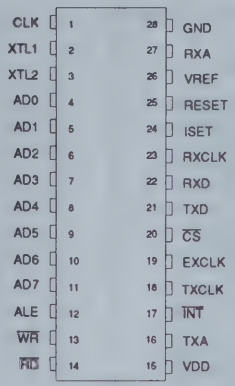

SSI 73K221, 73K221L
BER vs CARRIER OFFSET
HIGH BAND RECEIVE
DPSK OPERATION
3002 11.5 dB S/N
C2 10.8 dB S/N
BIT ERROR RATE
10-2
10-3
10-4
10-5
10-6
12
8
4
0
-4
-8
-12
SIGNAL TO NOISE (dB)

SSI 73K221/K221L
CCITT V.22, V.21
Single-Chip Modem

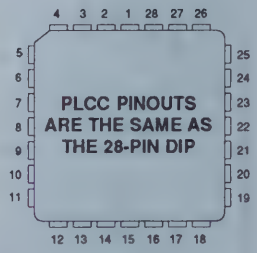
PACKAGE PIN DESIGNATIONS
(TOP VIEW)



400-Mil
22-Pin DIP



600-Mil
28-Pin DIP



28-Lead
PLCC

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 73K221 with Parallel Bus Interface		
28-Pin 12 Volt Supply		
Plastic Dual-In-Line	73K221 – IP	SSI 73K221 – IP
Plastic Leaded Chip Carrier	73K221 – IH	SSI 73K221 – IH
28-Pin 5 Volt Supply		
Plastic Dual-In-Line	73K221L – IP	SSI 73K221L – IP
Plastic Leaded Chip Carrier	73K221L – IH	SSI 73K221L – IH
SSI 73K221 with Serial Interface		
22-Pin 12 Volt Supply		
Plastic Dual-In-Line	73K221S – IP	SSI 73K221S – IP
22-Pin 5 Volt Supply		
Plastic Dual-In-Line	73K221SL – IP	SSI 73K221SL – IP

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SSI 73K222/K222L
V.22, V.21, Bell 212A Single-Chip Modem

July, 1989

1

DESCRIPTION

The SSI 73K222 is a highly integrated single-chip modem IC which provides the functions needed to construct a CCITT V.22, V.21 and Bell 212A compatible modem, capable of 1200 bit/s full–duplex operation over dial-up lines. The SSI 73K222 is an enhancement of the SSI 73K212 single-chip modem which adds V.22 and V.21 modes to the Bell 212A and 103 operation of the SSI 73K212. In Bell 212A mode, the SSI 73K222 provides the normal Bell 212A and 103 functions and employs a 2225 Hz answer tone. The SSI 73K222 in V.22 mode produces either 550 or 1800 Hz guard tone, recognizes and generates a 2100 Hz answer tone, and allows 600 bit/s V.22 or 0-300 bit/s V.21 fallback operation. The SSI 73K222 integrates analog, digital, and switched-capacitor array functions on a single substrate, offering excellent performance and a high level of functional integration in a single 28- or 22-pin DIP configuration. The SSI 73K222L, low power version of the SSI 73K222 provides identical performance and features, but operates from a single +5 volt supply with substantially lower power consumption.

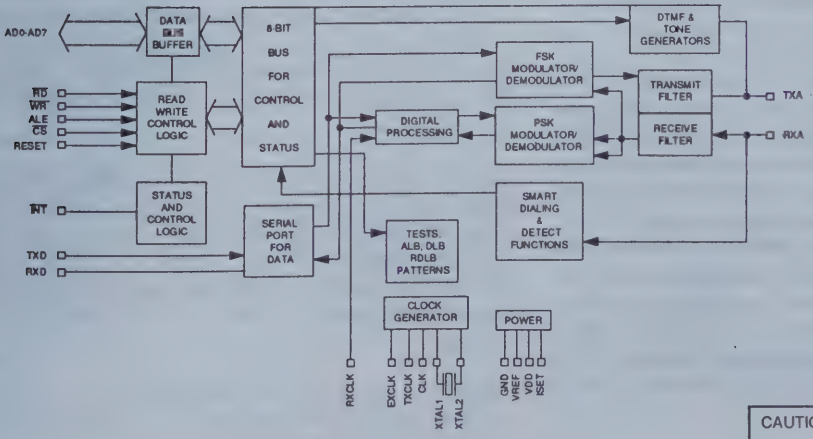
The SSI 73K222 includes the DPSK and FSK modulator/demodulator functions, call progress and handshake tone monitor and a tone generator capable of producing DTMF, answer and 550 or 1800 Hz guard

(Continued)

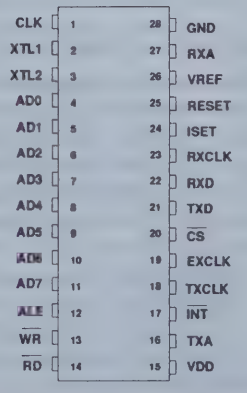
FEATURES

- One-chip CCITT V.22, V.21, Bell 212A and 103 standard compatible modem
- Full-duplex operation at 0-300 bit/s (FSK) or 600 and 1200 bit/s (DPSK)
- Pin and software compatible with other SSI K–Series 1-chip modems
- Interfaces directly with standard microprocessors (8048, 80C51 typical)
- Serial (22-pin DIP) or parallel (28-pin DIP) microprocessor bus for control
- Serial port for data transfer
- Both synchronous and asynchronous modes of operation including V.22 overspeed
- Call progress, carrier, precise answer tone (2100 or 2225 Hz), and long loop detectors
- DTMF, and 550 or 1800 Hz guard tone generators
- Test modes available: ALB, DL, RDL, Mark, Space, Alternating bit patterns
- Precise automatic gain control allows 45 dB dynamic range
- Space efficient 22- or 28-pin DIP packages
- CMOS technology for low power consumption using 30 mW @ 5V or 180 mW @ 12V
- Single +5 volt (73K222L) or +12 volt (73K222) versions

BLOCK DIAGRAM



PIN DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

DESCRIPTION (Continued)

tone required for European applications. This device supports V.22 (except mode v) and V. 21 modes of operation, allowing both synchronous and asynchronous communications. Test features such as analog loop, digital loop, and internal remote digital loopback are provided. Internal pattern generators are also included for self-testing. The SSI 73K222 is designed to appear to the systems designer as a microprocessor peripheral, and will easily interface with popular one–chip microprocessors (80C51 typical) for control of modem functions through its 8-bit multiplexed address/data bus or via an optional serial command bus. An ALE control line simplifies address demultiplexing. Data communications occurs through a separate serial port only.

OPERATION

The SSI 73K222 is ideal for use in either free standing or integral system modem products where full-duplex 1200 bit/s data communications over the 2-wire switched telephone network is desired. Its high functionality, low power consumption and efficient packaging simplify design requirements and increase system reliability. A complete modem requires only the addition of the phone line interface, a control microprocessor, and RS-232 level converter for a typical system. The SSI 73K222 is part of Silicon Systems' K-Series family of pin and function compatible single-chip modem products. These devices allow systems to be configured for higher speeds and Bell or CCITT operation with only a single component change.

ASYNCHRONOUS MODE

Data transmission for the DPSK mode requires that data ultimately be transmitted in a synchronous fashion, The SSI 73K222 includes ASYNC/SYNC and SYNC/ASYNC converters which delete or insert stop bits in order to transmit data at a regular rate. In asynchronous mode the serial data comes from the TXD pin into the ASYNC/SYNC rate converter. The ASYNC/SYNC rate converter accepts the data provided on the TXD pin which normally must be 1200 or 600 bit/s +1.0%, -2.5%. The rate converter will then insert or delete stop bits in order to output a signal which is 1200 or 600 bit/s ± .01% (± .01% is the crystal tolerance).

The serial data stream from the transmit buffer or the rate converter is passed through the data scrambler and onto the analog modulator. The data scrambler can be bypassed under processor control when unscrambled data must be transmitted. The ASYNC/SYNC rate converter and the data scrambler are bypassed in all FSK modes. If serial input data contains a break signal through one character (including start and stop bits) the break will be extended to at least 2 • N + 3 bits long (where N is the number of transmitted bits/character).

Serial data from the demodulator is passed normally first through the data descrambler and then through the SYNC/ASYNC rate converter. The SYNC/ASYNC convertor will reinsert any deleted stop bits and transmit output data at an intra-character rate (bit-to-bit timing) of no greater than 1219 bit/s. An incoming break signal (low through two characters) will be passed through without incorrectly inserting a stop bit.

The SYNC/ASYNC converter also has an overspeed mode which allows selection of an output overspeed range of either +1% or +2.3%. In the overspeed mode, some stop bits are output at 7/8 the normal width.

Similar to the transmit side, both the SYNC/ASYNC rate converter and the data descrambler are bypassed in the FSK modes.

SYNCHRONOUS MODE

The CCITT V.22 standard defines synchronous operation at 600 and 1200 bit/s. The Bell 212A standard defines synchronous operation only at 1200 bit/s. Operation is similar to that of the asynchronous mode except that data must be synchronized to a provided clock and no variation in data transfer rate is allowable. Serial input data appearing at TXD must be valid on the rising edge of TXCLK.

TXCLK is an internally derived signal in internal mode and is connected internally to the RXCLK pin in slave mode. Receive data at the RXD pin is clocked out on the falling edge of RXCLK. The ASYNCH/SYNCH converter is bypassed when synchronous mode is selected and data is transmitted out at the same rate as it is input.

DPSK MODULATOR/DEMODULATOR

The SSI 73K222 modulates a serial bit stream into di–bit pairs that are represented by four possible phase shifts as prescribed by the Bell 212A or V.22 standards. The baseband signal is then filtered to reduce intersymbol interference on the bandlimited 2-wire telephone line. Transmission occurs on either a 1200 Hz (originate mode) or 2400 Hz carrier (answer mode). Demodulation is the reverse of the modulation process, with the incoming analog signal eventually decoded into di-bits and converted back to a serial bit stream. The demodulator also recovers the clock which was encoded into the analog signal during modulation. Demodulation occurs using either a 1200 Hz carrier (answer mode or ALB originate mode) or a 2400 Hz carrier (originate mode or ALB answer mode). The SSI 73K222 uses a phase locked loop coherent demodulation technique that offers inherently better performance than typical DPSK demodulators used by other manufacturers.

FSK MODULATOR/DEMODULATOR

The FSK modulator produces a frequency modulated analog output signal using two discrete frequencies to represent the binary data. In Bell 103, the standard frequencies of 1270 and 1070 Hz (originate, mark and space) or 2225 and 2025 Hz (answer, mark and space) are used. V.21 mode uses 980 and 1180 Hz (originate, mark and space), or 1650 and 1850Hz (answer, mark and space). Demodulation involves detecting the received frequencies and decoding them into the appropriate binary value. The rate converter and scrambler/descrambler are bypassed in the 103 or V.21 modes.

PASSBAND FILTERS AND EQUALIZERS

A high and low band filter is included to shape the amplitude and phase response of the transmit and receive signals and provide compromise delay equalization and rejection of out-of-band signals in the receive channel. Amplitude and phase equalization are necessary to compensate for distortion of the transmission line and to reduce intersymbol interference in the bandlimited receive signal. The transmit signal filtering approximates a 75% square root of raised Cosine frequency response characteristic.

AGC

The automatic gain control maintains a signal level at the input to the demodulators which is constant to within 1 dB. It corrects quickly for increases in signal which would cause clipping and provides a total dynamic range of >45 dB.

PARALLEL BUS INTERFACE

Four 8-bit registers are provided for control, option select and status monitoring. These registers are addressed with the AD0, AD1, and AD2 multiplexed address lines (latched by ALE) and appear to a control microprocessor as four consecutive memory locations. Two control registers and the tone register are read/write memory. The status detect register is read only and cannot be modified except by modem response to monitored parameters.

SERIAL COMMAND INTERFACE

The serial command mode allows access to the SSI 73K222 control and status registers via a serial command port (22-pin version only). In this mode the A0, A1 and A2 lines provide register addresses for data passed through the data pin under control of the $\overline{RD}$ and $\overline{WR}$ lines. A read operation is initiated when the $\overline{RD}$ line is taken low. The next eight cycles of EXCLK will then transfer out eight bits of the selected address location LSB first. A write takes place by shifting in eight bits of data LSB first for eight consecutive cycles of EXCLK. $\overline{WR}$ is then pulsed low and data transferred into the selected register occurs on the rising edge of $\overline{WR}$.

SPECIAL DETECT CIRCUITRY

The special detect circuitry monitors the received analog signal to determine status or presence of carrier, call-progress tones, answer tone and weak received signal (long loop condition). An unscrambled mark request signal is also detected when the received data out of the DPSK demodulator before the descrambler has been high for 165.5 ms ± 6.5 ms. The appropriate status bit is set when one of these conditions changes and an interrupt is generated for all purposes except long loop. The interrupts are disabled (masked) when the enable interrupt bit is set to 0.

DTMF GENERATOR

The DTMF generator will output one of 16 standard dual-tones determined by a 4-bit binary value and TX DTMF mode bit previously loaded into the tone register. Dialing is initiated when the DTMF mode is selected and the transmit enable (CR0 bit D1) is changed from 0 to 1.

PIN DESCRIPTION

POWER

NAME	28-PIN	22-PIN	TYPE	DESCRIPTION
GND	28	1	I	System Ground.
VDD	15	11	I	Power supply input, 12V +10%, -20% (or 5V ±10%). Bypass with .1 and 22 µF capacitors to Ground.
Vref	26	21	O	An internally generated reference voltage. Bypass with .1 µF capacitor to ground.
Iset	24	19	I	Chip current reference. Sets bias current for op-amps. The chip current is set by connecting this pin to VDD through a 2 MΩ resistor. Iset should be bypassed to GND with a .1 µF capacitor.

PARALLEL MICROPROCESSOR INTERFACE

ALE	12	-	I	Address latch enable. The falling edge of ALE latches the address on AD0-AD2 and the chip select on $\overline{CS}$.
AD0-AD7	4-11	-	I/O	Address/data bus. These bidirectional tri-state multiplexed lines carry information to and from the internal registers.
$\overline{CS}$	20	-	I	Chip select. A low on this pin allows a read cycle or a write cycle to occur. AD0-AD7 will not be driven and no registers will be written if $\overline{CS}$ (latched) is not active. $\overline{CS}$ is latched on the falling edge of ALE.
CLK	1	2	O	Output clock. This pin is selectable under processor control to be either the crystal frequency (for use as a processor clock) or 16 x the data rate for use as a baud rate clock in DPSK modes only. The pin defaults to the crystal frequency on reset.
$\overline{INT}$	17	13	O	Interrupt. This open drain output signal is used to inform the processor that a detect flag has occurred. The processor must then read the detect register to determine which detect triggered the interrupt. $\overline{INT}$ will stay active until the processor reads the detect register or does a full reset.
$\overline{RD}$	14	-	I	Read. A "low" requests a read of the SSI 73K222 internal registers. Data cannot be output unless both $\overline{RD}$ and the latched $\overline{CS}$ are active or "low."
RESET	25	20	I	Reset. An active signal "high" on this pin will put the chip into an inactive state. All control register bits (CR0, CR1, Tone) will be reset. The output of the CLK pin will be set to the crystal frequency. An internal pull down resistor permits power on reset using a capacitor to VDD.

PIN DESCRIPTION (Continued)

PARALLEL MICROPROCESSOR INTERFACE (Continued)

NAME	28-PIN	22-PIN	TYPE	DESCRIPTION
$\overline{WR}$	13	-	I	Write. A "low" on this informs the SSI 73K222 that data is available on AD0-AD7 for writing into an internal register. Data is latched on the rising edge of $\overline{WR}$. No data is written unless both $\overline{WR}$ and the latched $\overline{CS}$ are active ("low").

SERIAL MICROPROCESSOR INTERFACE

A0-A2	-	5-7	I	Register Address Selection. These lines carry register addresses and should be valid during any read or write operation.
DATA	-	8	I/O	Serial Control Data. Data for a read/write operation is clocked in or out on the falling edge of the EXCLK pin. The direction of data flow is controlled by the $\overline{RD}$ pin. $\overline{RD}$ low outputs data. $\overline{RD}$ high inputs data.
$\overline{RD}$	-	10	I	Read. A "low" on this input informs the SSI 73K222 that data or status information is being read by the processor. The falling edge of the $\overline{RD}$ signal will initiate a read from the addressed register. The $\overline{RD}$ signal must continue for eight falling edges of EXCLK in order to read all eight bits of the referenced register. Read data is provided LSB first. Data will not be output unless the $\overline{RD}$ signal is active.
$\overline{WR}$	-	9	I	Write. A "low" on this input informs the SSI 73K222 that data or status information has been shifted in through the DATA pin and is available for writing to an internal register. The normal procedure for a write is to shift in data LSB first on the DATA pin for eight consecutive falling edges of EXCLK and then to pulse $\overline{WR}$ low. Data is written on the rising edge of $\overline{WR}$.

Note: In the serial, 22-pin version, the pins AD0-AD7, ALE and $\overline{CS}$ are removed and replaced with the pins; A0, A1, A2, DATA, and an unconnected pin. Also, the $\overline{RD}$ and $\overline{WR}$ controls are used differently.

The serial control mode is provided in the 28-pin version by tying ALE high and $\overline{CS}$ low. In this configuration AD7 becomes DATA and AD0, AD1 and AD2 become A0, A1 and A2, respectively.

PIN DESCRIPTION (Continued)

RS-232 INTERFACE

NAME	28-PIN	22-PIN	TYPE	DESCRIPTION
EXCLK	19	15	I	External Clock. This signal is used in synchronous transmission when the external timing option has been selected. In the external timing mode the rising edge of EXCLK is used to strobe synchronous DPSK transmit data available on the TXD pin. Also used for serial control interface.
RXCLK	23	18	O	Receive Clock. The falling edge of this clock output is coincident with the transitions in the serial received data output. The rising edge of RXCLK can be used to latch the valid output data. RXCLK will be valid as long as a carrier is present.
RXD	22	17	O	Received Digital Data Output. Serial receive data is available on this pin. The data is always valid on the rising edge of RXCLK when in synchronous mode. RXD will output constant marks if no carrier is detected.
TXCLK	18	14	O	Transmit Clock. This signal is used in synchronous transmission to latch serial input data on the TXD pin. Data must be provided so that valid data is available on the rising edge of the TXCLK. The transmit clock is derived from different sources depending upon the synchronization mode selection. In Internal Mode the clock is generated internally. In External Mode TXCLK is phase locked to the EXCLK pin. In Slave Mode TXCLK is phase locked to the RXCLK pin. TXCLK is always active.
TXD	21	16	I	Transmit Digital Data Input. Serial data for transmission is input on this pin. In synchronous modes, the data must be valid on the rising edge of the TXCLK clock. In asynchronous modes (1200/600 bit/s or 300 baud) no clocking is necessary. DPSK data must be 1200/600 bit/s +1%, -2.5% or +2.3%, -2.5 % in overspeed mode.

ANALOG INTERFACE

RXA	27	22	I	Received modulated analog signal input from the phone line.
TXA	16	12	O	Transmit analog output to the phone line.
XTAL1 XTAL2	2 3	3 4	I I	These pins are for the internal crystal oscillator requiring a 11.0592 MHz parallel mode crystal. Load capacitors should be connected from XTAL1 and XTAL2 to Ground. XTAL2 can also be driven from an external clock.

REGISTER DESCRIPTIONS

Four 8-bit internal registers are accessible for control and status monitoring. The registers are accessed in read or write operations by addressing the A0, A1 and A2 address lines in serial mode, or the AD0, AD1 and AD2 lines in parallel mode. The address lines are latched by ALE. Register CR0 controls the method by which data is transferred over the phone line. CR1 controls the interface between the microprocessor and the SSI 73K222 internal state. DR is a detect register which provides an indication of monitored modem status conditions. TR, the tone control register, controls the DTMF generator, answer and guard tones and RX output gate used in the modem initial connect sequence. All registers are read/write except for DR which is read only. Register control and status bits are identified below:

REGISTER BIT SUMMARY

	ADDRESS	DATA BIT NUMBER							
REGISTER	AD2 - AD0	D7	D6	D5	D4	D3	D2	D1	D0
CONTROL REGISTER 0 CR0	000	MODULATION OPTION		TRANSMIT MODE 3	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ANSWER/ ORIGINATE
CONTROL REGISTER 1 CR1	001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTERRUPT	BYPASS SCRAMBLER	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0
DETECT REGISTER DR	010			RECEIVE DATA	UNSCR. MARKS	CARRIER DETECT	ANSWER TONE	CALL PROGRESS	LONG LOOP
TONE CONTROL REGISTER TR	011	RXD OUTPUT CONTROL	TRANSMIT GUARD TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF3	DTMF2	DTMF1/ OVERSPEED	DTMF0/ GUARD/ ANS TONE
CONTROL REGISTER 2 CR2	100				THESE REGISTER LOCATIONS ARE RESERVED FOR				
CONTROL REGISTER 3 CR3	101				USE WITH OTHER K-SERIES FAMILY MEMBERS				
ID REGISTER ID	110	1	0						

NOTE: When a register containing reserved control bits is written into, the reserved bits must be programmed as 0's.

REGISTER ADDRESS TABLE

REGISTER	ADDRESS AD2 - AD0	DATA BIT NUMBER D7	D6	D5	D4	D3	D2	D1	D0
CONTROL REGISTER 0 CR0	000	MODULATION OPTION		TRANSMIT MODE 3	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ORIGINATE/ ANSWER
		0=1200 BIT/S DPSK 1=600 BIT/S DPSK 0=BELL 103 FSK 1=V.21 FSK		0000=PWR DOWN 0001=INT SYNCH 0010=EXT SYNCH 0011=SLAVE SYNCH 0100=ASYNCH 8 BITS/CHAR 0101=ASYNCH 9 BITS/CHAR 0110=ASYNCH 10 BITS/CHAR 0111=ASYNCH 11 BITS/CHAR 1100=FSK				0=SQUELCH ANALOG 1=ENABLE ANALOG	0=ANSWER 1=ORIGINATE
CONTROL REGISTER 1 CR1	001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTERRUPT	BYPASS SCRAMBLER	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0
		00=TX DATA 01=TX ALTERNATE 10=TX MARK 11=TX SPACE		0=OFF 1=ON	0=NORMAL 1=BYPASS SCRAMBLER	0=XTAL 1=16 X DATA RATE OUTPUT AT CLK PIN IN DPSK MODE ONLY	0=NORMAL 1=RESET	00=NORMAL 01=ANALOG LOOPBACK 10=REMOTE DIGITAL LOOPBACK 11=LOCAL DIGITAL LOOPBACK	
DETECT REGISTER DR	010			RECEIVE DATA	UNSCR. MARKS	CARRIER DETECT	ANSWER TONE	CALL PROGRESS	LONG LOOP
				OUTPUTS RECEIVED DATA STREAM	0=CONDITION NOT DETECTED 1=CONDITION DETECTED				
TONE CONTROL REGISTER TR	011	RXD OUTPUT CONTROL	TRANSMIT GUARD/ TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF3	DTMF2	DTMF1/ OVERSPEED	DTMF0/ GUARD/ ANSWER/ TONE
		RXD PIN 0=NORMAL 1=TRI STATE	0=OFF 1=ON	0=OFF 1=ON	0=DATA 1=TX DTMF	4 BIT CODE FOR 1 OF 16 DUAL TONE COMBINATIONS. OVERIDES OTHER TRANSMIT MODES			0=2225 Hz A.T. 1800 Hz G.T. 1=2100 Hz A.T. 500 Hz G.T.
ID REGISTER ID	110	ID BIT 1	ID BIT 0						
		00=73K212(L) or 73K322L 01=73K221(L) or 73K302L 10=73K222(L) 11=73K224(L)							

CONTROL REGISTER 0

	D7	D6	D5	D4	D3	D2	D1	D0
CR0 000	MODUL. OPTION		TRANSMIT MODE 3	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ANSWER/ ORIGINATE

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	Answer/ Originate	0	Selects answer mode (transmit in high band, receive in low band).
		1	Selects originate mode (transmit in low band, receive in high band).
D1	Transmit Enable	0	Disables transmit output at TXA.
		1	Enables transmit output at TXA. Note: TX Enable must be set to 1 to activate Answer Tone and DTMF Transmit.
D5, D4, D3, D2	Transmit Mode	D5 D4 D3 D2	
		0 0 0 0	Selects power down mode. All functions disabled except digital interface.
		0 0 0 1	Internal synchronous mode. In this mode TXCLK is an internally derived 1200 Hz signal. Serial input data appearing at TXD must be valid on the rising edge of TXCLK. Receive data is clocked out of RXD on the falling edge of RXCLK.
		0 0 1 0	External synchronous mode. Operation is identical to internal synchronous, but TXCLK is connected internally to EXCLK pin, and a 1200 Hz clock must be supplied externally.
		0 0 1 1	Slave synchronous mode. Same operation as other synchronous modes. TXCLK is connected internally to the RXCLK pin in this mode.
		0 1 0 0	Selects PSK asynchronous mode - 8 bits/character (1 start bit, 6 data bits, 1 stop bit).
		0 1 0 1	Selects PSK asynchronous mode - 9 bits/character (1 start bit, 7 data bits, 1 stop bit).
		0 1 1 0	Selects PSK asynchronous mode - 10 bits/character (1 start bit, 8 data bits, 1 stop bit).
		0 1 1 1	Selects PSK asynchronous mode - 11 bits/character (1 start bit, 8 data bits, Parity and/or 1 or 2 stop bits).
		1 1 0 0	Selects FSK operation.
D6		0	Not used; must be written as a "0."

CONTROL REGISTER 0 (Continued)

	D7	D6	D5	D4	D3	D2	D1	D0
CR0 000	MODUL. OPTION		TRANSMIT MODE 3	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ANSWER/ ORIGINATE

BIT NO.	NAME	CONDITION	DESCRIPTION
D7	Modulation Option	D7 D5 D4	Selects:
		0 0 X	PSK mode at 1200 bit/s.
		1 0 X	PSK mode at 600 bit/s.
		0 1 1	FSK Bell 103 mode.
		1 1 1	FSK CCITT V.21 mode.
			X = Don't care

CONTROL REGISTER 1

	D7	D6	D5	D4	D3	D2	D1	D0
CR1 001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTER.	BYPASS SCRAMB	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0

BIT NO.	NAME	CONDITION	DESCRIPTION
D1, D0	Test Mode	D1 D0	
		0 0	Selects normal operating mode.
		0 1	Analog loopback mode. Loops the transmitted analog signal back to the receiver, and causes the receiver to use the same center frequency as the transmitter. To squelch the TXA pin, transmit enable must be forced low.
		1 0	Selects remote digital loopback. Received data is looped back to transmit data internally, and RXD is forced to a mark. Data on TXD is ignored.
		1 1	Selects local digital loopback. Internally loops TXD back to RXD and continues to transmit data from TXA pin.
D2	Reset	0	Selects normal operation.
		1	Resets modem to power down state. All control register bits (CR0, CR1, Tone) are reset to zero. The output of the clock pin will be set to the crystal frequency.
D3	CLK Control (Clock Control)	0	Selects 11.0592 MHz crystal echo output at CLK pin.
		1	Selects 16 X the data rate, output at CLK pin in DPSK modes only.

CONTROL REGISTER 1 (Continued)

	D7	D6	D5	D4	D3	D2	D1	D0
CR1 001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTER.	BYPASS SCRAMB	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0

BIT NO.	NAME	CONDITION	DESCRIPTION
D4	Bypass Scrambler	0	Selects normal operation. DPSK data is passed through scrambler.
		1	Selects Scrambler Bypass. Bypass DPSK data is routed around scrambler in the transmit path.
D5	Enable Detect Interrupt	0	Disables interrupt at $\overline{INT}$ pin. All interrupts are normally disabled in power down modes.
		1	Enables $\overline{INT}$ output. An interrupts will be generated with a change in status of DR bits D1-D4. The answer tone and call progress detect interrupts are masked when the TX enable bit is set. Carrier detect is masked when TX DTMF is activated. All interrupts will be disabled if the device is in power down mode.
D7, D6	Transmit Pattern	D7 D6	
		0 0	Selects normal data transmission as controlled by the state of the TXD pin.
		0 1	Selects an alternating mark/space transmit pattern for modem testing.
		1 0	Selects a constant mark transmit pattern.
		1 1	Selects a constant space transmit pattern.

DETECT REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
DR 010			RECEIVE DATA	UNSCR. MARK	CARR. DETECT	ANSWER TONE	CALL PROG.	LONG LOOP

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	Long Loop	0	Indicates normal received signal.
		1	Indicates low received signal level.
D1	Call Progress Detect	0	No call progress tone detected.
		1	Indicates presence of call progress tones. The call progress detection circuitry is activated by energy in the 350 to 620 Hz call progress bandwidth.

DETECT REGISTER (Continued)

	D7	D6	D5	D4	D3	D2	D1	D0
DR 010			RECEIVE DATA	UNSCR. MARK	CARR. DETECT	ANSWER TONE	CALL PROG.	LONG LOOP

BIT NO.	NAME	CONDITION	DESCRIPTION
D2	Answer Tone Received	0	No answer tone detected.
		1	Indicates detection of 2225 Hz answer tone in Bell mode or 2100 Hz in CCITT mode. The device must be in originate mode for detection of answer tone in normal operation. For V.22 answer tone detection, bit D0 of the Tone Register must be set to a 1.
D3	Carrier Detect	0	No carrier detected in the receive channel.
		1	Indicates carrier has been detected in the received channel.
D4	Unscr. Mark (Unscrambled Mark)	0	No unscrambled mark.
		1	Indicates detection of unscrambled marks in the received data. A valid indication requires that unscrambled marks be received for > 165.5 ± 6.5 ms.
D5	Receive Data		Continuously outputs the received data stream. This data is the same as that output on the RXD pin, but it is not disabled when RXD is tri-stated.
D6, D7			Not used.

TONE REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
TR 011	RXD OUTPUT CONTR.	TRANSMIT GUARD TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF 3	DTMF 2	DTMF 1/ OVER-SPEED	DTMF 0/ ANSWER/ GUARD

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	DTMF 0/ Answer/ Guard Tone	D6 D5 D4 D0	D0 interacts with bits D6, D5, and D4 as shown.
		X X 1 X	Transmit DTMF tones.
		X 1 0 0	Transmits and detects 2225 Hz answer tone (Bell).
		X 1 0 1	Transmits and detects 2100 Hz answer tone (CCITT).
		1 0 0 0	Select 1800 Hz guard tone.
		1 0 0 1	Select 550 Hz guard tone.
D1	DTMF 1/ Overspeed	D4 D1	D1 interacts with D4 as shown.
		0 0	Asynchronous DPSK +1.0% -2.5%.
		0 1	Asynchronous DPSK +2.3% -2.5%.

TONE REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
TR 011	RXD OUTPUT CONTR.	TRANSMIT GUARD TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF 3	DTMF 2	DTMF 1/ OVER-SPEED	DTMF 0/ ANSWER/ GUARD

BIT NO.	NAME	CONDITION	DESCRIPTION
D3, D2, D1, D0	DTMF 3, 2, 1, 0	D3 D2 D1 D0 0 0 0 0 - 1 1 1 1	Programs 1 of 16 DTMF tone pairs that will be transmitted when TX DTMF and TX enable bit (CR0, bit D1) is set. Tone encoding is shown below:

KEYBOARD EQUIVALENT	DTMF CODE D3 D2 D1 D0	TONES LOW HIGH
1	0 0 0 1	697 1209
2	0 0 1 0	697 1336
3	0 0 1 1	697 1477
4	0 1 0 0	770 1209
5	0 1 0 1	770 1336
6	0 1 1 0	770 1477
7	0 1 1 1	852 1209
8	1 0 0 0	852 1336
9	1 0 0 1	852 1477
0	1 0 1 0	941 1336
*	1 0 1 1	941 1209
#	1 1 0 0	941 1477
A	1 1 0 1	697 1633
B	1 1 1 0	770 1633
C	1 1 1 1	852 1633
D	0 0 0 0	941 1633

D4	TX DTMF (Transmit DTMF)	0	Disabled DTMF.
		1	Activates DTMF. The selected DTMF tones are transmitted continuously when this bit is high. TX DTMF overrides all other transmit functions.
D5	TX ANS (Transmit Answer tone)	D5 D4 D0	D5 interacts with bits D4 and D0 as shown.
		0 0 X	Disables answer tone generator.
		1 0 0	Enables answer tone generator. A 2225 Hz answer tone will be transmitted continuously when the Transmit Enable bit is set in CR0. The device must be in answer mode.
		1 0 1	Likewise a 2100 Hz answer tone will be transmitted.

TONE REGISTER (Continued)

	D7	D6	D5	D4	D3	D2	D1	D0
TR 011	RXD OUTPUT CONTR.	TRANSMIT GUARD TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF 3	DTMF 2	DTMF 1/ OVER-SPEED	DTMF 0/ ANSWER/ GUARD

BIT NO.	NAME	CONDITION	DESCRIPTION
D6	TX Guard (Transmit Guard Tone)	0	Disables guard tone generator.
		1	Enables guard tone generator (See D0 for selection of guard tones).
D7	RXD Output Control	0	Enables RXD pin. Receive data will be output on RXD.
		1	Disables RXD pin. The RXD pin reverts to a high impedance with internal weak pull-up resistor.

ID REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
ID 110	ID 1	ID 0						

BIT NO.	NAME	CONDITION	DESCRIPTION
D7, D6	Device Identification Signature	D7 D6	Indicates Device:
		0 0	SSI 73K212(L) or 73K322L
		0 1	SSI 73K221(L) or 73K302L
		1 0	SSI 73K222(L)
		1 1	SSI 73K224L

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
VDD Supply Voltage	14	V
Storage Temperature	-65 to 150	°C
Soldering Temperature (10 sec.)	260	°C
Applied Voltage	-0.3 to VDD+0.3	V

Note: All inputs and outputs are protected from static charge using built-in, industry standard protection devices and all outputs are short-circuit protected.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
VDD Supply Voltage					
5V Version (73K222L)		4.5	5	5.5	V
12V Version (73K222)		9.6	12	13.2	V
Digital Pins					
VIH, Input High Voltage					
Reset, XTAL1, XTAL2		3.0		VDD	V
All other inputs		2.0		VDD	V
VIL, Input Low Voltage		0		0.8	V
IOH, Output High Current		-0.4			mA
IOL, Output Low Current				1.6	mA
TA, Operating Free-Air Temperature		-40		+85	°C
External Component (Refer to Application section for placement.)					
VREF Bypass capacitor	(VREF to GND)	0.1			µF
Bias setting resistor	(Placed between VDD and ISET pins)	1.8	2	2.2	MΩ
ISET Bypass capacitor	(ISET pin to GND)	0.1			µF
VDD Bypass capacitor 1	(VDD to GND)	0.1			µF
VDD Bypass capacitor 2	(VDD to GND)	22			µF
Clock Variation	(11.0592 MHz) Crystal or external clock	-0.01		+0.01	%

ELECTRICAL SPECIFICATIONS (Continued)

DC ELECTRICAL CHARACTERISTICS

(TA = -40°C to 85°C, VDD = recommended range unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
IDD, Supply Current	CLK = 11.0592 MHz				
5V Version (73K222L)	ISET Resistor = 2 MΩ				
IDDA, Active			6	9	mA
IDD1, Power-down	CLK = 11.0592 MHz			4	mA
IDD2, Power-down	CLK = 19.200 KHz			3	mA
12V Version (73K222)	CLK = 11.0592 MHz				
IDDA, Active	ISET Resistor = 2 MΩ		15	25	mA
IDD1, Power-down	CLK = 11.0592 MHz		6	12.5	mA
IDD2, Power-down	CLK = 19.200 KHz		5	12.5	mA
Digital Inputs					
IIH, Input High Current	VI = VIH Max			100	µA
IIL, Input Low Current	VI = VIL Min	-200			µA
Reset Pull-down Current	Reset = VDD	1		50	µA
Digital Outputs					
VOH, Output High Voltage					
5V Version (73K222L)	IOUT = -0.4 mA	2.4		VDD	V
12V Version (73K222)	IOUT = -0.4 mA	2.4			V
VOL, Output Low Voltage	IOUT = 1.6 mA			0.4	V
VOL, CLK Output	IO = 3.6 mA			0.6	V
RXD Tri-State Pull-Up Curr.	RXD = GND	-1		-50	µA
Capacitance					
Inputs	Capacitance, all Digital Input pins			10	pF
XTAL1, 2 Load Capacitors	Depends on crystal	15		60	pF
CLK	Maximum Capacitive Load			15	pF

ELECTRICAL SPECIFICATIONS (Continued)

DYNAMIC CHARACTERISTICS AND TIMING

(TA = -40°C to +85°C, VDD = recommended range unless otherwise noted.)

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNITS
PSK Modulator					
Carrier Suppression	Measured at TXA	55			dB
Output Amplitude	TX scrambled marks	-11	-10.0	-9	dBm0
FSK Mod/Demod					
Output Freq. Error	CLK = 11.0592 MHz	-0.35		+.35	%
Transmit Level	Transmit Dotting Pattern	-11	-10.0	-9	dBm0
Harmonic Distortion in 700-2900 Hz band	THD in the alternate band DPSK or FSK		-60	-50	dB
Output Bias Distortion	Transmit Dotting Pattern in ALB @ RXD		±8		%
Total Output Jitter	Random Input in ALB @ RXD	-15		+15	%
DTMF Generator					
Freq. Accuracy		-.25		+.25	%
Output Amplitude	Low Band, DPSK Mode	-10	-9	-8	dBm0
Output Amplitude	High Band, DPSK Mode	-8	-7	-6	dBm0
Twist	High-Band to Low-Band	1.0	2.0	3.0	dB
Long Loop Detect	DPSK or FSK	-38		-28	dBm0
Dynamic Range	Refer to Performance Curves		45		dB
Call Progress Detector					
Detect Level	2-Tones in 350-600 Hz band	-34		0	dBm0
Reject Level	2-Tones in 350-600 Hz band			-41	dBm0
Delay Time	-70 dBm0 to -30 dBm0 STEP	27		80	ms
Hold Time	-30 dBm0 to -70 dBm0 STEP	27		80	ms
Hysteresis		2			dB

Note: Parameters expressed in dBm0 refer to the following definition:

12V Version
- 10 dB loss in the Transmit path to the line.
- 9 dB gain in the Receive path from the line.

5V Version
- 0 dB loss in the Transmit path to the line.
- 2 dB gain in the Receive path from the line.

Refer to the Basic Box Modem diagram in the Applications section for the DAA design.

ELECTRICAL SPECIFICATIONS (Continued)

DYNAMIC CHARACTERISTICS AND TIMING (Continued)

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNITS
Carrier Detect	DPSK or FSK				
Threshold	receive data	-49		-42	dBm0
Delay Time	-70 dBm0 to -30 dBm0 STEP	15		45	ms
Hysteresis	Single tone detected	2	3.0		dB
Hold Time	-30 dBm0 to -70 dBm0 STEP	10		24	ms
Answer Tone Detector					
Detect Level	In FSK mode	-49.5		-42	dBm0
Delay Time	-70 dBm0 to -30 dBm0 STEP	20		45	ms
Hold Time	-30 dBm0 to -70 dBm0 STEP	10		30	ms
Detect Freq. Range		-2.5		+2.5	%
Output Smoothing Filter					
Output load	TXA pin; FSK Single	10			KΩ
	Tone out for THD = -50 db in .3 to 3.4 KHz			50	pF
Spurious Freq. Comp.	Frequency = 76.8 KHz			-39	dBm0
	Frequency = 153.6 KHz			-45	dBm0
Output Impedance	TXA pin		200	300	Ω
Clock Noise	TXA pin; 76.8 KHz				
5V Version (73K222L)				1.0	mVrms
12V Version (73K222)				2	mVrms
Carrier VCO					
Capture Range	Originate or Answer	-10		+10	Hz
Capture Time	-10 Hz to +10 Hz Carrier Freq. Change Assum.		40	100	ms
Recovered Clock					
Capture Range	% of frequency center frequency (center at 1200 Hz)	-625		+625	ppm
Data Delay Time	Analog data in at RXA pin to receive data valid at RXD pin		30	50	ms

ELECTRICAL SPECIFICATIONS (Continued)

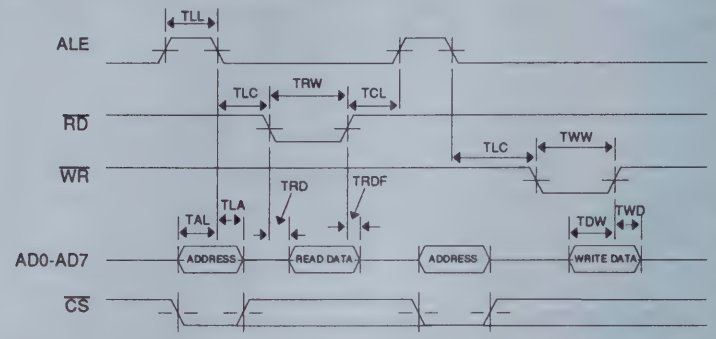
DYNAMIC CHARACTERISTICS AND TIMING (Continued)

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNITS
Guard Tone Generator					
Tone Accuracy	550 Hz				
	1800 Hz	-20		+20	Hz
Tone Level	550 Hz	-4.0	-3.0	-2.0	dB
(Below DPSK Output)	1800 Hz	-7.0	-6.0	-5.0	dB
Harmonic Distortion	550 Hz			-50	dB
700 to 2900 Hz	1800 Hz			-60	dB
Timing (Refer to Timing Diagrams)					
TAL	$\overline{CS}$/Addr. setup before ALE	30			ns
TLA	$\overline{CS}$/Addr. Hold after latch	20			ns
TLC	Latch to $\overline{RD}/\overline{WR}$ control	40			ns
TCL	$\overline{RD}/\overline{WR}$ Control to Latch	10			ns
TRD	Data out from $\overline{RD}$	0		160	ns
TLL	ALE width	60			ns
TRDF	Data float after READ	0		80	ns
TRW	READ width	200		25000	ns
TWW	WRITE width	140		25000	ns
TDW	Data setup before WRITE	150			ns
TWD	Data hold after WRITE	20			ns
TCKD	Data out after CLK			200	ns
TCKW	WRITE after CLK	150			ns
TDCK	Data setup before CLK	150			ns
TAC	Address setup before control [1]	50			ns
TCA	Address hold after control [1]	50			ns

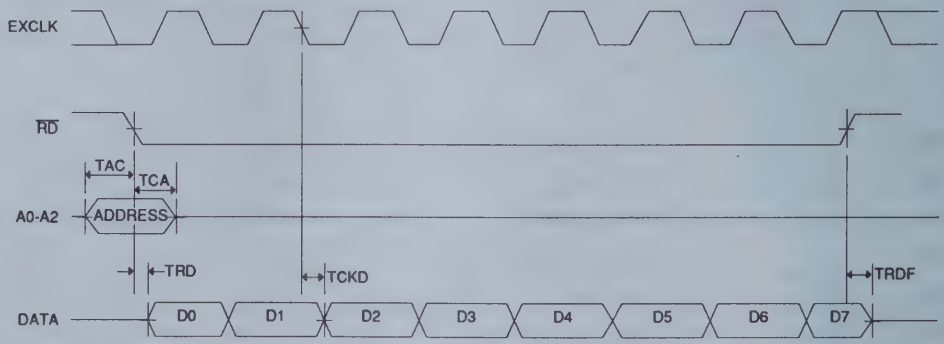
1: Control for setup is the falling edge of $\overline{RD}$ or $\overline{WR}$.
Control for hold is the falling edge of $\overline{RD}$ or the rising edge of $\overline{WR}$.

TIMING DIAGRAMS

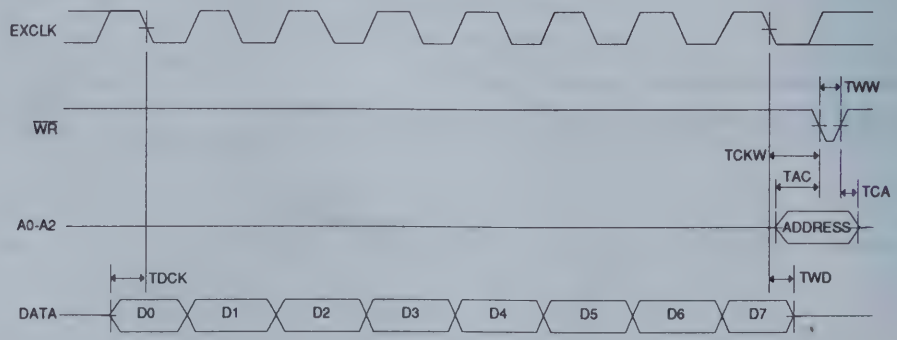
BUS TIMING DIAGRAM (PARALLEL VERSION)



READ TIMING DIAGRAM (SERIAL VERSION)



WRITE TIMING DIAGRAM (SERIAL VERSION)



APPLICATIONS INFORMATION

GENERAL CONSIDERATIONS

Figures 1 and 2 show the basic circuit diagram for K–Series modem integrated circuits. K-Series products are designed to be used in conjunction with a control processor, a UART or RS-232 serial data interface, and a DAA phone line interface to function as a typical intelligent modem. The K-Series ICs interface directly with Intel 8048 and 80C51 microprocessors for control and status monitoring purposes. Two typical DAA arrangements are shown: one for a split ±5 or ±12 volt design and one for a single 5 volt design. These diagrams are for reference only and do not represent production-ready modem designs.

K-Series devices are available in two control interface versions: one for a parallel multiplexed address/data interface, and one for a serial interface. The parallel version is intended for use with 8039/48 or 8031/51 microcontrollers from Intel or many other manufacturers. The serial interface 22-pin version can be used with other microcontrollers or in applications where only a limited number of port lines are available. The parallel versions may also be used in the serial mode, as explained in the data sheet pin description.

In most applications the controller will monitor the serial data for commands from the DTE and the received data for break signals from the far end modem. In this way, command data to the modem is sent over the same data line as the transmitted data. In other applications the RS-232 interface handshake lines are used for modem control.

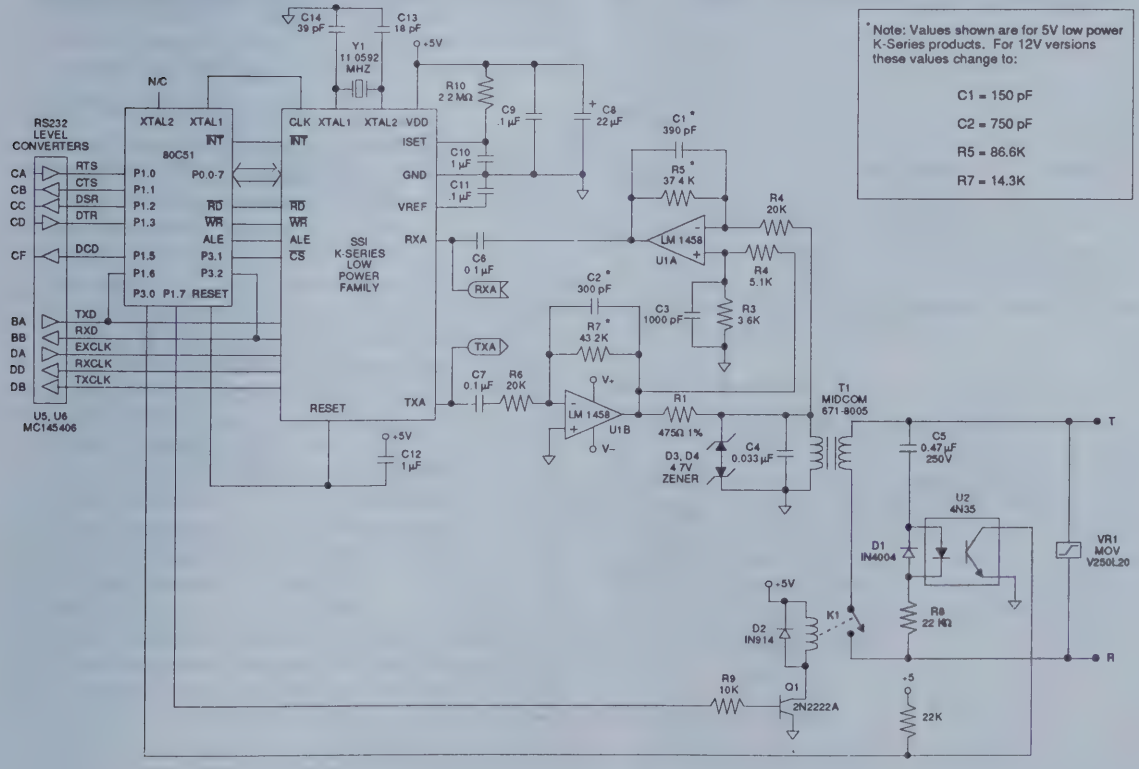


FIGURE 1: Basic Box Modem with Dual-Supply DAA

DIRECT ACCESS ARRANGEMENT (DAA)

The DAAs shown are two examples of how the "hybrid" may be implemented. The split supply design (Figure 1) is a typical two op-amp hybrid. The receive op-amp serves two purposes. It supplies gain to amplify the receive signal to the proper level for the modem's detectors and demodulator, and it removes the transmitted signal from the receive signal present at the transformer. This is done by supplying a portion of the transmitted signal to the non-inverting input of the receive op-amp at the same amplitude as the signal appearing at the transformer, making the transmit signal common mode.

The single-supply DAA is more complex than the dual-supply version described above, but its use eliminates the need for a second power supply. This DAA (Figure 2) uses a bridged drive to allow undistorted signals to be sent with a single 5 volt supply. Because DTMF tones utilize a higher amplitude than data, these signals will clip if a single-ended drive approach is used. The bridged driver uses an extra op-amp (U1A) to invert the signal coming from the gain setting op-amp (U1B) before sending it to the other leg of the transformer. Each op-amp then supplies half the drive signal to the transformer. The receive amplifier (op-amp C) picks off its signal at the junction of the impedance matching resistor and the transformer. Because the bottom leg of the transformer is being driven in one direction by U1A and the resistor is driven in the opposite direction at the same time by U1B, the summing point of the transformer and resistor remains relatively constant and the receive signal is unaffected.

DESIGN CONSIDERATIONS

Silicon Systems 1-chip modem products include all basic modem functions on a single IC, accessible from a standard bus interface. This makes these devices adaptable for use in a variety of applications, and as easy to control as conventional digital bus peripherals.

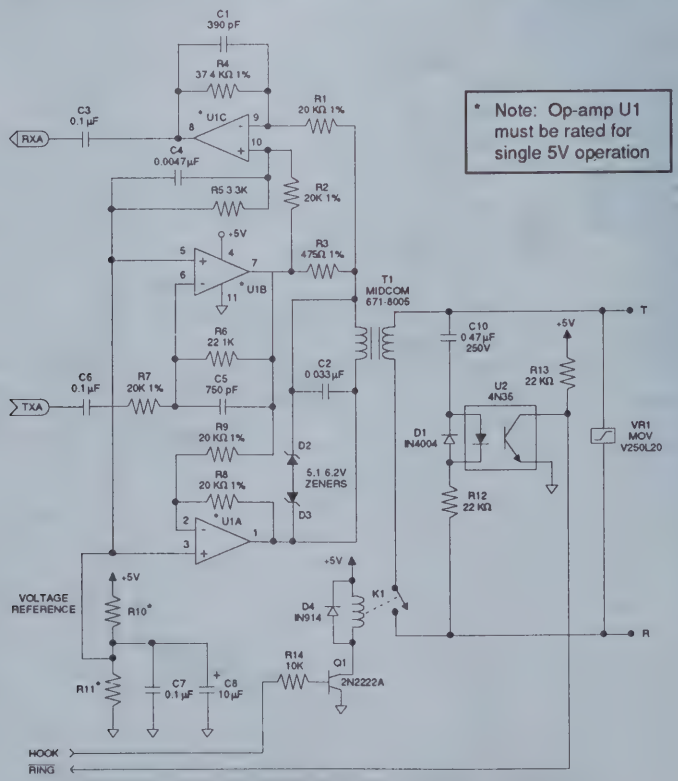


FIGURE 2: Single 5V DAA Version

Unlike digital logic circuitry, however, modem designs must properly contend with precise frequency tolerances, and very low level analog signals, to insure acceptable performance. Using good analog circuit design practices will generally result in a sound design. Folllowing are additional recommendations which should be taken into consideration when starting new designs.

CRYSTAL OSCILLATOR

The K-Series crystal oscillator requires a parallel mode (antiresonant) crystal which operates at 11.0592 MHz. It is important that this precise frequency be maintained to within ±.01% accuracy.

In order for a parallel mode crystal to operate correctly and to specification, it must have a load capacitor connected to the junction of each of the crystal and internal inverter connections, terminated to ground. The values of these capacitors depend primarily on the crystal's characteristics, and to a lesser degree on the internal inverter circuit. The values used affect the accuracy and start up characteristics of the oscillator.

LAYOUT CONSIDERATIONS

Good analog/digital design rules must be used to control system noise in order to obtain highest performance in modem designs. The more digital circuitry present on the PC board, the more this attention to noise control is needed. The modem should be treated as a high impedance analog device. A 22 µF electrolytic capacitor in parallel with a 0.1 µF ceramic capacitor between VDD and ground is recommended. Liberal use of ground planes and larger traces on power and ground are also highly favored. High speed digital circuits tend to generate a significant amount of EMI (Electro-Magnetic Interference) which must be minimized in order to meet regulatory agency limitations. To accomplish this, high speed digital devices should be locally bypassed, and the DAA and K-Series device should be located close to each other near the area of the board where the phone line connection is accessed. To avoid problems, power supply and ground traces should be routed separately to the analog and digital functions on the board, and digital signals should not be routed near low level or high impedance analog traces. The analog and digital grounds should only connect at one point near the analog supplies to avoid ground loops. The K–Series modem IC's should have both high frequency and low frequency bypassing as near to the package as possible.

MODEM PERFORMANCE CHARACTERISTICS

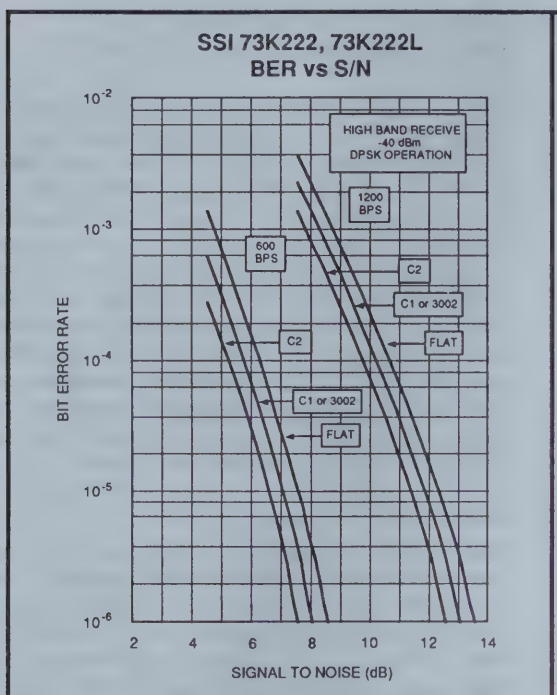
The curves presented here define modem IC performance under a variety of line conditions while inducing disturbances that are typical of those encountered during data transmission on public service telephone lines. Test data was taken using an AEA Electronics' "Autotest I" modem test set and line simulator, operating under computer control. All tests were run full-duplex, using a Concord Data Systems 224 as the reference modem. A 511 pseudo-random-bit pattern was used with $1X10^6$ bits transmitted for each data point. Noise was C-message weighted and all signal-to-noise (S/N) ratios reflect total power measurements similar to the CCITT V.56 measurement specification. The individual tests are defined as follows.

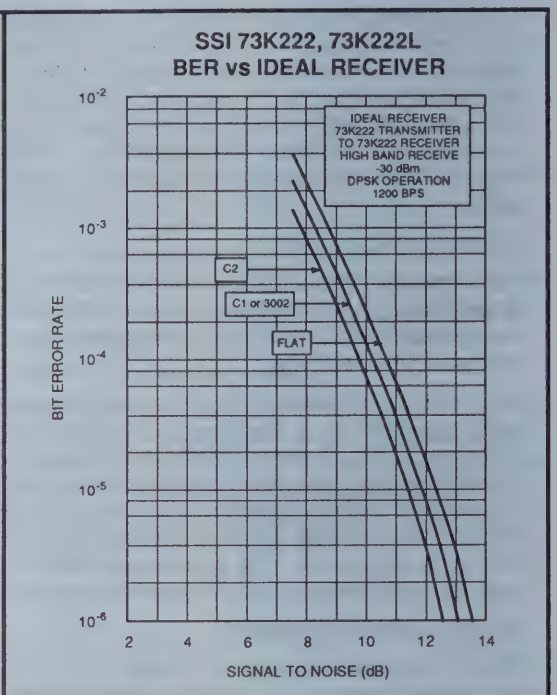
BER vs.S/N

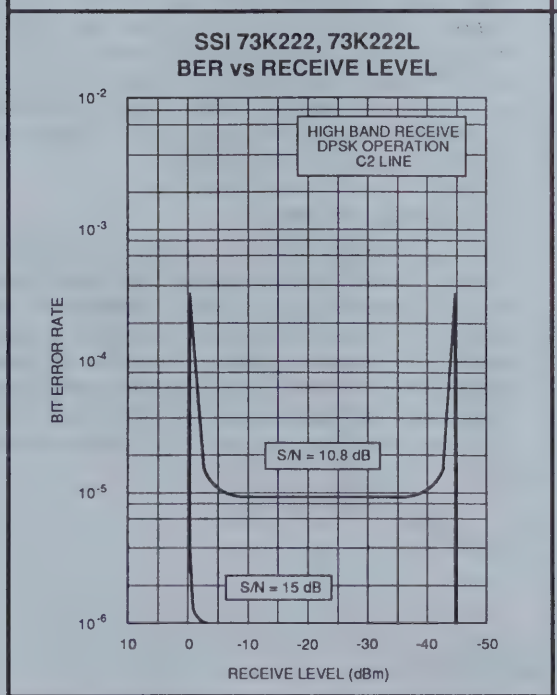
This test measures the ability of the modem to operate over noisy lines with a minimum of data-transfer errors. Since some noise is generated in the best of dial-up lines, the modem must operate with the lowest S/N ratio possible. Optimum modem performance is indicated by test curves that are closest to the zero axis. A narrow spread between curves representing the four line parameters indicates minimal variation in performance while operating over a range of aberrant operating conditions. Typically, a PSK modem will exhibit better BER-performance test curves operating in the highband range than in the lowband.

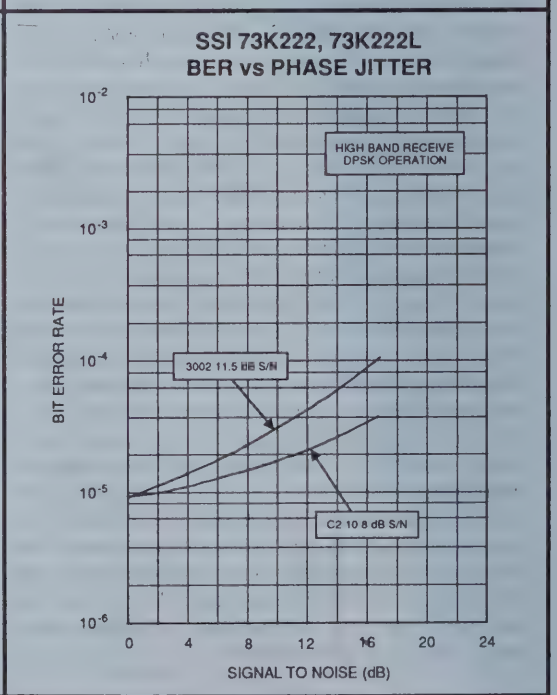
BER vs. Receive Level

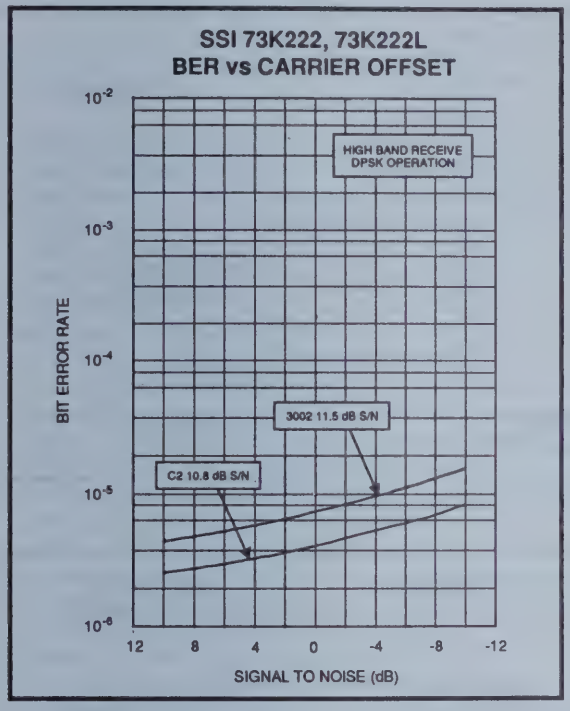
This test measures the dynamic range of the modem. Because signal levels vary widely over dial-up lines, the widest possible dynamic range is desirable. The minimum Bell specification calls for 36 dB of dynamic range. S/N ratios are held constant at the indicated values while the receive level is lowered from a very high to very low signal levels. The width of the "bowl" of these curves, taken at the BER point, is the measure of dynamic range.


SSI 73K222, 73K222L
BER vs S/N
HIGH BAND RECEIVE
-40 dBm
DPSK OPERATION
1200
BPS
600
BPS
C2
C1 or 3002
C2
FLAT
C1 or 3002
FLAT
BIT ERROR RATE
SIGNAL TO NOISE (dB)


SSI 73K222, 73K222L
BER vs IDEAL RECEIVER
IDEAL RECEIVER
73K222 TRANSMITTER
TO 73K222 RECEIVER
HIGH BAND RECEIVE
-30 dBm
DPSK OPERATION
1200 BPS
C2
C1 or 3002
FLAT
BIT ERROR RATE
SIGNAL TO NOISE (dB)


SSI 73K222, 73K222L
BER vs RECEIVE LEVEL
HIGH BAND RECEIVE
DPSK OPERATION
C2 LINE
S/N = 10.8 dB
S/N = 15 dB
BIT ERROR RATE
RECEIVE LEVEL (dBm)

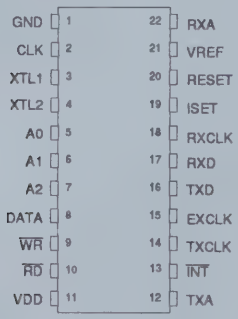

SSI 73K222, 73K222L
BER vs PHASE JITTER
HIGH BAND RECEIVE
DPSK OPERATION
3002 11.5 dB S/N
C2 10 8 dB S/N
BIT ERROR RATE
SIGNAL TO NOISE (dB)


SSI 73K222, 73K222L
BER vs CARRIER OFFSET
HIGH BAND RECEIVE
DPSK OPERATION
3002 11.5 dB S/N
C2 10.8 dB S/N
BIT ERROR RATE
10-2
10-3
10-4
10-5
10-6
12
8
4
0
-4
-8
-12
SIGNAL TO NOISE (dB)

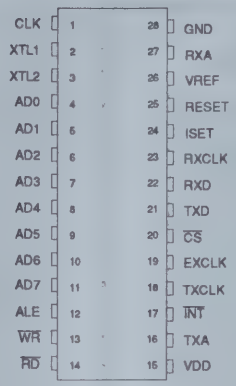
SSI 73K222/K222L
V.22, V.21, Bell 212A
Single-Chip Modem

PACKAGE PIN DESIGNATIONS

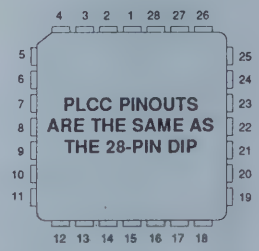
(TOP VIEW)



400-Mil
22-Pin DIP



600-Mil
28-Pin DIP



28-Lead
PLCC

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 73K222 with Parallel Bus Interface		
28-Pin 12 Volt Supply		
Plastic Dual-In-Line	73K222 – IP	SSI 73K222 – IP
Plastic Leaded Chip Carrier	73K222 – IH	SSI 73K222 – IH
28-Pin 5 Volt Supply		
Plastic Dual-In-Line	73K222L – IP	SSI 73K222L – IP
Plastic Leaded Chip Carrier	73K222L – IH	SSI 73K222L – IH
SSI 73K222 with Serial Interface		
22-Pin 12 Volt Supply		
Plastic Dual-In-Line	73K222S – IP	SSI 73K222S – IP
22-Pin 5 Volt Supply		
Plastic Dual-In-Line	73K222SL – IP	SSI 73K222SL – IP

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SSI 73K222U
Single-Chip Modem with UART

1

July, 1989

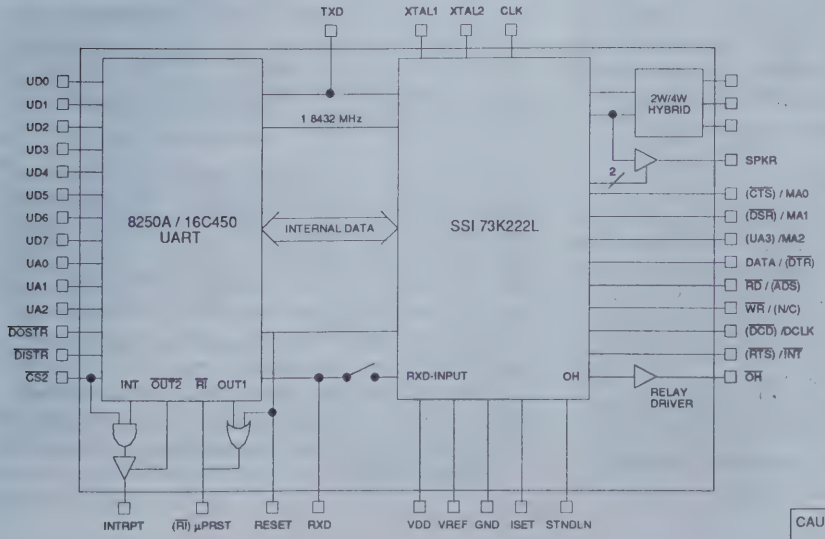
DESCRIPTION

The SSI 73K222U is a compact, high-performance modem which includes a 8250A/16C450 compatible UART with the 1200 bit/s modem function on a single chip. Based on the SSI 73K222L 5-volt low power CMOS modem IC, the SSI 73K222U is the perfect modem/UART component for dedicated integral modem applications. It is ideal for applications such as portable terminals and laptop computers. The SSI 73K222U is the first fully featured modem IC which can function as an intelligent modem in integral applications without requiring a separate dedicated microcontroller. It provides for data communication at 1200, 600, and 300 bit/s in a multi-mode manner that allows operation compatible with both Bell 212A/103 and CCITT V.22/V.21 operating standards. The digital interface section contains a high speed version of the industry-standard, 8250A/16C450 UART, commonly used in personal computer products. A unique feature of the SSI 73K222U is that the UART section can be used without the modem function, providing an additional asynchronous port at no added cost. The SSI 73K222U is designed in CMOS technology and operates from a single +5V supply. Available packaging includes 40-pin DIP or 44-pin PLCC for surface mount applications.

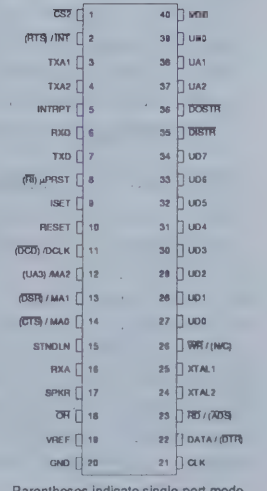
FEATURES

- **Modem/UART combination optimized for integral bus applications**
- **Includes features of SSI 73K222L single-chip modem**
- **Fully compatible 16C450/8250 UART with 8250B or 8250A selectable interrupt emulation**
- **High speed UART will interface directly with high clock rate bus with no wait states**
- **Compatible with SSI 73K212U (Bell 212A/103) and SSI 73K221U (CCITT V.22/V.21) family members**
- **Single-port mode allows full modem and UART control from CPU bus, with no dedicated microprocessor required**
- **Dual-port mode suits conventional designs using local microprocessor for transparent modem operation**
- **Complete modem functions for 1200 bit/s (Bell 212A, V.22) and 0-300 bit/s (Bell 103, V.21)**
- **Includes DTMF generator, carrier, call-progress and precise answer-tone detectors for intelligent dialing capability**
- **On chip 2-wire/4-wire hybrid driver and off-hook relay buffer**
- **Speaker output with four-level software driven volume control**
- **Low power CMOS (40 mW) with power down mode (15 mW)**
- **Operates from single +5V supply**

BLOCK DIAGRAM



PIN DIAGRAM



Parentheses indicate single-port mode.

CAUTION: Use handling procedures necessary for a static sensitive component.

SSI 73K222U
Single-Chip Modem with UART

FUNCTIONAL DESCRIPTION

The SSI 73K222U integrates an industry standard 8250/16C450 UART function with the modem capability provided by the SSI 73K222L single chip modem IC. The SSI 73K222U is designed specifically for integral microprocessor bus intelligent modem products. These designs typically require the standard 8250 or higher speed 16450 UART to perform parallel-to-serial and serial-to-parallel conversion process necessary to interface a parallel bus with the inherently serial modem function. The SSI 73K222U provides a highly integrated design which can eliminate multiple components in any integral bus modem application, and is ideal for internal PC modem applications.

The SSI 73K222U includes two possible operating modes. In the dual-port mode, the device is suitable for conventional plug-in modem card designs which use a separate local microprocessor for command interpretation and control of the modem function. In this mode, a dedicated microcontroller communicates with the SSI 73K222U using a separate serial command port. In the single-port mode the main CPU can control both the UART and modem function using the parallel data bus. This allows very efficient modem design with no local microprocessor required for dedicated applications such as laptop PC's or specialized terminals.

To make designs more space efficient, the SSI 73K222U includes the 2-wire to 4-wire hybrid drivers, off-hook relay driver, and an audio monitor output with software volume control for audible call progress monitoring. As an added feature the UART function can be used independent of the modem function, providing an added asynchronous port in a typical PC application with no additional circuitry required.

UART FUNCTION (16C450)

The UART section of the SSI 73K222U is completely compatible with the industry standard 16C450 and the 8250 UART devices. The bus interface is identical to the 16450, except that only a single polarity for the control signals is supported. The register contents and addresses are also the same as the 16C450. To insure compatibility with all existing releases of the 8250 UART design, external circuitry normally used in PC applications to emulate 8250B or 8250A interrupt operation has been included on the SSI 73K222U. A select line is then provided to enable the desired interrupt operation. The UART used in the SSI 73K222U can tolerate faster bus read and write cycles than a conventional 16C450 UART. This allows it to interface directly with higher clock rate microprocessors with no need for external circuitry to generate wait states.

The primary function of the UART is to perform parallel-to-serial conversion on data received from the CPU and serial-to-parallel conversion on data received from the internal modem or an external device. The UART can program the number of bits per character, parity bit generation and checking, and the number of stop bits. The UART also provides break generation and detection, detection of error conditions, and reporting of status at any time. A prioritized maskable interrupt is also provided.

The UART block has a progammable baud rate generator which divides an internal 1.8432 MHz clock to generate a clock at 16 x the data rate. The data rate for the transmit and receive sections must be the same. For DPSK modulation, the data rate must be 1200 Hz or 600 Hz. For FSK modulation, the data rate must be 300 Hz or less. The baud generator can create a clock that supports digital transfer at up to 115.2 KHz. The output of the baud generator can be made available at the CLK pin under program control.

MODEM FUNCTION (SSI 73K222L)

The modem section of the SSI 73K222U provides all necessary analog functions required to create a single chip Bell 212A/103 and CCITT V.22/V.21 modem, controlled by the system CPU or a local dedicated microprocessor. Asynchronous 1200 bit/s DPSK (Bell 212A and V.22) and 300 baud FSK (Bell 103 and V.21) modes are supported.

The modem portion acts as a peripheral to the microprocessor on a serial command bus. In both modes of operation, control information is stored in register memory at specific address locations. In the single-port mode, the modem section can be controlled through the 16C450 interface, with no external microcontroller required. The primary analog blocks are the DPSK modulator/demodulator, the FSK modulator/demodulator, the high and low band filters, the AGC, the special detect circuitry, and the DTMF tone generator. The analog functions are performed with switched capacitor technology.

SSI 73K222U
Single-Chip Modem with UART

PSK MODULATOR / DEMODULATOR

The SSI 73K222U modulates a serial bit stream into dibit pairs that are represented by four possible phase shifts as prescribed by the Bell 212A or V.22 standard. The baseband signal is then filtered to reduce intersymbol interference on the band limited 2-wire PSTN line. Transmission occurs using either a 1200 Hz (originate mode) or 2400 Hz carrier (answer mode). Demodulation is the reverse of the modulation process, with the incoming analog signal eventually decoded into dibits and converted back to a serial bit stream. The demodulator also recovers the clock which was encoded into the analog signal during modulation. The demodulator decodes either a 1200 Hz carrier (originate carrier) or a 2400 Hz carrier (answer carrier). The SSI 73K222U uses a phase-locked-loop coherent demodulation technique that offers inherently better performance than typical DPSK demodulators used by other manufacturers.

FSK MODULATOR/DEMODULATOR

The FSK modulator frequency modulates the analog output signal using two discrete frequencies to represent the binary data. In Bell 103, the standard frequencies of 1270 Hz and 1070 Hz (originate mark and space) and 2225Hz and 2025 Hz (answer mark and space) are used. V.21 mode uses 980 Hz and 1180 Hz (originate, mark and space) or 1650 Hz and 1850 Hz (answer, mark and space). Demodulation involves detecting the received frequencies and decoding them into the appropriate binary value.

PASSBAND FILTERS AND EQUALIZERS

A high and low band filter is included to shape the amplitude and phase response of the transmit signal and provide compromise delay equalization and rejection of out-of-band signals in the receive channel. Amplitude and phase equalization is necessary to compensate for distortion of the transmission line and to reduce intersymbol interference in the band limited receive signal. The transmit signal filtering approximates a 75% square root of raised Cosine frequency response characteristic.

AGC

The automatic gain control maintains a signal level at the input to the demodulators which is constant to within 1 dB. It corrects quickly for increases in signal which would cause clipping, and provides a total dynamic range of >45 dB.

SPECIAL DETECT CIRCUITRY

The special detect circuitry monitors the received analog signal to determine status or presence of carrier, call-progress tones, answer tone, and weak received signal (long loop condition). An unscrambled mark signal is also detected when the received data out of the DPSK demodulator before the descrambler has been high for 165.5 mS±13.5 mS. The appropriate status bit is set when one of these conditions changes and an interrupt is generated for all monitored conditions except long loop. The interrupts are disabled (masked) when the enable interrupt bit is set to a 0.

DTMF GENERATOR

The DTMF generator will output one of 16 standard dual-tones determined by a 4-bit binary value and TX DTMF mode bit previously loaded into the tone register. Dialing is initiated when the DTMF mode is selected and the transmit enable (CR0 bit D1) is changed from a 0 to a 1.

TEST FEATURES

Test features such as analog loopback (ALB), remote digital loopback, local digital loopback, and internal pattern generators are also included.

LINE INTERFACE

The line interface of the SSI 73K222U consists of a two-to-four wire hybrid, and an off-hook relay driver.

The two-to-four wire converter has a differential transmit output and requires only a line transformer and an external impedance matching resistor. Four-wire operation is also available by simply using either of the transmit output signals.

The relay driver output of the SSI 73K222U is an open drain signal capable of sinking 20 mA, which can control a line closure relay used to take the line off hook and to perform pulse dialing.

AUDIO MONITOR

An audio monitor output is provided which has a software programmable volume control. Its output is the received signal. The audio monitor output can directly drive a high impedance load, but an external power amplifier is necessary to drive a low-impedance speaker.

PIN DESCRIPTION

GENERAL

NAME	DIP	PLCC	TYPE	DESCRIPTION
VDD	40	44	I	+5V Supply ±10%, bypass with a .1 and a 22µF capacitor to GND
GND	20	22	I	System Ground
VREF	19	21	O	VREF is an internally generated reference voltage which is externally bypassed by a .1µF capacitor to the system ground.
ISET	9	11	I	The analog current is set by connecting this pin to VDD through a 2MΩ resistor. ISET should be bypassed to GND. Alternatively, an internal bias can be selected by connecting ISET to GND, which will result in a larger worst-case supply current due to the low tolerance of on-chip resistors. Bypass with .1µF capacitor if resistor is used.
XTAL1 XTAL2	25 24	27 26	I I	These pins are inputs for the internal crystal oscillator requiring an 11.0592 MHz crystal (9216Hz x 1200). XTAL2 can also be TTL driven from an external clock.
CLK	21	23	O	Output Clock. This pin is selectable under processor control to be either the crystal frequency (which might be used as a processor clock) or the output of the baud generator.
RESET	10	12	I	Reset. An active signal (high) on this pin will put the chip into an inactive state. The control register bits (except the Receiver Buffer, Transmitter Holding, and Divisor latches) will be reset. The output of the CLK pin will be set to the crystal frequency. An internal pull-down resistor permits power-on reset using a 0.1µF capacitor connected to the 5V supply.
STNDLN	15	17	I	Single-port mode select (active high). In a single-port system there is no local microprocessor and all the modem control is done through the 16C450 parallel bus interface. The local microprocessor interface is replaced with UART control signals which allow the device to function as a digital UART as well as modem.

PIN DESCRIPTION (continued)

UART INTERFACE

NAME	DIP	PLCC	TYPE	DESCRIPTION
UA0-UA2 UA3	37-39 12	41-43 14	I I	UART Address. These pins determine which of the UART registers is being selected during a read or write on the UART data bus. The contents of the DLAB bit in the UART's Line Control Register also control which register is referenced. In single-port mode, UA0-UA3 are latched when $\overline{ADS}$ goes high. In dual-port, only UA0-UA2 are used.
UD0-UD7	27-34	30-37	I/O	(3 state) UART Data. Data or control information to the UART registers is carried over these lines.
$\overline{DISTR}$	35	38	I	Data Input Strobe. A low on this pin requests a read of the internal UART registers. Data is output on the D0-D7 lines if $\overline{DISTR}$ and $\overline{CS2}$ are active.
$\overline{DOSTR}$	36	39	I	Data Output Strobe. A low on this pin requests a write of the internal UART registers. Data on the D0-D7 lines are latched on the rising edge of $\overline{DOSTR}$. Data is only written if both $\overline{DOSTR}$ and $\overline{CS2}$ are active.
$\overline{CS2}$	1	2	I	Chip Select. A low on this pin allows a read or write to the UART registers to occur. In single port mode, $\overline{CS2}$ is latched on $\overline{ADS}$.
INTRPT	5	7	O	(3 state) UART Interrupt. This signal indicates that an interrupt condition on the UART side has occurred. If the Enable 8250A interrupt bit in the interrupt Enable Register is 0 the interrupt is gated by the $\overline{DISTR}$ signal to provide compatibility with the 8250B. The output can be put in a high impedance state with the OUT2 register bit in the Modem Control Register. In single-port mode, INTRPT also becomes valid when a modem interrupt signal is generated by the modem section's Detect Register.
RXD	6	8	I/O	Function is determined by STNDLN pin and bit 7, Tone Control Register:

STNDLN	D7	
0	0	RXD outputs data received by modem.
1	0	RXD is electrically an input but signal is ignored.
X	1	RXD is a serial input to UART.

PIN DESCRIPTION (continued)

UART INTERFACE (continued)

TXD	7	9	O	Function is determined by STNDLN pin and bit 7, Tone Control Register:		
				STNDLN	D7	
				0	0	TXD is a serial output of UART.
				1	0	TXD is forced to a mark.
				X	1	TXD is a serial output of UART.

ANALOG / LINE INTERFACE

NAME	DIP	PLCC	TYPE	DESCRIPTION
TXA1 TXA2	3 4	4 5	O O	(differential) Transmitted Analog. These pins provide the analog output signals to be transmitted to the phone line. The drivers will differentially drive the impedance of the line transformer and the line matching resistor. An external hybrid can also be built using TXA1 as a single ended transmit signal.
RXA	16	18	I	Received Analog. This pin inputs analog information that is being received by the two-to-four wire hybrid. This input can also be taken directly from an external hybrid.
SPKR	17	19	O	Speaker Output. This pin outputs the received signal through a programmable attenuator stage, which can be used for volume control and disabling the speaker.
$\overline{OH}$	18	20	O	Off-hook relay driver. This signal is an open drain output capable of sinking 20mA and is used for controlling a relay. The output is the complement of the $\overline{OH}$ register bit in CR3.

PIN DESCRIPTION (continued)

UART CONTROL INTERFACE (STNDLN = 1)

(See Figure 1: Single-port mode)

NAME	DIP	PLCC	TYPE	DESCRIPTION
$\overline{ADS}$	23	25	I	Address Strobe. $\overline{ADS}$ is used to latch address and chip select to simplify interfacing to a multiplexed Address/Data Bus. UA0-UA3 and $\overline{CS2}$ are latched when the $\overline{ADS}$ signal goes high.
UA3	12	14	I	UART Address Bit 3. UA3 is used in single-port mode to address the modem registers from the 16C450 interface. If UA3 is 0, the normal 16C450 registers are addressed by UA0-UA2 and if UA3 is 1, the modem registers are addressed. UA3 is latched when $\overline{ADS}$ goes high.
$\overline{CTS}$	14	16	I	Clear to Send. This pin is the complement of CTS bit in the Modem Status Register. The signal is used in modem handshake control to signify that communications have been established and that data can be transmitted.
$\overline{DSR}$	13	15	I	Data Set Ready. This pin is the complement of DSR bit in the Modem Status Register. The signal is used in modem handshake to signify that the modem is ready to establish communications.
$\overline{DCD}$	11	13	I	Data Carrier Detect. This pin is the complement of DCD bit in the Modem Status Register. The signal is used in modem control handshake to signify that the modem is receiving a carrier.
$\overline{DTR}$	22	24	O	Data Terminal Ready. The $\overline{DTR}$ output is programmed through a bit in the Modem Control Register. The signal is used in modem handshake to signify that the 16C450 is available to communicate.
$\overline{RTS}$	2	3	O	Request to Send. The $\overline{RTS}$ output is programmed through a bit in the Modem Control Register. The signal is used in modem handshake to signify that the 16C450 has data to transmit.
$\overline{RI}$	8	10	I	Ring Indicator. This Indicates that a telephone ringing signal is being received. This pin is the complement of the RI bit in the Modem Status Register.

PIN DESCRIPTION (continued)

MICROPROCESSOR INTERFACE (STNDLN = 0)

(See Figure 2: Dual-port mode)

NAME	DIP	PLCC	TYPE	DESCRIPTION
MA0-MA2	12-14	14-16	I	Modem Address Control. These lines carry register addresses for the modem registers and should be valid throughout any read or write operation.
DATA	22	24	I/O	Serial Control Data. Serial control data to be read/written is clocked in/out on the falling edge of the DCLK pin. The direction of data transfer is controlled by the state of the $\overline{RD}$ pin. If the $\overline{RD}$ pin is active (low) the DATA line is an output. Conversely, if the $\overline{RD}$ pin is inactive (high) the DATA line is an input.
$\overline{RD}$	23	25	I	Read. A low on this input informs the SSI 73K222U that control data or status information is being read by the processor from a modem register.
$\overline{WR}$	26	28	I	Write. A low on this input informs the SSI 73K222U that control data or status information is available for writing into a modem register. The procedure for writing is to shift in data LSB first on the DATA pin for eight consecutive cycles of DCLK and then to pulse $\overline{WR}$ low. Data is written on the rising edge of $\overline{WR}$.
DCLK	11	13	I	Data Clock. The falling edge of this clock is used to strobe control data for the modem registers in or out on the DATA pin. The normal procedure for a write is to shift in data LSB first on the DATA pin for eight consecutive cycles of DCLK and then to pulse $\overline{WR}$ low. Data is written on the rising edge of $\overline{WR}$. The falling edge of the $\overline{RD}$ signal must continue for eight cycles of DCLK in order to read all eight bits of the reference register. Read data is provided LSB first. Data will not be output unless the $\overline{RD}$ signal is active.
$\overline{INT}$	2	3	O	(with weak pull-up) Modem Interrupt. This output signal is used to inform the modem processor that a change in a modem detect flag has occurred. The processor must then read the Modem Detect Register to determine which detect triggered the interrupt. $\overline{INT}$ will stay active until the processor reads the Modem Detect Register or does a full reset.
µPRST*	8	10	O	Microprocessor Reset. This output signal is used to provide a hardware reset to the microprocessor. This signal is high if the RESET pin is high or the MCR bit D3 (OUT1) bit is set.

* NOTE: The µPRST pin is an upgraded function which was not included in the initial definition of the SSI 73K222U.

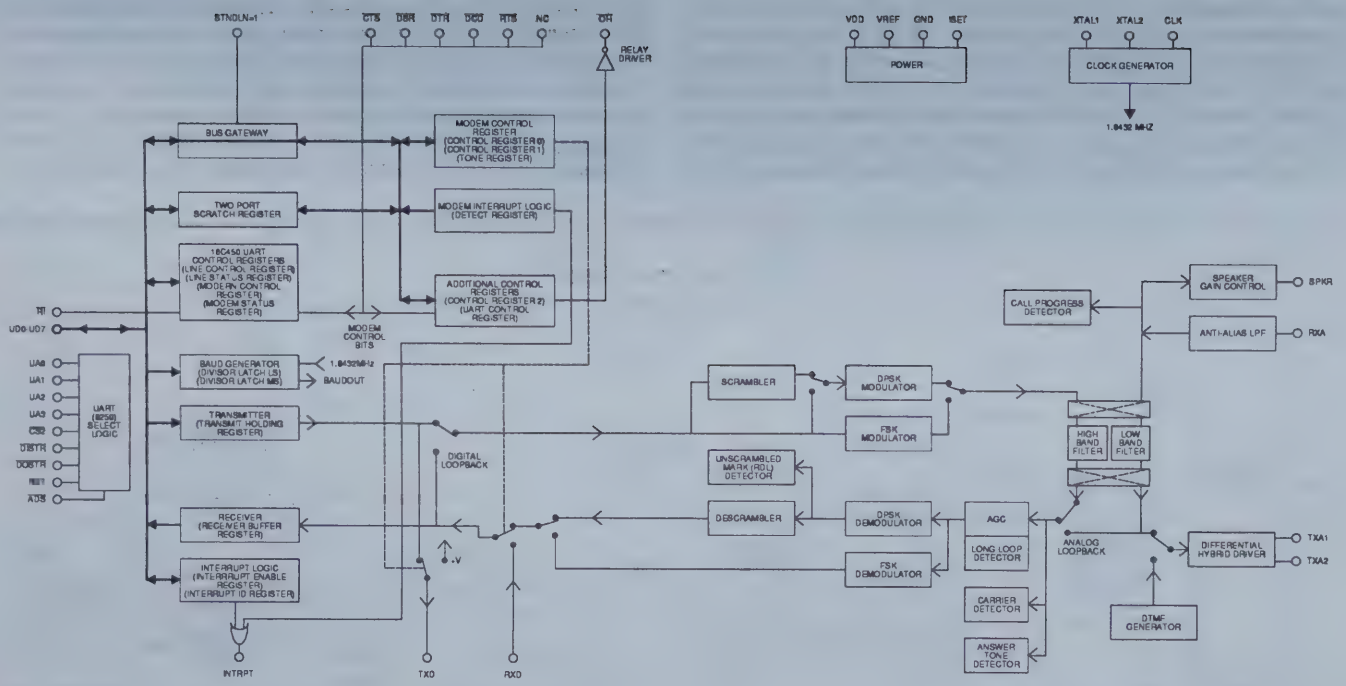


FIGURE 1:
SINGLE-PORT MODE

In the single-port mode, the SSI 73K222U is designed to be accessed only by the main CPU using the same parallel bus utilized for data transfer. This mode is enabled when the STNDLN pin is at a logic "1". In the single port mode, internal registers are accessed by the main CPU to configure both the UART section and the modem function, eliminating the need for a separate microcontroller. In this mode, multiplexed pins provide the $\overline{CTS}$, $\overline{DSR}$, $\overline{DTR}$, $\overline{DED}$ and $\overline{RI}$ signals normally associated with the UART function. A separate pin, $\overline{ADS}$, is used for bus control.

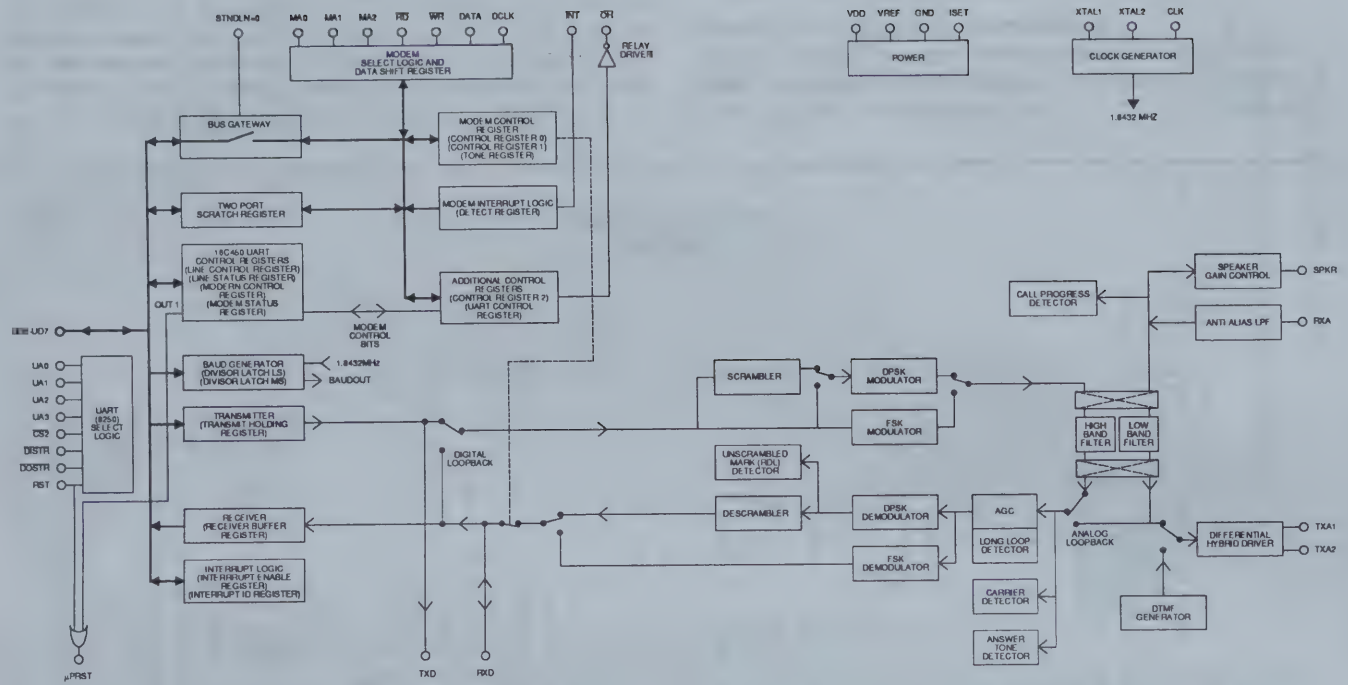


FIGURE 2:
DUAL-PORT MODE

The dual-port mode allows use of a dedicated microprocessor for control of the modem function, and is enabled when the STNDLN pin = "0". This mode is useful for conventional plug-in card modem designs where it is necessary to make the modem function transparent to the main CPU. In this mode, the SSI 73K222U's multiplexed pins form the serial command bus used to communicate with the external microprocessor. The $\overline{RI}$, $\overline{CTS}$, $\overline{DSR}$, $\overline{DTR}$, and $\overline{DCD}$ logic functions must then be implemented using ports from the dedicated microprocessor.

The serial control interface allows access to the control and status registers via a serial command port. In this mode the MA0, MA1, and MA2 lines provide register addresses for data passed through the DATA pin under control of the $\overline{RD}$ and $\overline{WR}$ lines. A read operation is initiated when the $\overline{RD}$ line is taken low. The next eight cycles of DCLK will then transfer out eight bits of the selected address location LSB first. A write takes place by shifting in eight bits of data LSB first for eight consecutive cycles of DCLK. $\overline{WR}$ is then pulsed low and data transfer into the selected register occurs on the rising edge of $\overline{WR}$.

UART CONTROL REGISTER OVERVIEW

REGISTER		UART ADDRESS UA3-UA0*	DATA BIT NUMBER D7	D6	D5	D4	D3	D2	D1	D0
RECEIVER BUFFER REGISTER (READ ONLY)	RBR	0000 DLAB = 0	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
TRANSMIT HOLDING REGISTER (WRITE ONLY)	THR	0000 DLAB = 0	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
INTERRUPT ENABLE REGISTER	IER	0001 DLAB = 0	0	0	0	ENABLE 8250A/ 16C450 INTERRUPT	ENABLE MODEM STATUS INTERRUPT	ENABLE REC. LINE STATUS INTERRUPT	ENABLE THR EMPTY INTERRUPT	ENABLE REC. DATA AVAILABLE INTERRUPT
INTERRUPT ID REGISTER (READ ONLY)	IIR	0010	0	0	0	0	0	INTERRUPT ID BIT 1	INTERRUPT ID BIT 0	"0" IF INTERRUPT PENDING
LINE CONTROL REGISTER	LCR	0011	DIVISOR LATCH ACCESS (DLAB)	SET BREAK	STICK PARITY	EVEN PARITY SELECT (EPS)	PARITY ENABLE (PEN)	NUMBER OF STOP BITS (STB)	WORD LENGTH SELECT 1 (WLS1)	WORD LENGTH SELECT 0 (WLS0)
MODEM CONTROL REGISTER	MCR	0100	0	0	0	LOOP	ENABLE INTERRUPT (OUT2 IN 16C450)	µPRST (OUT1 IN 16C450)	REQUEST TO SEND (RTS)	DATA TERMINAL READY (DTR)
LINE STATUS REGISTER	LSR	0101	0	TRANSMIT SHIFT REG. EMPTY (TSRE)	TRANSMIT HOLDING REGISTER EMPTY(THRE)	BREAK INTERRUPT (BI)	FRAMING ERROR (FE)	PARITY ERROR (PE)	OVERRUN ERROR (OE)	DATA READY (DR)
MODEM STATUS REGISTER (READ ONLY)	MSR	0110	DATA CARRIER DETECT (DCD)	RING INDICATOR (RI)	DATA SET READY (DSR)	CLEAR TO SEND (CTS)	DELTA DATA CARR. DETECT (DDCD)	TRAILING EDGE RING INDICATOR (TERI)	DELTA DATA SET READY (DDSR)	DELTA CLEAR TO SEND (DCTS)
SCRATCH REGISTER	SCR	0111	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DIVISOR LATCH (LS)	DLL	0000 DLAB = 1	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DIVISOR LATCH (MS)	DLM	0001 DLAB = 1	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8

* In single-port mode (STNDLN pin = 1), all four address lines UA3-UA0 are used to address the UART Control Registers.

* In dual-port mode (STNDLN pin = 0), only three address lines UA2-UA0 are used to address the UART Control Registers; the UA3 pin becomes the MA2 pin in this mode.

MODEM CONTROL REGISTER OVERVIEW

REGISTER		ADDRESS STNDLN 0 MA2-MA0	ADDRESS STNDLN 1 UA3-UA0	DATA BIT NUMBER D7	D6	D5	D4	D3	D2	D1	D0
CONTROL REGISTER 0	CR0	000	1000	MODULATION OPTION	0	MODULATION MODE	POWER ON	CHARACTER SIZE 1 (READ ONLY)	CHARACTER SIZE 0 (READ ONLY)	TRANSMIT ENABLE	ORIGINATE/ ANSWER
CONTROL REGISTER 1	CR1	001	1001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTERRUPT	BYPASS SCRAMBLE	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0
DETECT REGISTER	DR	010	1010	DEVICE SIGNAL 1	DEVICE SIGNAL 0	RECEIVE DATA	UNSCR. MARK DETECT	CARRIER DETECT	ANSWER TONE DETECT	CALL PROGRESS DETECT	LONG LOOP DETECT
TONE CONTROL REGISTER	TONE	011	1011	RXD/TXD CONTROL	TRANSMIT GUARD TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF 3	DTMF 2	DTMF 1	DTMF 0 GUARD/ANS. TONE
CONTROL REGISTER 2	CR2	100	1100	RESERVED FOR FUTURE USE							
CONTROL REGISTER 3	CR3	101	1101	SPEAKER VOLUME 1	SPEAKER VOLUME 0	OFF-HOOK	X	X	X	X	X
SCRATCH REGISTER	SCR	110	1110	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
UART CONTROL REGISTER	UCR	111	1111	TXCLK (READ ONLY)	X	REQUEST TO SEND (RTS) (READ ONLY)	DATA TERM. READY (DTR) (READ ONLY)	RING INDICATOR (RI)	DATA CARRIER DETECT (DCD)	DATA SET READY (DSR)	CLEAR TO SEND (CTS)

UART REGISTER BIT DESCRIPTIONS

RECEIVER BUFFER REGISTER (RBR) (READ ONLY)

STNDLN:	0	1
ADDRESS:	UA2 - UA0 = 000, DLAB = 0	UA3 - UA0 = 0000, DLAB = 0

This read only register contains the parallel received data with start, stop, and parity bits (if any) removed. The high order bits for less than 8 data bits/character will be set to 0.

TRANSMIT HOLDING REGISTER (THR) (WRITE ONLY)

STNDLN:	0	1
ADDRESS:	UA2 - UA0 = 000, DLAB = 0	UA3 - UA0 = 0000, DLAB = 0

This write only register contains the parallel data to be transmitted. The data is sent LSB first with start, stop, and parity bits (if any) added to the serial bit stream as the data is transferred.

INTERRUPT ENABLE REGISTER (IER)

STNDLN:	0	1
ADDRESS:	UA2 - UA0 = 001, DLAB = 0	UA3 - UA0 = 0001, DLAB = 0

This 8-bit register enables the four types of interrupts of the UART to separately activate the chip Interrupt (INTRPT) output signal. It is possible to totally disable the interrupt system by resetting bits 0 through 3 of the Interrupt Enable Register. Similarly, by setting the appropriate bits of this register to a logic 1, selected interrupts can be enabled. Disabling the interrupt system inhibits the Interrupt Identification Register and the active (high) INTRPT output from the chip. All other system functions operate in their normal manner, including the setting of the Line Status and Modem Status Registers.

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	Received Data	1	This bit enables the Received Data Available Interrupt when set to logic 1.
D1	Transmitter Holding Register Empty	1	This bit enables the Transmitter Holding Register Empty Interrupt, when set to logic 1.
D2	Receiver Line Status Interrupt	1	This bit enables the Receiver Line Status Interrupt, when set to logic 1.
D3	Modem Status	1	This bit enables the Modem Status Register Interrupt when set to interrupt logic 1.
D4	8250A/16450	1/0	Set for compatibility with 8250A/16C450 UARTS. Reset this bit to disable the gating of the INTRPT interrupt line with the $\overline{\text{DISTR}}$ signal which is needed for 8250B compatibility.
D5 - D7	Not Used	0	These three bits are always logic 0.

INTERRUPT ID REGISTER (IIR) (READ ONLY) **UART SECTION**

STNDLN:	**0**	**1**
ADDRESS:	**UA2 - UA0 = 010**	**UA3 - UA0 = 0010**

The IIR register gives prioritized information as to the status of interrupt conditions. When accessed, the IIR freezes the highest priority interrupt pending and no other interrupts are acknowledged until the particular interrupt is serviced by the CPU.

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	Interrupt Pending	0	This bit can be used in either a hardwired priortized or polled environment to indicate whether an interrupt is pending. When bit 0 is a logic 0, an interrupt is pending and the IIR contents may be used as a pointer to the appropriate interrupt service routine.
		1	When bit 0 is a logic 1, no interrupt is pending.
D1, D2	Interrupt ID bits 0, 1	Table below	These two bits of the IIR are used to identify the highest priority interrupt pending as indicated in the following table.
D3 - D7	Not Used	0	These five bits of the IIR are always logic 0.

INTERRUPT PRIORITY TABLE

D2	D1	D0	PRIORITY	TYPE	SOURCE	RESET
0	0	1	-	None	None	-
1	1	0	Highest	Receiver Line Status	Overrun Error, Parity Error, Framing Error or Break Interrupt	Reading the Line Status Register
1	0	0	Second	Receive Data Available	Receive Data Available	Reading the Rcvr. Buffer Register
0	1	0	Third	Transmit Holding Register Empty	Transmit Holding Register Empty	Reading IIR Register (if source of interrupt) or Writing to Transmit Holding Register
0	0	0	Fourth	Modem Status	Clear to Send or Data Set Ready or Ring Indicator or Data Carrier Det.	Reading the Modem Status Register

LINE CONTROL REGISTER (LCR)
STNDLN: 0 1
ADDRESS: UA2 - UA0 = 011 UA3 - UA0 = 0011

The user specifies the format of the asynchronous data communications exchange via the Line Control Register. In addition to controlling the format, the user may retrieve the contents of the Line Control Register for inspection. This feature simplifies system programming and eliminates the need for separate storage in system memory of the line characteristics.

BIT NO.	NAME	CONDITION		DESCRIPTION
D0	Word Length Select 0			Bits D0 and D1 select the number of data bits per character as shown:
D1	Word Length Select 1	D1	D0	Word Length
		0	0	5 bits
		0	1	6 bits
		1	0	7 bits
		1	1	8 bits
D2	Number of Stop Bits	0 or 1		This bit specifies the number of stop bits in each transmitted character. If bit 2 is a logic 0, one stop bit is generated in the transmitted data. If bit 2 is a logic 1 when a 5-bit word length is selected via bits 0 and 1, one-and-a-half stop bits are generated. If bit 2 is a logic 1 when either a 6, 7, or 8-bit word length is selected, two stop bits are generated. The receiver checks the first stop bit only, regardless of the number of stop bits selected.
D3	Parity Enable	1		This bit is the Parity Enable bit. When bit 3 is a logic 1, a parity bit is generated (transmit data) or checked (receive data) between the last data word bit and stop bit of the serial data. (The parity bit is used to produce an even or odd number of 1's when the data word bits and the parity bit are summed).
D4	Even Parity Select	1 or 0		This bit is the Even Parity Select bit. When bit 3 is a logic 1 and bit 4 is a logic 0, an odd number of logic 1's are transmitted or checked in the data word bits and parity bit. When bit 3 is a logic 1 and bit 4 is a logic 1, an even number of logic 1's are transmitted or checked.

LINE CONTROL REGISTER (LCR) (Continued) **UART SECTION**

BIT NO.	NAME	CONDITION		DESCRIPTION
D5	Stick Parity	1 or 0		This bit is the Stick Parity bit. When bit 3 is a logic 1 and bit 5 is a logic 1, the parity bit is transmitted and checked by the receiver as a logic 0 if bit 4 is a logic 1 or as a logic 1 if bit 4 is a logic 0.
		D5	D4	Parity
		0	0	ODD Parity
		0	1	EVEN Parity
		1	0	MARK Parity
		1	1	SPACE Parity
D6	Set Break	1		Output of modem is set to a spacing state. When the modem is transmitting DPSK data if the Set Break bit is held for one full character (start, data, parity, stop) the break will be extended to 2 N + 3 space bits (where N = # data bits + parity bit + 1 start + 1 stop). Any data bits generated during this time will be ignored. See note below.
D7	Divisor Latch Access Bit (DLAB)	1		This bit is the Divisor Latch Access Bit (DLAB). It must be set high (logic 1) to access the Divisor Latches of the baud generator during a Read or Write operation. It must be set low (logic 0) to access the Receiver Buffer, the Transmitter Holding Register, or the Interrupt Enable Register.

NOTE: This feature enables the CPU to alert a terminal in a computer communications system. If the following sequence is followed, no erroneous or extraneous characters will be transmitted because of the break.

1. Load an all 0's pad character in response to THRE.
2. Set break in response to the next THRE.
3. Wait for the Transmitter to be idle. (TSRE = 1), and clear break when normal transmission has to be restored.

During the break, the Transmitter can be used as a character timer to accurately establish the break duration.

MODEM CONTROL REGISTER (MCR)

STNDLN:	**0**	**1**
ADDRESS:	**UA2 - UA0 = 100**	**UA3 - UA0 = 0100**

The MCR register controls the interface with the modem. Bits D1 and D0 are also available as read only bits in the UART Control Register in the Modem Registers. In single-port mode, bits D1 and D0 are available inverted at the $\overline{RTS}$ and $\overline{DTR}$ pins.

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	DTR	1	This bit controls the Data Terminal Ready ($\overline{DTR}$) output. When bit 0 is set to a logic 1, the $\overline{DTR}$ output is forced to a logic 0. When bit 0 is reset to a logic 0, the $\overline{DTR}$ output is forced to a logic 1.
D1	RTS	1	This bit controls the Request to Send ($\overline{RTS}$) output. When bit 1 is set to a logic 1, the $\overline{RTS}$ output is forced to a logic 0. When bit 1 is reset to a logic 0, the $\overline{RTS}$ output is forced to a logic 1.
D2	µPRST* (OUT1 in 16C450)	1	In single-port mode inactive unless loop = 1, then functions as below (D4). In dual-port mode the µPRST pin is the logical OR of this bit and the RESET pin.
D3	Enable !nterrupt (OUT2 in 16C450)	0	Sets INTRPT pin to high impedance if STNDLN = 1.
		1	INTRPT output enabled.
D4	LOOP	1	This bit provides a local loopback feature for diagnostic testing of the UART portion of the SSI 73K222U. When bit D4 is set to logic 1, the following occurs: 1. TXD is forced to mark, RXD is ignored. 2. The output of the Transmitter is looped to the Receiver. 3. The four modem control inputs to the UART ($\overline{CTS}$, $\overline{DSR}$, $\overline{DCD}$, and $\overline{RI}$) are ignored and the UART signals $\overline{RTS}$, $\overline{DTR}$, Enable Interrupt, and µPRST are forced inactive. 4. The UART signals RTS, DTR, Enable Interrupt, and µPRST are internally connected to the four control signals CTS, DSR, DCD and RI respectively. Note that the Modem Status Register Interrupts are now controlled by the lower four bits of the Modem Control Register. The interrupts are still controlled by the Interrupt Enable Register.
D5 - D7		0	These bits are permanently set to logic 0.

* Note: The µPRST bit has an upgraded function which was not included in the initial definition of the SSI 73K222U.

LINE STATUS REGISTER (LSR) **UART SECTION**

STNDLN:	**0**	**1**
ADDRESS:	**UA2 - UA0 = 101**	**UA3 - UA0 = 0101**

This register provides status information to the CPU concerning the data transfer.

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	DR	1	The Data Ready (DR) bit is set to a 1 whenever a complete incoming character has been received and transferred into the Receiver Buffer Register. Data Ready is reset to 0 by reading the data in the Receiver Buffer Register or by writing a 0 into it from the processor.
D1	OE	1	The Overrun Error (OE) bit indicates that the data in the Receiver Buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer Register, thereby destroying the previous character. The OE indicator is reset whenever the CPU reads the contents of the Line Status Register.
D2	PE	1	The Parity Error (PE) bit indicates that the received character did not have the correct parity. The bit is reset to 0 whenever the CPU reads the Line Status Register.
D3	FE	1	The Framing Error (FE) bit indicates that the received character did not have a valid stop bit. The FE indicator is reset whenever the CPU reads the contents of the Line Status Register. A framing error will not occur in DPSK receive from the modem due to the fact that missing stop bits are reinserted.
D4	BI	1	The Break Interrupt (BI) bit indicates that a break has been received. A break occurs whenever the received data is held to 0 for a full data word (start + data + stop) or for two full data words when receiving in DPSK mode from the modem. The BI bit is reset to 0 whenever the CPU reads the Line Status Register.
D5	THRE	1	The Transmit Holding Register Empty (THRE) indicates that the Transmitter is ready to accept a new character for transmission. The THRE bit is reset when the CPU loads a character into the Transmit Holding Register.
D6	TSRE	1	The Transmit Shift Empty (TSRE) indicates that both the Transmit Holding Register and the Transmit Shift Registers are empty.
D7	-	0	Always zero.

MODEM STATUS REGISTER (MSR) (READ ONLY)

STNDLN:	**0**	**1**
ADDRESS:	**UA2 - UA0 = 110**	**UA3 - UA0 = 0110**

This register provides the current state of the control signals from the modem. In addition, four bits provide change information. The CTS, DSR, DCD, and RI signals come from the UART Control Register if STNDLN = 0 and from the $\overline{CTS}$, $\overline{DSR}$, $\overline{DCD}$ and $\overline{RI}$ pins (inverted) if STNDLN = 1. This register is READ ONLY. The delta bits indicate whether the inputs have changed since the last time the Modem Status Register has been read. In Loop Mode CTS, DSR, RI and DCD are taken from RTS, DTR, µPRST, and Enable Interrupt in the Modem Control Register respectively.

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	DCTS	1	This bit is the Delta Clear to Send (DCTS) indicator. Bit 0 indicates that the $\overline{CTS}$ input to the chip has changed state since the last time it was read by the CPU.
D1	DDSR	1	This bit is the Delta Data Set Ready (DDSR) indicator. Bit 1 indicates that the $\overline{DSR}$ input to the chip has changed state since the last time it was read by the CPU.
D2	TERI	1	This bit is the Trailing Edge of the Ring Indicator (TERI) detector. Bit 2 indicates that the $\overline{RI}$ input to the chip has changed state.
D3	DDCD	1	This bit is the Delta Data Carrier Detect (DDCD) indicator. Bit 3 indicates that the $\overline{DCD}$ input to the chip has changed state.
D4	CTS	1	This bit is the complement of the Clear To Send ($\overline{CTS}$) input. If STNDLN = 0, this reflects the status of the UART Control Register bit. If bit 4 (loop) of the MCR is set to a 1, this bit is equivalent to RTS in the MCR.
D5	DSR	1	This bit is the complement of the Data Set Ready ($\overline{DSR}$) input. If STNDLN = 0, this reflects the status of the UART Control Register bit. If bit 4 of the MCR is set to a 1, this bit is the equivalent of DTR in the MCR.
D6	RI	1	This bit is the complement of the Ring Indicator ($\overline{RI}$) input. If STNDLN = 0, this reflects the status of the UART Control Register bit. If bit 4 of the MCR is set to a 1, this bit is equivalent to µPRST in the MCR.
D7	DCD	1	This bit is the complement of the Data Carrier Detect ($\overline{DCD}$) If STNDLN = 0, this reflects the status of the UART Control Register bit. If bit 4 of the MCR is set to a 1, this bit is equivalent to Enable Interrupt in the MCR.

UART SECTION

SCRATCH REGISTER (SCR)

STNDLN:	0	1
ADDRESS:	UA2 - UA0 = 111	UA3 - UA0 = 0111

The Scratch Register is a dual port register which can be simultaneously accessed through both the UART bus and the modem bus. This provides the possibility for the modem controller to communicate directly with the central CPU. Note that if both processors write the Scratch Register, the data stored will be from whichever processor last wrote the register.

DIVISOR LATCH (Least significant byte) (DLL)

STNDLN:	0	1
ADDRESS:	UA2 - UA0 = 000, DLAB = 1	UA3 - UA0 = 0000, DLAB = 1

DIVISOR LATCH (Most significant byte) (DLM)

STNDLN:	0	1
ADDRESS:	UA2 - UA0 = 001, DLAB = 1	UA3 - UA0 = 0001, DLAB = 1

DIVISOR LATCH VALUE VS. DATA RATE

The Divisor Latch is two 8-bit write only registers which control the rate of the programmable baud generator. The programmable baud generator generates an output clock by dividing an internal 1.8432MHz clock by the value stored in the divisor latch. This output clock has a value of 16X the data rate at which the modem will operate. This output clock is available at pin 21 under the control of bit 3 (D3) of the Modem Control Register 1. Upon loading either of the Divisor Latches the 16-bit device counter is immediately loaded, preventing long counts on initial load. The following table shows divisor values for common data rates.

DESIRED DATA RATE	DIVISOR USED FOR 16 x DATA RATE CLOCK	% ERROR GENERATED	DESIRED DATA RATE	DIVISOR USED FOR 16 x DATA RATE CLOCK	% ERROR GENERATED
50	2304		4800	24	
75	1536		7200	16	
110	1047		9600	12	
134.5	857	0.058	19200	6	
159	768		38400	3	
300	384		56000	2	2.86
600	192				
1200	96				
1800	64				
2000	58	0.69			
2400	48				
3600	32				

1. Data Rate valid for FSK transmission.
2. Data Rate valid for halfspeed DPSK transmission.
3. Data Rate valid for normal 1200BPS DPSK transmission.

MODEM REGISTER BIT DESCRIPTIONS

CONTROL REGISTER (CR0)
STNDLN: 0 1
ADDRESS: MA2 - MA0 = 000 UA3 - UA0 = 1000

BIT NO.	NAME	CONDITION		DESCRIPTION
D0	Answer/Originate	0		Selects Answer Mode (transmit in high band, receive in low band).
		1		Selects Originate Mode (transmit in low band, receive in high band).
D1	Transmit Enable	0		Disables transmit output at TXA.
		1		Enables transmit output at TXA. NOTE: Answer tone and DTMF TX control require Transmit Enable. If Transmit Enable is on, call progress and answer tone detector interrupts are masked.
D2, D3	Character Size 0, 1			These bits are read only. These bits represent the character size. The character size is determined by the UART Line Control Register and includes data, parity (if used), one start bit, and one stop bit.
		D3	D2	Character length
		0	0	8-bit character
		0	1	9-bit character
		1	0	10-bit character
		1	1	11-bit character
D4	Power ON			This bit controls the power down mode of the SSI 73K222U, the analog, and most digital portions of the chip. The digital interface is active during power down.
		0		Power down mode.
		1		Normal operation.
D5	Modulation Mode	0		DPSK
		1		FSK
D6	Reserved	0		Must be written as zero.
D7	Modulation Option	0		DPSK: 1200 bit/s
		1		600 bit/s
		0		FSK: 103 mode
		1		V.21 mode

CONTROL REGISTER (CR1)
STNDLN: 0 1
ADDRESS: MA2 - MA0 = 001 UA3 - UA0 = 1001

BIT NO.	NAME	CONDITION		DESCRIPTION
D0, D1	Test Mode	D1	D0	
		0	0	Selects normal operating mode.
		0	1	Analog Loopback Mode. Loops the transmitted analog signal back to the receiver, and causes the receiver to use the same center frequency as the Transmitter. To squelch the TXA pin, transmit enable bit must be forced low.
		1	0	Selects remote digital loopback. Received data is looped back to transmit data internally, and RXD is forced to a mark. Data in TXD is ignored.
		1	1	Selects half-duplex. Internally performs a logical AND of TXD and RXD to send to the UART receiver. Both transmit and receive characters will occur at the Receiver Buffer Register.
D2	Reset	0		Selects normal operation.
		1		Resets modem to power down state. All Control Register bits (CR0, CR1, TONE) are reset to zero. The output of the clock pin will be set to the crystal frequency.
D3	CLK Control (Clock Control)	0		CLK pin output is selected to be an 11.0592 MHz crystal echo output.
		1		CLK pin output is selected to be 16 x the Data Rate set by the UART divisor latch.
D4	Bypass Scrambler	0		Selects normal operation. DPSK data is passed through scrambler.
		1		Selects Scrambler Bypass. DPSK data is routed around scrambler in the transmit path.

CONTROL REGISTER (CR1) (Continued)

BIT NO.	NAME	CONDITION		DESCRIPTION
D5	Enable Detect Interrupt	0		Disables interrupts generated by Detect Register bits D1 - D4 at INT pin in dual-port mode, or at INTRPT pin in single-port mode. All interrupts normally disabled in power down modes.
		1		Enables interrupts generated by Detect Register bits D1 - D4 at $\overline{INT}$ pin in dual-port mode, or at INTRPT pin in single-port mode. An interrupt will be generated with a change in status of DR bits D1 - D4. The answer tone and call progress detect interrupts are masked when the TX enable bit is set. Carrier detect is masked when TX DTMF is activated. All interrupts will be disabled if the device is in power down mode. The interrupt is reset when the DR register is read.
D6, D7	Transmit Pattern	D7	D6	
		0	0	Selects normal data transmission as controlled by the state of the TXD pin.
		0	1	Selects an alternating mark/space transmit pattern for modem testing.
		1	0	Selects a constant mark transmit pattern.
		1	1	Selects a constant space transmit pattern.

DETECT REGISTER (DR)
STNDLN: 0 1
ADDRESS: MA2 - MA0 = 010 UA3 - UA0 = 1010

BIT NO.	NAME	CONDITION		DESCRIPTION
D0	Long Loop	0		Indicates normal received signal.
		1		Indicates low received signal level (< -38 dBm).
D1	Call Progress Detect	0		No call progress tone detected.
		1		Indicates presence of call progress tones. The call progress detection circuitry is activated by energy in the normal 350 to 620 Hz call progress bandwidth.
D2	Answer Tone Received	0		No answer tone detected.
		1		Indicates detection of 2225 Hz answer tone in Bell mode or 2100 Hz in CCITT mode. The device must be in Originate Mode for detection of answer tone for normal operation. For CCITT answer tone detection, bit D0 of the Tone Register must be set.
D3	Carrier Detect	0		No carrier detected in the receive channel.
		1		Carrier has been detected in the receive channel.
D4	Unscrambled Marks	0		No unscrambled mark detected.
		1		Indicates detection of unscrambled marks in the received data. A valid indication requires that unscrambled marks be received for > 165.5 ± 13.5 ms.
D5	Receive Data			Continuously outputs the received data stream. This data is the same as that output on the RXD pin, but it is not disabled when RXD is tri-stated.
D6, D7	Device Signature 0, 1	D7	D6	Product Identified
		0	0	SSI 73K212U
		0	1	SSI 73K221U
		1	0	SSI 73K222U

TONE CONTROL REGISTER (TONE)

STNDLN:	**0**	**1**
ADDRESS:	**MA2 - MA0 = 011**	**UA3 - UA0 = 1011**

The Tone Control Register contains information on the tones that are transmitted. Tones are transmitted only if the Transmit Enable bit is set. The priority of the transmit tones are: 1) DTMF, 2) Answer, 3) FSK, 4) Guard.

BIT NO.	NAME	CONDITION				DESCRIPTION
D0	DTMF 0 / Answer/ Guard Tone	D6	D5	D4	D0	D0 interacts with bits D6, D5, and D4 as shown:
		X	X	1	X	Transmit DTMF tones.
		X	1	0	0	Select 2225Hz answer tone (Bell).
		X	1	0	1	Select 2100Hz answer tone (CCITT).
		1	0	0	0	Select 1800Hz guard tone.
		1	0	0	1	Select 550Hz guard tone.
D0, D1, D2, D3	DTMF	Table below				Programs 1 of 16 DTMF tone pairs that will be transmitted when TX DTMF and TX enable bit (CR0, bit D1) is set. Tone encoding is shown below.

KEYBOARD EQUIVALENT	DTMF CODE D3	D2	D1	D0	TONES LOW	HIGH
1	0	0	0	1	697	1209
2	0	0	1	0	697	1336
3	0	0	1	1	697	1477
4	0	1	0	0	770	1209
5	0	1	0	1	770	1336
6	0	1	1	0	770	1477
7	0	1	1	1	852	1209
8	1	0	0	0	852	1336
9	1	0	0	1	852	1477
0	1	0	1	0	941	1336
*	1	0	1	1	941	1209
#	1	1	0	0	941	1477
A	1	1	0	1	697	1633
B	1	1	1	0	770	1633
C	1	1	1	1	852	1633
D	0	0	0	0	941	1633

TONE CONTROL REGISTER (TONE) (Continued)

D4	TX DTMF (Transmit DTMF)	0		Disable DTMF.
		1		Activates DTMF. The selected DTMF tones are transmitted continuously when this bit is high. TX DTMF overrides all other transmit functions.
D5	TX ANS (Transmit Answer Tone)	D5	D0	D5 interacts with bit D0 as shown.
		0	X	Disables answer tone generator.
		1	0	Enables answer tone generator. A 2225Hz answer tone will be transmitted continuously when the transmit enable bit is set. The device must be in answer mode.
		1	1	Enables a 2100Hz answer tone generator, with operation same as above.
D6	TX Guard (Transmit Guard Tone)	0		Disables guard tone generator.
		1		Enables guard tone generator. (See D0 for selection of guard tones).
D7	RXD/TXD Control	STNDLN	D7	Function is dependant on status of STNDLN pin.
		0	0	RXD is output data received by modem, TXD is serial output of UART.
		1	0	RXD is electrically an input, but the signal is ignored, TXD is forced to a mark.
		X	1	RXD is serial input to UART, TXD is serial output of UART.

CONTROL REGISTER (CR3)
STNDLN: 0 1
ADDRESS: MA2 - MA0 = 101 UA3 - UA0 = 1101

BIT NO.	NAME	CONDITION		DESCRIPTION
D0 - D4	Not Used			Not presently used.
D5	Off Hook	0		Relay driver open.
		1		Open drain driver pulling low.
D6, D7	Speaker Volume 0, 1	D7	D6	Speaker volume control status.
		0	0	Speaker off
		0	1	-24dB
		1	0	-12dB
		1	1	0dB

SCRATCH REGISTER (SCR)

STNDLN:	**0**	**1**
ADDRESS:	**MA2 - MA0 = 110**	**UA3 - UA0 = 1110**

The Scratch Register is a dual-port register which can be accessed either through the UART bus or the modem bus. It can be used for a communication path outside the data stream.

UART CONTROL REGISTER (UCR)

STNDLN:	**0**	**1**
ADDRESS:	**MA2 - MA0 = 111**	**UA3 - UA0 = 1111**

The UART Control Register contains the handshaking signals necessary for the microprocessor to communicate with the central CPU through the UART.

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	CTS	1	In dual-port mode, CTS, DSR, DCD and RI are writeable locations which can be read through the 16C450 port in the Modem Status Register.
D1	DSR	1	
D2	DCD	1	In the single-port mode, D0 - D3 are ignored and the information for the Modem Status Register comes directly from the external pins.
D3	RI	1	
D4	DTR	1	
D5	RTS	1	DTR and RTS are read only versions of the same register bits in the Modem Contol Register.
D6	Not Used		
D7	TXCLK	Clock	TXCLK is the clock that the UART puts out with TXD. The falling edge of TXCLK is coincident with the transitions of data on TXD. TXCLK can also be used for the microprocessor to send synchronous data independent of the UART by forcing data patterns using CR1 bits 6 and 7 before the rising edge of TXCLK.
NOTE: Control Register 2 (CR2) is reserved for future products and is disabled.			

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

TA = -40°C to 85°C, VDD = 5V ± 10%, unless otherwise noted.

PARAMETER	RATING	UNIT
VDD Supply Voltage	7	V
Storage Temperature	-65 to 150	°C
Soldering Temperature (10 sec.)	260	°C
Applied Voltage	-0.3 to VDD +0.3	V
NOTE: All inputs and outputs are protected from static charge using built-in, industry standard protection devices and all outputs are short-circuit protected.		

RECOMMENDED OPERATING CONDITIONS

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNIT
VDD, Supply Voltage		4.5	5	5.5	V
TA, Operating Free-Air Temperature		-40		85	°C
External Component (Refer to application drawing for placement.)					
VREF Bypass Capacitor[1]	(VREF to GND)	0.1			µF
Bias Setting Resistor[1]	(Placed between VDD and ISET pins)	1.8	2	2.2	MΩ
ISET Bypass Capacitor[1]	ISET pin to GND	0.1			µF
VDD Bypass Capacitor[1]	(VDD to GND)	0.1			µF
Input Clock Variation	(11.0592 MHz)	-0.01		+0.01	%

1. Optional for minimum worst case current consumption.
2. Minimum for optimized system layout; may require higher values for noisy environments.

DC ELECTRICAL CHARACTERISTICS

TA = -40°C to +85 °C, VDD = 5V ± 10%, unless otherwise noted.

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNIT
IDD, Supply Current					
IDDA, Active	ISET Resistor = 2MΩ		8	12	mA
IDDA, Active	ISET = GND		8	15	mA
IDD1, Power-Down	CLK = 11.0592MHz		3	4	mA
IDD2, Power-Down	CLK = 19.200KHz		2	3	mA
Digital Inputs					
Input High Current IIH	VI = VDD			100	µA
Input Low Current IIL	VI = 0	-200			µA
Input Low Voltage VIL				0.8	V
Input High Voltage VIH	Except RESET & XTAL 1	2.0			V
Input High Voltage VIH	RESET & XTAL 1	3.0			V
Pull Down Current RESET PIN		5		30	µA
Input Capacitance				10	pF
Digital Outputs					
Output High Voltage VOH	IOUT = - 1 mA	2.4		VDD	V
VOL UD0-UD7 and INTRPT	IOUT = 3.2 mA			.4	V
VOL other outputs	IOUT = 1.6 mA			.4	V
CLK Output VOL	IOUT = 3.2 mA			0.6	V
OH Output VOL	IOUT = 20 mA			1.0	V
OH Output VOL	IOUT = 10 mA			0.5	V
Offstate Current INTRPT pin	VO = 0V	-20		20	µA
Analog Pins					
RXA Input Resistance			200		KΩ
RXA Input Capacitance				25	pF

DYNAMIC CHARACTERISTICS AND TIMING
TA = -40°C to +85°C, VDD = 5V ± 10%, unless otherwise noted.

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNIT
DPSK Modulator					
Carrier Suppression	Measured at TXA	55			dB
Output Amplitude	ANS TONE 2225 or 2100 Hz	-11	-10.0	-9	dBm0
	DPSK TX Scrambled Marks	-11	-10.0	-9	dBm0
	FSK Dotting Pattern	-11	-10.0	-9	dBm0
FSK Tone Error	Bell 103 or V.21			±5	Hz
DTMF Generator					
Freq. Accuracy		-.25		.25	%
Output Amplitude	Low Band	-10	-9	-8	dBm0
Output Amplitude	High Band	-8	-7	-6	dBm0
Long Loop Detect	DPSK or FSK	-40		-32	dBm0
Demodulator Dynamic Range	DPSK or FSK		45		dB
Call Progress Detector					
Detect Level	2-Tones in 350-600Hz Band	-39		0	dBm0
Reject Level	2-Tones in 350-600Hz Band			-46	dBm0
Delay Time	-70dBm0 to -30dBm0 Step	27		80	ms
Hold Time	-30dBm0 to -70dBm0 Step	27		80	ms
Hysteresis		2			dB
Carrier Detect	DPSK or FSK Receive				
Threshold	Data	-49		-42	dBm0
Delay Time	-70 dBm0 to -30 dBm0 Step	15		45	ms
Hysteresis		2	3.0		dB
Hold Time	-30 dBm0 to -70 dBm0 Step	10		24	ms
Answer Tone Detector					
Detect Level Threshold	In FSK mode	-49.5		-42	dBm0
Delay Time	-70dBm0 to -30dBm0 STEP	20		45	ms
Hold Time	-30dBm0 to -70dBm0 STEP	10		30	ms
Detect Frequency Range		-2.5		+2.5	%

1. All units in dBm0 are measured at the line input to the transformer. The interface circuit inserts an 8 dB loss in the transmit path (TXA1 - TXA2 to line), and a 3dB loss in the receive path (line to RXA).

DYNAMIC CHARACTERISTICS AND TIMING (Continued)

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNIT
Hybrid Loading					
R1	See Figure 3		600		Ω
R2			600		Ω
C	TXA Hybrid Loading	.02		.033	µF
Speaker Output					
Gain Error		-1		+1	dB
Output Swing SPKR	10K||50pF LOAD 5% THD	2.75			VP
Carrier VCO					
Capture Range	Originate or Answer	-10		10	Hz
Capture Time	-10Hz to +10Hz Carrier Frequency change assumed		40	100	ms
Recovered Clock					
Capture Range	% of Center Frequency	-625		+625	ppm
Data Delay Time	Analog data in at RXA pin to receive data valid at RXD pin.		30	50	ms
Guard Tone Generator					
Tone Accuracy	550 or 1800Hz	-20		+20	Hz
Tone Level	550HZ	-4.0	-3.0	-2.0	dB
(Below DPSK Output)	1800HZ	-7.0	-6.0	-5.0	dB
Harmonic Distortion	700 to 2900HZ			-60	dB
Capacitance					
Inputs				10	pF
XTAL1, XTAL2			30		pF
CLK				15	pF

SERIAL BUS INTERFACE (See Figure 4)
The following times are for CL = 100pF.

PARAMETER		MIN	NOM	MAX	UNIT
TRD	Data out from Read	0		140	ns
TCKD	Data out after Clock			200	ns
TRDF	Data Float after Read	0		200	ns
TRCK	Clock High after Read	200			ns
TWW	Write Width	140		10000	ns
TDCK	Data Setup Before Clock	150			ns

SERIAL BUS INTERFACE (Continued)

TCKD	Data Hold after Clock	20			ns
TCKW	Write after Clock	150			ns
TACR	Address setup before Control	50			ns
TCAR	Address Hold after Control	50			ns
TACW	Address setup before Write	50			ns
TCAW	Address Hold after Write	50			ns
1. Control is later of falling edge of RD or DCLK.					

PARALLEL BUS INTERFACE (See Figure 5) The following times are for Cl = 100pF.

PARAMETER		MIN	MAX	MIN	MAX	UNIT
		Dual-Port Mode		Single-Port Mode		
RC	Read Cycle = TAD + TRC	240		340		ns
TDIW	DISTR Width	80		80		ns
TDDD	Delay DISTR to Data (read time)		80		80	ns
THZ	DISTR to Floating Data Delay	0	50	0	50	ns
TRA	Address Hold after DISTR	20		20		ns
TRCS	Chip select hold after DISTR	20		20		ns
TAR	DISTR Delay after Address	20		20		ns
TCSR	DISTR Delay after Chip Select	20		20		ns
WC	Write Cycle = TAW + TDOW + TWC	140		140		ns
TDOW	DOSTR Width	80		80		ns
TDS	Data Setup	30		50		ns
TDH	Data Hold	20		20		ns
TWA	Address Hold after DOSTR	20		20		ns
TWCS	Chip select hold after DOSTR	20		20		ns
TAW	DOSTR delay after Address	20		20		ns
TCSW	DOSTR delay after Chip Select	20		20		ns
TADS	Address Strobe Width			40		ns
TAS	Address Setup Time			30		ns
TAH	Address Hold Time			0		ns
TCS	Chip Select Setup Time			30		ns
TCH	Chip Select Hold Time			0		ns
TRC	Read Cycle Delay	40		40		ns
TWC	Write Cycle Delay	40		40		ns
TAD	Address to Read Data	200		300		ns

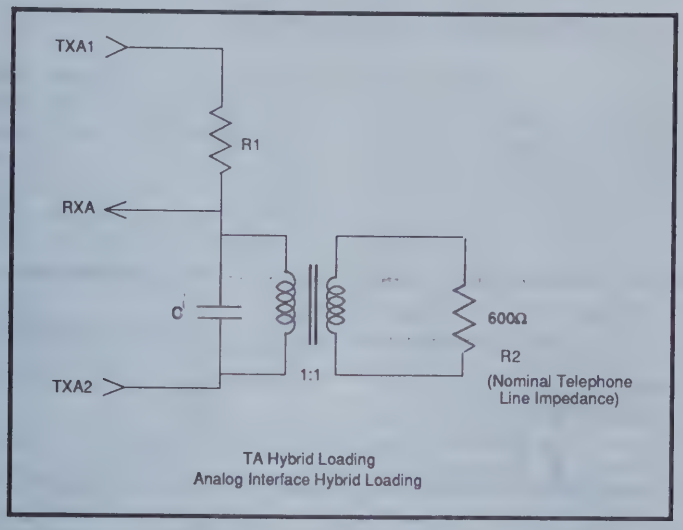


FIGURE 3: TXA Hybrid Loading Analog Interface Hybrid Loading

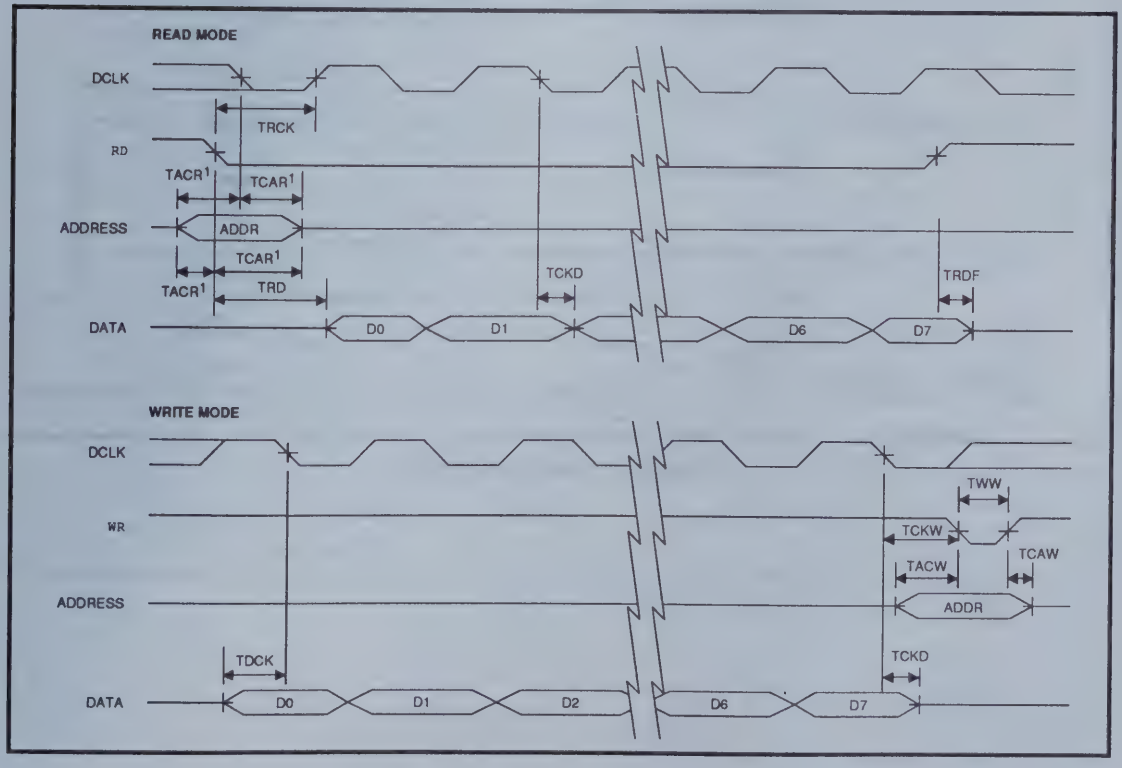


FIGURE 4: Modem Serial Bus Timing

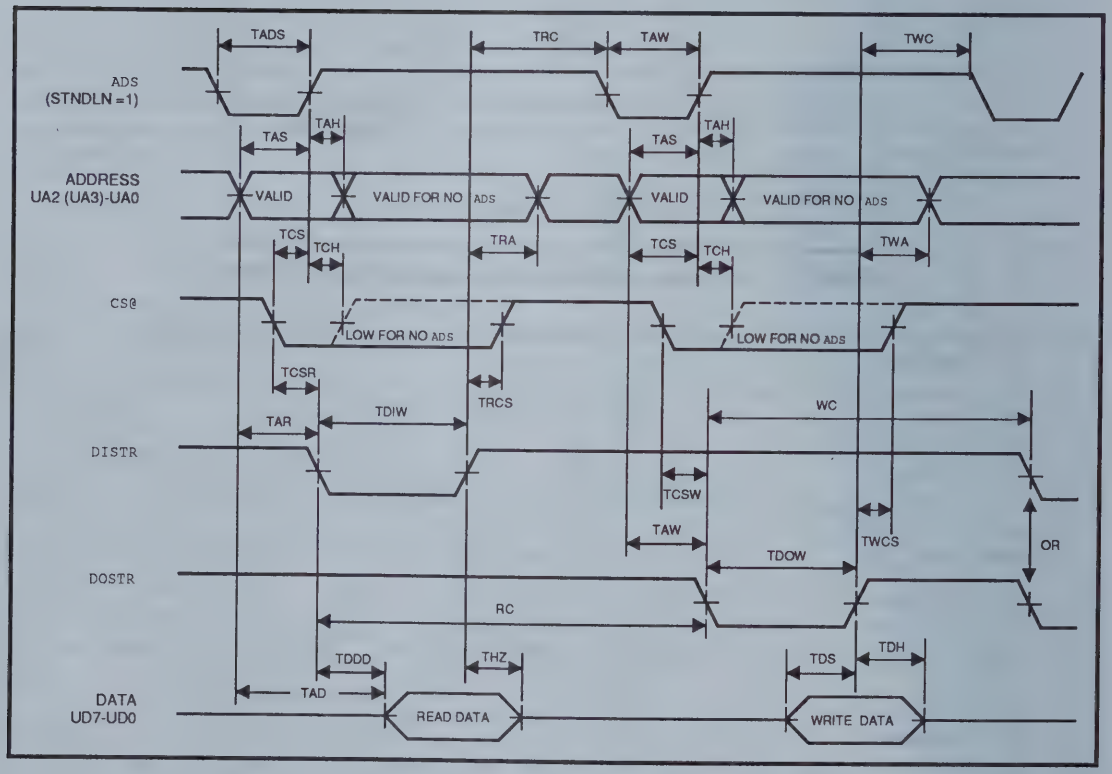


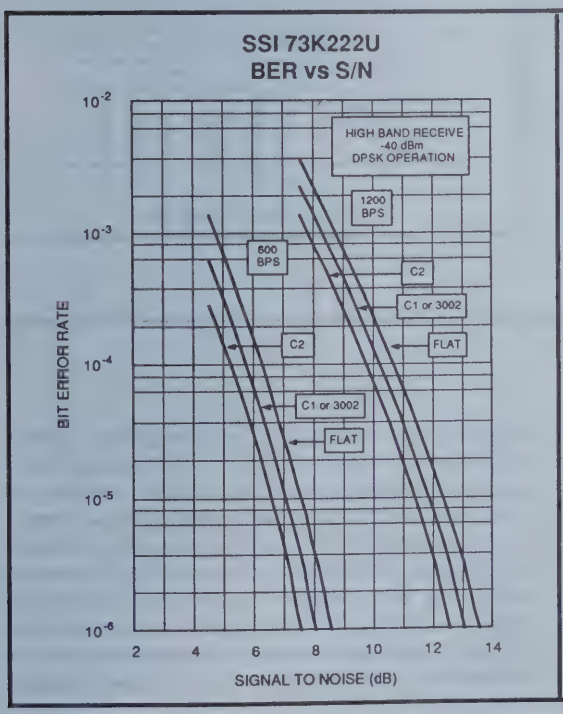
FIGURE 5: UART Bus Timing

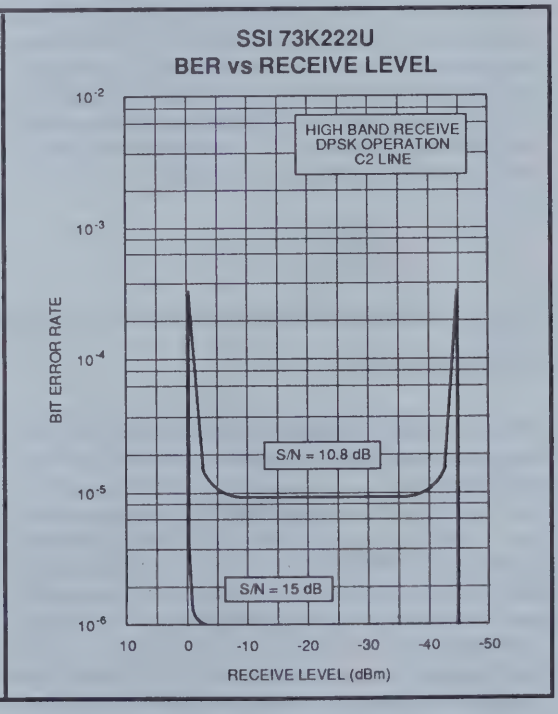
TYPICAL PERFORMANCE CHARACTERISTICS

The SSI 73K222U was designed using an integrated analog/digital architecture that offers optimum performance over a wide range of line conditions. The SSI 73K222U utilizes the circuit design proven in SSI's 73K222L one-chip modem, with added enhancements which extend low signal level performance and increase immunity to spurious noise typically encountered in integral bus applications. The SSI 73K222U provides excellent immunity to the types of disturbances present with usage of the dial-up telephone network. The following curves show representative Bit Error Rate performance under various line conditions.

BER vs S/N

This test measures the ability of the modem to function with minimum errors when operating over noisy lines. Since some noise is generated by even the best dial-up lines, the modem must operate with as low a S/N ratio as possible. Optimum performance is shown by curves that are closest to the zero axis. A narrow spread between curves for the four line conditions indicates minimal variation in performance when operating over a range of line qualities and is typical of high performance adaptive equalization receivers. High band receive data is typically better than low band due to the inherent design of PSK modems.



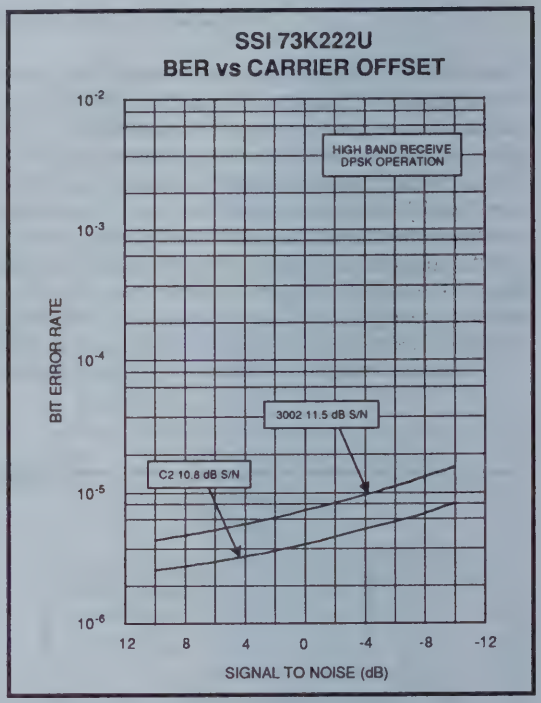


BER vs Receive Level

This measures the dynamic range of the modem. As signal levels vary widely over dial-up lines, the widest dynamic range possible is desirable. The minimum Bell specification calls for 36dB of dynamic range. S/N ratios were held constant at the indicated values while receive level was lowered from very high to very low signal levels. The "width of the bowl" of these curves taken at the 10^{-3} BER point is a measure of the dynamic range.

BER vs Carrier Offset

This parameter indicates how the modem performance is impacted by frequency shifts encountered in normal PSTN operation. Flat curves show no performance degradation from frequency offsets. The SSI K-Series devices use a 2nd order carrier tracking phase-locked-loop, which is insensitive to carrier offsets in excess of 10Hz. The Bell network specifications allow as much as 7Hz offset, and the CCITT specifications require modems to operate with 7Hz of offset.



APPLICATION

The SSI 73K222U includes additional circuitry to greatly simplify integral modem designs in either of two different configurations. The single-port mode represents the most efficient implementation for an integral modem. Figure 9 shows a typical schematic using this mode. In this configuration, the SSI 73K222U transfers data and commands through the single parallel port. All modem control is provided by the main CPU, eliminating the need for an external microcontroller and supporting components. The SSI 73K222U is unique in that access to both the UART and modem sections is possible through the UART port. Also shown is a separate serial port, which can be used independent of the modem function when the modem section is inactive. Figure 10 shows a more conventional integral modem design, in which a local microprocessor handles modem supervision, allowing the modem function to be transparent to the main processor. Inclusion of the hybrid drivers, audio volume control, and off hook relay driver reduces component count for a highly efficient design. In either mode of operation, the SSI 73K222U's ability to operate from a single +5 volt power supply eliminates the need for additional supply voltages and keeps power usage to a minimum.

(See Figure 9 & 10: Typical Integral Applications Single and Dual-Port Modes.)

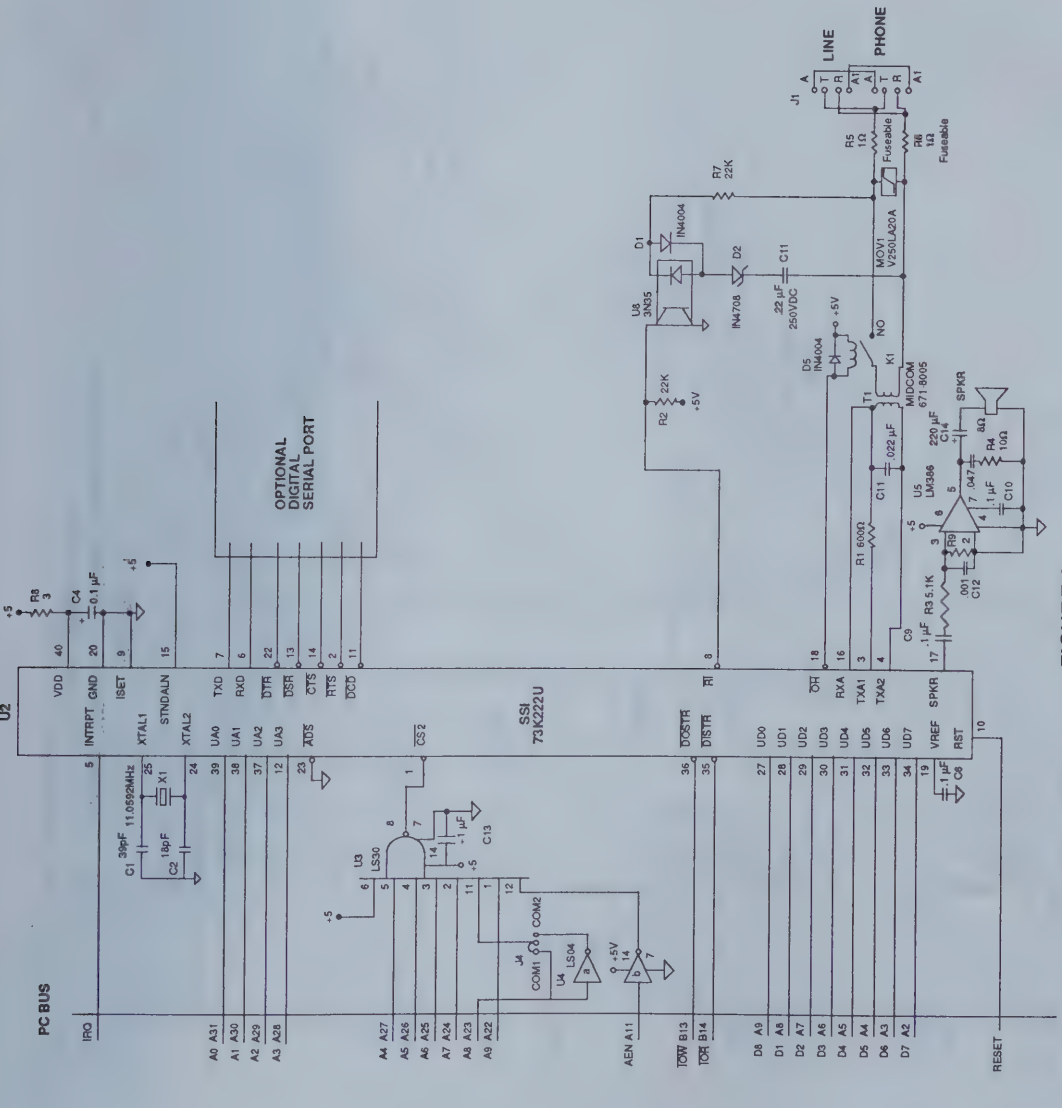


FIGURE 9
73K222U TYPICAL INTEGRAL APPLICATION
SINGLE-PORT MODE

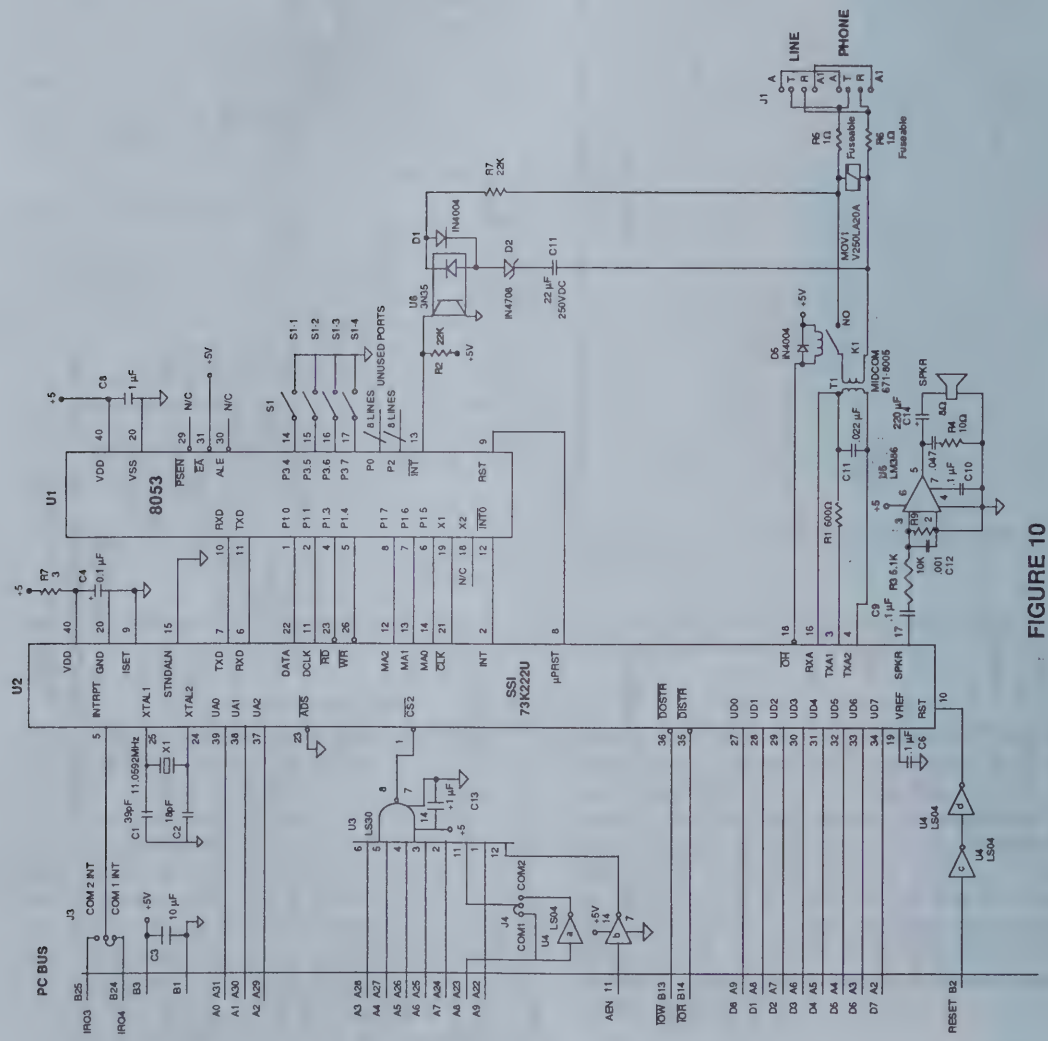
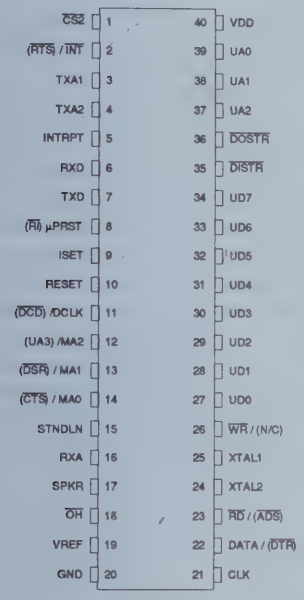


FIGURE 10
73K222U TYPICAL INTEGRAL APPLICATION
DUAL-PORT MODE

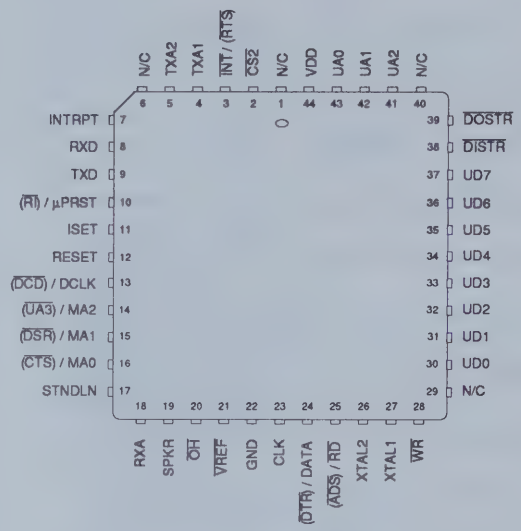
PACKAGE PIN DESIGNATIONS

(TOP VIEW)



600-Mil
40-Pin DIP

Parentheses indicate single-port mode.



44-Lead
PLCC

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 73K222U		
40-Pin Plastic Dual-In-Line	SSI 73K222U – IP	SSI 73K222U – IP
44-Pin Plastic Leaded Chip Carrier	SSI 73K222U – IH	SSI 73K222U – IH

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NOTES:

SSI 73K224L
V.22 bis/V.22/V.21, Bell 212A/103 Single-Chip Modem

July, 1989

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DESCRIPTION

The SSI 73K224L is a highly integrated single-chip modem IC which provides the functions needed to construct a V.22 bis compatible modem, capable of 2400 bit/s full-duplex operation over dial-up lines. The SSI 73K224L offers excellent performance and a high level of functional integration in a single 28-pin DIP. This device supports V.22 bis, V.22, V.21, Bell 212A and Bell 103 modes of operation, allowing both synchronous and asynchronous communication. The SSI 73K224L is designed to appear to the systems designer as a microprocessor peripheral, and will easily interface with popular single-chip microprocessors (80C51 typical) for control of modem functions through its 8-bit multiplexed address/data bus or via an optional serial command bus. An ALE control line simplifies address demultiplexing. Data communications normally occur through a separate serial port. The SSI 73K224L is pin and software compatible with the SSI 73K212L and SSI 73K222L single-chip modem ICs, allowing system upgrades with a single component change.

The SSI 73K224L operates from a single +5 volt supply for low power consumption.

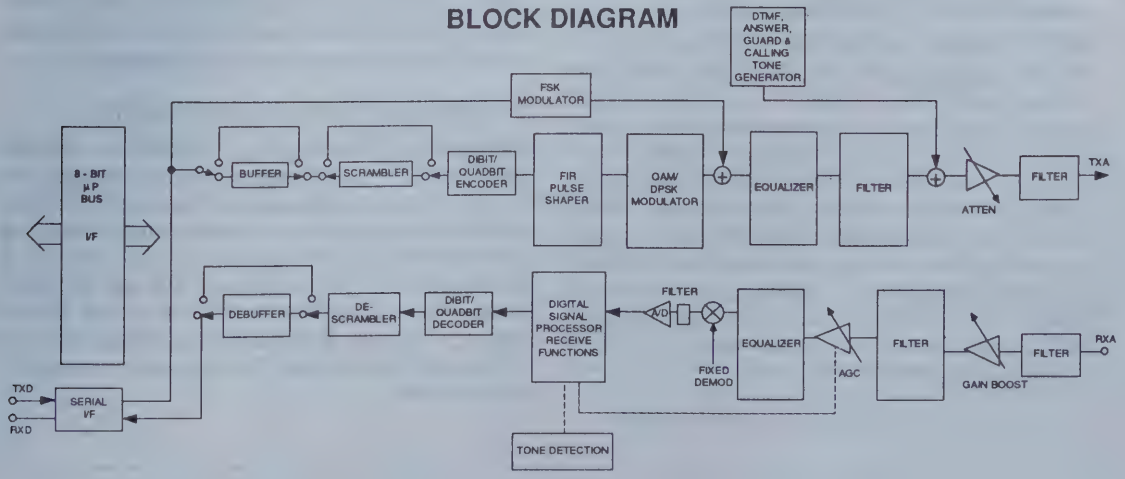
The SSI 73K224L is ideal for use in either free-standing or integral system modem products where full-duplex

(Continued)

FEATURES

- One-chip multi-mode V.22 bis/V.22/V.21 and Bell 212A/103 compatible modem
- FSK (300 bit/s), DPSK (600, 1200 bit/s), or QAM (2400 bit/s) encoding
- Pin and software compatible with other SSI K–Series 1-chip modems
- Interfaces directly with standard microprocessors (8048, 80C51 typical)
- Parallel microprocessor bus (28-pin DIP, 44-pin quad) for control
- Selectable asynch/synch with internal buffer/debuffer and scrambler/descrambler functions
- All synchronous and asynchronous operating modes (internal, external, slave)
- Adaptive equalization for optimum performance over all lines
- Programmable transmit attenuation (15 dB, 1 dB steps), selectable receive boost (+12 dB)
- Call progress, carrier, answer tone, unscrambled mark, S1, and signal quality monitors
- DTMF, answer and guard tone generators
- Test modes available: ALB, DL, RDL, Mark, Space, Alternating bit, S1 pattern
- CMOS technology for low power consumption (125 mW @ 5V) with power-down mode (30 mW @ 5V)
- TTL and CMOS compatible inputs and outputs

BLOCK DIAGRAM



DESCRIPTION (Continued)

2400 bit/s data communications over the 2–wire switched telephone network is desired. Its high functionality, low power consumption, and efficient packaging simplify design requirements and increase system reliability. A complete modem requires only the addition of the phone line interface, a control microprocessor, and RS–232 level converters for a typical system.

OPERATION

The SSI 73K224L is designed to be a complete V.22 bis compatible modem on a chip. The complete modem requires only the addition of the phone line interface, a control microprocessor, and RS-232 level converter for a typical system. Many functions were included to simplify implementation of typical modem designs. In addition to the basic 2400 bit/s QAM, 600/1200 bit/s DPSK and 300 bit/s FSK modulator/demodulator sections, the device also includes SYNCH/ASYNCH converters, scrambler/descrambler, call progress tone detect, DTMF tone generator capabilities and handshake pattern detectors. V.22 bis, V.22, V.21 and Bell 212A/103 modes are supported (synchronous and asynchronous) and test modes are provided for diagnostics. Most functions are selectable as options and logical defaults are provided when override modes are chosen. The device can be directly interfaced to a microprocessor via its 8-bit multiplexed address/data bus for control and status monitoring. Data-communication takes place through a separate serial port.

QAM MODULATOR/DEMODULATOR

The SSI 73K224L encodes incoming data into quadbits represented by 16 possible signal points with specific phase and amplitude levels. The baseband signal is then filtered to reduce intersymbol interference on the bandlimited telephone network. The modulator transmits this encoded data using either a 1200 Hz (originate mode) or 2400 Hz (answer mode) carrier. The demodulator, although more complex, essentially reverses this procedure while also recovering the data clock from the incoming signal. Adaptive equalization corrects for varying line conditions by automatically changing filter parameters to compensate for line characteristics.

DPSK MODULATOR/DEMODULATOR

The SSI 73K224L modulates a serial bit stream into di–bit pairs that are represented by four possible phase shifts as prescribed by the Bell 212A/V.22 standards. The base-band signal is then filtered to reduce intersymbol interference on the bandlimited 2-wire PSTN line. Transmission occurs on either a 1200 Hz (originate mode) or 2400 Hz carrier (answer mode). Demodulation is the reverse of the modulation process, with the incoming analog signal eventually decoded into di-bits and converted back to a serial bit stream. The demodulator also recovers the clock which was encoded into the analog signal during modulation. Demodulation occurs using either a 1200 Hz carrier (answer mode or ALB originate mode) or a 2400 Hz carrier (originate mode or ALB answer mode). The SSI 73K224L uses a phase locked loop coherent demodulation technique that offers inherently better performance than typical DPSK demodulators used by other manufacturers. Adaptive equalization is also used in DPSK modes for optimum operation with varying line conditions.

FSK MODULATOR/DEMODULATOR

The FSK modulator produces a frequency modulated analog output signal using two discrete frequencies to represent the binary data. The Bell 103 standard frequencies of 1270 and 1070 Hz (originate mark and space) and 2225 and 2025 Hz (answer mark and space) are used when this mode is selected. V.21 mode uses 980 and 1180 Hz (originate, mark and space) or 1650 and 1850 Hz (answer, mark and space). Demodulation involves detecting the received frequencies and decoding them into the appropriate binary value. The rate converter and scrambler/descrambler are bypassed in the FSK modes.

PASSBAND FILTERS AND EQUALIZERS

High and low band filters are included to shape the amplitude and phase response of the transmit and receive signals and provide compromise delay equalization and rejection of out-of-band signals. Amplitude and phase equalization are necessary to compensate for distortion of the transmission line and to reduce intersymbol interference in the bandlimited receive signal. The transmit signal filtering corresponds to a 75% square root of raised Cosine frequency response characteristic.

ASYNCHRONOUS MODE

The asynchronous mode is used for communication with asynchronous terminals which may communicate at 600,1200, or 2400 bit/s +1%, -2.5% even though the modem's output is limited to the nominal bit rate ±.01%. When transmitting in this mode the serial data on the TXD input is passed through a rate converter which inserts or deletes stop bits in the serial bit stream in order to output a signal that is the nominal bit rate ±.01%. This signal is then routed to a data scrambler and into the analog modulator where quad-bit/di-bit encoding results in the output signal. Both the rate converter and scrambler can be bypassed for handshaking, FSK, and synchronous operation as selected. The device recognizes a break signal and handles it in accordance with Bell 212A specifications. Received data is processed in a similar fashion except that the rate converter now acts to reinsert any deleted stop bits and output data to the terminal at no greater than the bit rate plus 1%. An incoming break signal (low through two characters) will be passed through without incorrectly inserting a stop bit.

The SYNC/ASYNC converter also has an extended overspeed mode which allows selection of an output overspeed range of either +1% or +2.3%. In the overspeed mode, some stop bits are output at 7/8 the normal width.

Similar to the transmit side, both the SYNC/ASYNC rate converter and the data descrambler are bypassed in the FSK modes.

SYNCHRONOUS MODE

Synchronous operation is possible only in the QAM or DPSK modes. Operation is similar to that of the asynchronous mode except that data must be synchronized to a provided clock and no variation in data transfer rate is allowable. Serial input data appearing at TXD must be valid on the rising edge of TXCLK. TXCLK is an internally derived 1200 or 2400 Hz signal in internal mode and is connected internally to the RXCLK pin in slave mode. Receive data at the RXD pin is clocked out on the falling edge of RXCLK. The asynch/synch converter is bypassed when synchronous mode is selected and data is transmitted at the same rate as it is input.

PARALLEL BUS INTERFACE

Seven 8-bit registers are provided for control, option select, and status monitoring. These registers are addressed with the AD0, AD1, and AD2 multiplexed address lines (latched by ALE) and appear to a control microprocessor as seven consecutive memory locations. Five control registers are read/write memory. The status detect and ID registers are read only and cannot be modified except by modem response to monitored parameters.

DTMF GENERATOR

The DTMF generator will output one of 16 standard dual-tones determined by a 4-bit binary value and the TX DTMF mode bit previously loaded into the tone register. Transmission of DTMF tones is initiated when the DTMF mode is selected and the transmit enable (CR0 bit D1) is changed from 0 to 1.

PIN DESCRIPTION

POWER

NAME	28-PIN	44-PIN	TYPE	DESCRIPTION
GND	28	44	I	System Ground.
VDD	15	23	I	Power supply input, 5V ±10%. Bypass with .1 and 22 µF capacitors to ground.
Vref	26	42	O	An internally generated reference voltage. Bypass with .1 µF capacitor to Ground.
Iset	24	36	I	Chip current reference. Sets bias current for op-amps. The chip current is set by connecting this pin to VDD through a 2 MΩ resistor. Iset should be bypassed to GND with a .1 µF capacitor.

PARALLEL MICROPROCESSOR INTERFACE

NAME	28-PIN	44-PIN	TYPE	DESCRIPTION
ALE	12	20	I	Address latch enable. The falling edge of ALE latches the address on AD0-AD2 and the chip select on $\overline{CS}$.
AD0-AD7	4-11	4,9-15	I/O	Address/data bus. These bidirectional tri-state multiplexed lines carry information to and from the internal registers.
$\overline{CS}$	20	32	I	Chip select. A low on this pin allows a read cycle or a write cycle to occur. AD0-AD7 will not be driven and no registers will be written if $\overline{CS}$ (latched) is not active. $\overline{CS}$ is latched on the falling edge of ALE.
CLK	1	1	O	Output clock. This pin is selectable under processor control to be either the crystal frequency (for use as a processor clock) or 16 x the data rate for use as a baud rate clock in QAM/DPSK modes only. The pin defaults to the crystal frequency on reset.
$\overline{INT}$	17	25	O	Interrupt. This open drain weak pullup, output signal is used to inform the processor that a detect flag has occurred. The processor must then read the detect register to determine which detect triggered the interrupt. $\overline{INT}$ will stay active until the processor reads the detect register or does a full reset.
$\overline{RD}$	14	22	I	Read. A "low" requests a read of the SSI 73K224L internal registers. Data cannot be output unless both $\overline{RD}$ and the latched $\overline{CS}$ are active or "low."
RESET	25	37	I	Reset. An active signal "high" on this pin will put the chip into an inactive state. All control register bits (CR0, CR1, CR2, CR3, Tone) will be reset. The output of the CLK pin will be set to the crystal frequency. An internal pull down resistor permits power on reset using a capacitor to VDD.
$\overline{WR}$	13	21	I	Write. A "low" on this informs the SSI 73K224L that data is available on AD0-AD7 for writing into an internal register. Data is latched on the rising edge of $\overline{WR}$. No data is written unless both $\overline{WR}$ and the latched $\overline{CS}$ are active ("low").
Note:	The serial control mode is provided in the 28-pin version by tying ALE high and $\overline{CS}$ low. In this configuration AD7 becomes DATA and AD0, AD1 and AD2 become A0, A1 and A2, respectively.			

RS-232 INTERFACE

NAME	28-PIN	44-PIN	TYPE	DESCRIPTION
EXCLK	19	31	I	External Clock. This signal is used in synchronous transmission when the external timing option has been selected. In the external timing mode the rising edge of EXCLK is used to strobe synchronous DPSK transmit data available on the TXD pin. Also used for serial control interface.
RXCLK	23	35	O	Receive Clock. The falling edge of this clock output is coincident with the transitions in the serial received data output. The rising edge of RXCLK can be used to latch the valid output data. RXCLK will be active as long as a carrier is present.
RXD	22	34	O	Received Digital Data Output. Serial receive data is available on this pin. The data is always valid on the rising edge of RXCLK when in synchronous mode. RXD will output constant marks if no carrier is detected.
TXCLK	18	26	O	Transmit Clock. This signal is used in synchronous transmission to latch serial input data on the TXD pin. Data must be provided so that valid data is available on the rising edge of the TXCLK. The transmit clock is derived from different sources depending upon the synchronization mode selection. In Internal Mode the clock is generated internally. In External Mode TXCLK is phase locked to the EXCLK pin. In Slave Mode TXCLK is phase locked to the RXCLK pin. TXCLK is always active.
TXD	21	33	I	Transmit Digital Data Input. Serial data for transmission is input on this pin. In synchronous modes, the data must be valid on the rising edge of the TXCLK clock. In asynchronous modes (2400/1200/600 bit/s or 300 baud) no clocking is necessary. DPSK data must be +1%, -2.5% or +2.3%, -2.5 % in overspeed mode.

ANALOG INTERFACE

RXA	27	43	I	Received modulated analog signal input from the phone line.
TXA	16	24	O	Transmit analog output to the phone line.
XTAL1 XTAL2	2 3	2 3	I I	These pins are for the internal crystal oscillator requiring a 11.0592 MHz parallel mode crystal. Two capacitors from these pins to ground are also required for proper crystal operation. Consult crystal manufacturer for proper values. XTAL2 can also be driven from an external clock.

REGISTER DESCRIPTIONS

Seven 8-bit internal registers are accessible for control and status monitoring. The registers are accessed in read or write operations by addressing the A0, A1 and A2 address lines in serial mode, or the AD0, AD1 and AD2 lines in parallel mode. The address lines are latched by ALE. Register CR0 controls the method by which data is transferred over the phone line. CR1 controls the interface between the microprocessor and the SSI 73K224L internal state. DR is a detect register which provides an indication of monitored modem status conditions. TR, the tone control register, controls the DTMF generator, answer and guard tones and RX output gate used in the modem initial connect sequence. CR2 is the primary DSP control interface and CR3 controls transmit attenuation and receive gain adjustments. All registers are read/write except for DR and ID which are read only. Register control and status bits are identified below:

REGISTER BIT SUMMARY

	ADDRESS	DATA BIT NUMBER							
REGISTER	AD - A0	D7	D6	D5	D4	D3	D2	D1	D0
CONTROL REGISTER 0 CR0	000	MODULATION OPTION	MODULATION TYPE 1	MODULATION TYPE 0	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ANSWER/ ORIGINATE
CONTROL REGISTER 1 CR1	001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTERRUPT	BYPASS SCRAMBLER	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0
DETECT REGISTER DR	010	RECEIVE LEVEL	PATTERN S1 DET	RECEIVE DATA	UNSCR. MARK DETECT	CARRIER DETECT	ANSWER TONE DETECT	CALL PROGRESS DETECT	SIGNAL QUALITY
TONE CONTROL REGISTER TR	011	RXD OUTPUT CONTROL	TRANSMIT GUARD TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF3	DTMF2	DTMF1/ OVERSPEED	DTMF0/ GUARD/ ANSWER
CONTROL REGISTER 2 CR2	100	0	0	CALL INITIALIZE	TRANSMIT S1	16 WAY	RESET DSP	TRAIN INHIBIT	EQUALIZER ENABLE
CONTROL REGISTER 3 CR3	101	0	0	0	RECEIVE GAIN BOOST	TRANSMIT ATTEN. 3	TRANSMIT ATTEN. 2	TRANSMIT ATTEN. 1	TRANSMIT ATTEN. 0
ID REGISTER ID	110	1	1	0	USER DEFINABLE PERSONALITY				

NOTE: When a register containing reserved control bits is written into, the reserved bits must be programmed as 0's.

REGISTER ADDRESS TABLE

REGISTER	ADDRESS AD2 - AD0	DATA BIT NUMBER D7	D6	D5	D4	D3	D2	D1	D0
CONTROL REGISTER 0 CR0	000	MODULATION OPTION	MODULATION TYPE 1	MODULATION TYPE 0	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ANSWER/ ORIGINATE
		QAM: 0=2400 BIT/S DPSK: 0=1200 BIT/S 1=600 BIT/S FSK: 0=103 MODE 1=V.21	10=QAM 00=DPSK 01=FSK		0000=PWR DOWN 0001=INT SYNCH 0010=EXT SYNCH 0011=SLAVE SYNCH 0100=ASYCH 8 BITS/CHAR 0101=ASYCH 9 BITS/CHAR 0110=ASYCH 10 BITS/CHAR 0111=ASYCH 11 BITS/CHAR 1100=FSK			0=SQUELCH ANALOG 1=ENABLE ANALOG	0=ANSWER 1=ORIGINATE
CONTROL REGISTER 1 CR1	001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTERRUPT	BYPASS SCRAMBLER	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0
			00=TX DATA 01=TX ALTERNATE 10=TX MARK 11=TX SPACE	0=OFF 1=ON	0=NORMAL 1=BYPASS SCRAMBLER	0=XTAL 1=16 X DATA RATE OUTPUT AT CLK PIN IN QAM/DPSK MODE ONLY	0=NORMAL 1=RESET	00=NORMAL 01=ANALOG LOOPBACK 10=REMOTE DIGITAL LOOPBACK 11=LOCAL DIGITAL LOOPBACK	
DETECT REGISTER DR	010	RECEIVE LEVEL	PATTERN S1	RECEIVE DATA	UNSCR. MARKS	CARRIER DETECT	ANSWER TONE	CALL PROGRESS	SIGNAL QUALITY
		0=SIGNAL BELOW THRESHOLD 1=ABOVE THRESHOLD	0=NOT PRESENT 1=PATTERN FOUND	OUTPUTS RECEIVED DATA STREAM		0=CONDITION NOT DETECTED 1=CONDITION DETECTED			0=GOOD 1=BAD
TONE CONTROL REGISTER TR	011	RXD OUTPUT CONTROL	TRANSMIT GUARD TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF3	DTMF2	DTMF1/ OVERSPEED	DTMF0/ GUARD/ ANSWER
		RXD PIN 0=NORMAL 1=OPEN	0=OFF 1=ON	0=OFF 1=ON	0=DATA 1=TX DTMF	4 BIT CODE FOR 1 OF 16 DUAL TONE COMBINATIONS			0=2225 Hz A.T. 1800 Hz G.T. 1=2100 Hz A.T. 550 Hz G.T.
CONTROL REGISTER 2 CR2	100			CALL INITIALIZE	TRANSMIT S1	16 WAY	$\overline{\text{RESET}}$ DSP	TRAIN INHIBIT	EQUALIZER ENABLE
				0=DSP IN DEMOD MODE 1=DSP IN CALL PROGRESS MODE	0=NORMAL DOTTING 1=S1	0=RX=TX 1=RX=16 WAY	0=DSP INACTIVE 1=DSP ACTIVE	0=ADAPT EQ ACTIVE 1=ADAPT EQ FROZEN	0=ADAPT EQ IN INIT 1=ADAPT EQ OK TO ADAPT
CONTROL REGISTER 3 CR3	101				RECEIVE GAIN BOOST	TRANSMIT ATTEN. 3	TRANSMIT ATTEN. 2	TRANSMIT ATTEN. 1	TRANSMIT ATTEN. 0
					0=NO BOOST 1=12 dB BOOST	0000-1111, SETS TRANSMIT ATTENUATOR 15 dB RANGE			
ID REGISTER ID	110	ID 2	ID 1	ID 0	USER DEFINABLE PERSONALITY				
		00X 73K212(L) or 73K322L 01X 73K221(L) or 73K302L 10X 73K222(L) 110 73K224L							

CONTROL REGISTER 0

	D7	D6	D5	D4	D3	D2	D1	D0
CR0 000	MODUL. OPTION	MODUL. TYPE 1	MODUL. TYPE 0	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ANSWER/ ORIGINATE

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	Answer/ Originate	0	Selects answer mode (transmit in high band, receive in low band).
		1	Selects originate mode (transmit in low band, receive in high band).
D1	Transmit Enable	0	Disables transmit output at TXA.
		1	Enables transmit output at TXA.
			Note: Transmit Enable must be set to 1 to allow activation of Answer Tone or DTMF.
D5, D4, D3, D2	Transmit Mode	D5 D4 D3 D2	
		0 0 0 0	Selects power down mode. All functions disabled except digital interface.
		0 0 0 1	Internal synchronous mode. In this mode TXCLK is an internally derived 1200 or 2400 Hz signal. Serial input data appearing at TXD must be valid on the rising edge of TXCLK. Receive data is clocked out of RXD on the falling edge of RXCLK.
		0 0 1 0	External synchronous mode. Operation is identical to internal synchronous, but TXCLK is connected internally to EXCLK pin, and a 1200 or 2400 Hz clock must be supplied externally.
		0 0 1 1	Slave synchronous mode. Same operation as other synchronous modes. TXCLK is connected internally to the RXCLK pin in this mode.
		0 1 0 0	Selects asynchronous mode - 8 bits/character (1 start bit, 6 data bits, 1 stop bit).
		0 1 0 1	Selects asynchronous mode - 9 bits/character (1 start bit, 7 data bits, 1 stop bit).
		0 1 1 0	Selects asynchronous mode - 10 bits/character (1 start bit, 8 data bits, 1 stop bit).
		0 1 1 1	Selects asynchronous mode - 11 bits/character (1 start bit, 8 data bits, Parity and/or 1 or 2 stop bits).
		1 1 0 0	Selects FSK operation.
D6,D5	Modulation Type	D6 D5	
		1 0	QAM
		0 0	DPSK
		0 1	FSK

CONTROL REGISTER 0 (Continued)

	D7	D6	D5	D4	D3	D2	D1	D0
CR0 000	MODUL. OPTION	MODUL. TYPE 1	MODUL. TYPE 0	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ANSWER/ ORIGINATE

BIT NO.	NAME	CONDITION	DESCRIPTION
D7	Modulation Option	0	QAM selects 2400 bps. DPSK selects 1200 bps. FSK selects 103 mode.
		1	DPSK selects 600 bps. FSK selects V.21 mode.

CONTROL REGISTER 1

	D7	D6	D5	D4	D3	D2	D1	D0
CR1 001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INT.	BYPASS SCRAMB	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0

BIT NO.	NAME	CONDITION	DESCRIPTION
D1, D0	Test Mode	D1 D0	
		0 0	Selects normal operating mode.
		0 1	Analog loopback mode. Loops the transmitted analog signal back to the receiver, and causes the receiver to use the same center frequency as the transmitter. To squelch the TXA pin, transmit enable bit must be low.
		1 0	Selects remote digital loopback. Received data is looped back to transmit data internally, and RXD is forced to a mark. Data on TXD is ignored.
		1 1	Selects local digital loopback. Internally loops TXD back to RXD and continues to transmit data carrrier at TXA pin.
D2	Reset	0	Selects normal operation.
		1	Resets modem to power down state. All control register bits (CR0, CR1, CR2, CR3 and Tone) are reset to zero except CR3 bit D2. The output of the clock pin will be set to the crystal frequency.
D3	CLK Control (Clock Control)	0	Selects 11.0592 MHz crystal echo output at CLK pin.
		1	Selects 16 X the data rate, output at CLK pin in DPSK/ QAM modes only.

CONTROL REGISTER 1 (Continued)

	D7	D6	D5	D4	D3	D2	D1	D0
CR1 001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INT.	BYPASS SCRAMB	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0

BIT NO.	NAME	CONDITION	DESCRIPTION
D4	Bypass Scrambler	0	Selects normal operation. DPSK data is passed through scrambler.
		1	Selects Scrambler Bypass. Bypass DPSK data is routed around scrambler in the transmit path.
D5	Enable Detect Interrupt	0	Disables interrupt at $\overline{INT}$ pin. All interrupts are normally disabled in power down modes.
		1	Enables $\overline{INT}$ output. An interrupts will be generated with a change in status of DR bits D1-D4 and D6. The answer tone and call progress detect interrupts are masked when the TX enable bit is set. Carrier detect is masked when TX DTMF is activated. All interrupts will be disabled if the device is in power down mode.
D7, D6	Transmit Pattern	D7 D6	
		0 0	Selects normal data transmission as controlled by the state of the TXD pin.
		0 1	Selects an alternating mark/space transmit pattern for modem testing and handshaking. Also used for S1 pattern generation. See CR2 bit D4.
		1 0	Selects a constant mark transmit pattern.
		1 1	Selects a constant space transmit pattern.

DETECT REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
DR 010	RECEIVE LEVEL	PATTERN S1	RECEIVE DATA	UNSCR. MARK	CARR. DETECT	ANSWER TONE	CALL PROG.	SIGNAL QUALITY

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	Signal Quality	0	Indicates normal received signal.
		1	Indicates low received signal quality (above average error rate).
D1	Call Progress Detect	0	No call progress tone detected.
		1	Indicates presence of call progress tones. The call progress detection circuitry is activated by energy in the normal 350 to 620 Hz call progress bandwidth.

DETECT REGISTER (Continued)

	D7	D6	D5	D4	D3	D2	D1	D0
DR 010	RECEIVE LEVEL	PATTERN S1	RECEIVE DATA	UNSCR. MARK	CARR. DETECT	ANSWER TONE	CALL PROG.	SIGNAL QUALITY

BIT NO.	NAME	CONDITION	DESCRIPTION
D2	Answer Tone Received	0	No answer tone detected.
		1	Indicates detection of 2225 Hz answer tone in Bell mode (TR bit D0=0) or 2100 Hz if in CCITT mode (TR bit D0=1). The device must be in originate mode for detection of answer tone.
D3	Carrier Detect	0	No carrier detected in the receive channel.
		1	Indicated carrier has been detected in the received channel.
D4	Unscr. Mark (Unscrambled Mark)	0	No unscrambled mark.
		1	Indicates detection of unscrambled marks in the received data. Should be time qualified by software.
D5	Receive Data		Continuously outputs the received data stream. This data is the same as that output on the RXD pin, but it is not disabled when RXD is tri-stated.
D6	Pattern S1 (unscrambled double dibit pattern of 00 and 11)	0	No S1 pattern being received.
		1	S1 pattern detected (11001100.....). Should be time qualified by software.
D7	Receive level	0	Received signal level below threshold, (≈ -21 dBm0);can use receive gain boost (+12 dB).
		1	Received signal above threshold.

TONE REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
TR 011	RXD OUTPUT CONTR.	TRANSMIT GUARD TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF 3	DTMF 2	DTMF 1/ OVER-SPEED	DTMF 0/ ANSWER/ GUARD

BIT NO.	NAME	CONDITION	DESCRIPTION
		D6 D5 D4 D0	D0 interacts with bits D6, D5, and D4 as shown.
D0	DTMF 0/	X X 1 X	Transmit DTMF tones.
	Answer/	X 1 0 0	Select Bell mode answer tone. Interacts with DR bit D2 and TR bit D5.
(Continued)	Guard Tone	X 1 0 1	Select CCITT mode answer tone. Interacts with DR bit D2 and TR bit D5.

TONE REGISTER (Continued)

	D7	D6	D5	D4	D3	D2	D1	D0
TR 011	RXD OUTPUT CONTR.	TRANSMIT GUARD TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF 3	DTMF 2	DTMF 1/ OVER-SPEED	DTMF 0/ ANSWER/ GUARD

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	DTMF 0/	D6 D5 D4 D0	D0 interacts with bits D6, D5, and D4 as shown.
	Answer/	1 0 0 0	Select 1800 Hz guard tone.
	Guard Tone	1 0 0 1	Select 550 Hz guard tone.
D1	DTMF 1/	D4 D1	D1 interacts with D4 as shown.
		0 0	Asynchronous QAM or DPSK +1.0% -2.5%.
	Overspeed	0 1	Asynchronous QAM or DPSK +2.3% -2.5%.
D3, D2, D1, D0	DTMF 3, 2, 1, 0	D3 D2 D1 D0 0 0 0 0 - 1 1 1 1	Programs 1 of 16 DTMF tone pairs that will be transmitted when TX DTMF and TX enable bit (CR0, bit D1) is set. Tone encoding is shown below:

KEYBOARD EQUIVALENT	DTMF CODE D3 D2 D1 D0	TONES LOW HIGH
1	0 0 0 1	697 1209
2	0 0 1 0	697 1336
3	0 0 1 1	697 1477
4	0 1 0 0	770 1209
5	0 1 0 1	770 1336
6	0 1 1 0	770 1477
7	0 1 1 1	852 1209
8	1 0 0 0	852 1336
9	1 0 0 1	852 1477
0	1 0 1 0	941 1336
*	1 0 1 1	941 1209
#	1 1 0 0	941 1477
A	1 1 0 1	697 1633
B	1 1 1 0	770 1633
C	1 1 1 1	852 1633
D	0 0 0 0	941 1633

D4	TX DTMF	0	Disabled DTMF.
	(Transmit DTMF)	1	Activates DTMF. The selected DTMF tones are transmitted continuously when this bit is high. TX DTMF overrides all other transmit functions.

TONE REGISTER (Continued)

	D7	D6	D5	D4	D3	D2	D1	D0
TR 011	RXD OUTPUT CONTR.	TRANSMIT GUARD TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF 3	DTMF 2	DTMF 1/ OVER-SPEED	DTMF 0/ ANSWER/ GUARD

BIT NO.	NAME	CONDITION	DESCRIPTION
D5	TX ANS (Transmit Answer Tone)	D5 D4 D0	D5 interacts with bits D4 and D0 as shown. Also interacts with DR bit D2 in originate mode. See Detect Register description.
		0 0 X	Disables answer tone generator.
		1 0 0	In answer mode, a Bell 2225 Hz tone is transmitted continuously when the Transmit Enable bit is set.
		1 0 1	Likewise, a CCITT 2100 Hz answer tone is transmitted.
D6	TX Guard (Transmit Guard Tone)	0	Disables guard tone generator.
		1	Enables guard tone generator. (See D0 for selection of guard tones.)
D7	RXD Output Control	0	Enables RXD pin. Receive data will be output on RXD.
		1	Disables RXD pin. The RXD pin reverts to a high impedance with internal weak pull-up resistor.

CONTROL REGISTER 2

	D7	D6	D5	D4	D3	D2	D1	D0
CR2 100	0	0	CALL INIT	TRANSMIT S1	16 WAY	$\overline{\text{RESET}}$ DSP	TRAIN INHIBIT	EQUALIZER ENABLE

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	Equalizer Enable	0	The adaptive equalizer is in its initialized state.
		1	The adaptive equalizer is enabled. This signal is used in handshakes to control when the equalizer should calculate its coefficients.
D1	Train Inhibit	0	The adaptive equalizer is active.
		1	The adaptive equalizer coefficients are frozen.
D2	$\overline{\text{RESET DSP}}$	0	The DSP is inactive and all variables are initialized.
		1	The DSP is running based on the mode set by other control bits

CONTROL REGISTER 2 (Continued)

	D7	D6	D5	D4	D3	D2	D1	D0
CR2 100	0	0	CALL INIT	TRANSMIT S1	16WAY	$\overline{\text{RESET}}$ DSP	TRAIN INHIBIT	EQUALIZER ENABLE

BIT NO.	NAME	CONDITION	DESCRIPTION
D3	16 Way	0	The receiver and transmitter are using the same decision plane (based on the Modulator Control Mode).
		1	The receiver, independent of the transmitter, is forced into a 16 point decision plane. Used for QAM handshaking.
D4	Transmit S1	0	The transmitter when placed in QAM alternating mark/space mode transmits 0101..... scrambled or not dependent on the bypass scrambler bit.
		1	When this bit is 1 and only when the transmitter is placed in alternating mark/space mode by CR1 bits D7, D6, an unscrambled repetitive double dibit pattern of 00 and 11 at 1200 bit/s (S1) is sent.
D5	Call Init	0	The DSP is setup to do demodulation and pattern detection based on the various mode bits.
		1	The DSP decodes both answer tone and call progress tones.

CONTROL REGISTER 3

	D7	D6	D5	D4	D3	D2	D1	D0
CR3 101	0	0	0	RECEIVE ENABLE BOOST	TRANSMIT ATTEN. 3	TRANSMIT ATTEN. 2	TRANSMIT ATTEN. 1	TRANSMIT ATTEN. 0

BIT NO.	NAME	CONDITION	DESCRIPTION
D3, D2, D1,D0	Transmit Attenuator	D3 D2 D1 D0 0 0 0 0 - 1 1 1 1	Sets the attenuation level of the transmitted signal in 1dB steps. The default (D3-D0=0100) is for a transmit level of 10 dBm0 at the line with the recommended hybrid transmit gain. The total range is 15 dB.
D4	Receive Gain Boost	0	12 dB receive front end boost is not used.
		1	Boost is in the path. This boost does not change reference levels. It is used to extend dynamic range by compensating for internally generated noise when receiving weak signals. The receive level detect signal and knowledge of the hybrid and transmit attenuator setting will determine when boost should be enabled.

ID REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
ID	ID 2	ID 1	ID 0	USER DEFINABLE PERSONALITY				

BIT NO.	NAME	CONDITION	DESCRIPTION
D7, D6, D5 110	Device Identification Signature	D7 D6 D5	Indicates Device:
		0 0 X	SSI 73K212(L) or 73K322L
		0 1 X	SSI 73K221(L) or 73K302L
		1 0 X	SSI 73K222(L)
		1 1 0	SSI 73K224L

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
VDD Supply Voltage	14	V
Storage Temperature	-65 to 150	°C
Soldering Temperature (10 sec.)	260	°C
Applied Voltage	-0.3 to VDD+0.3	V

Note: All inputs and outputs are protected from static charge using built-in, industry standard protection devices and all outputs are short-circuit protected.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
VDD Supply voltage					
5V Version (73K224L)		4.5	5	5.5	V
Digital Pins					
VIH, Input high voltage					
Reset, XTAL2		3.0		VDD	V
All other inputs		2.0		VDD	V
VIL, Input low voltage		0		0.8	V
IOH, Output high current		-0.4			mA
IOL, Output low current				1.6	mA
TA, Operating Free-Air Temperature		-40		70	°C

RECOMMENDED OPERATING CONDITIONS (Continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
External Component (Refer to Application section for placement.)					
VREF Bypass capacitor	(VREF to GND)	0.1			µF
Bias setting resistor	(Placed between VDD and ISET pins)	1.8	2	2.2	MΩ
ISET Bypass capacitor	(ISET pin to GND)	0.1			µF
VDD Bypass capacitor 1	(VDD to GND)	0.1			µF
VDD Bypass capacitor 2	(VDD to GND)	22			µF
Clock Variation	(11.0592 MHz) Crystal or external clock	-0.01		+0.01	%

DC ELECTRICAL CHARACTERISTICS
*(TA = -40°C to 70°C, VDD =recommended range unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
IDD, Supply Current	CLK = 11.0592 MHz				
5V Version (73K224L)	ISET Resistor = 2 MΩ				
IDDA, Active			25	27	mA
IDD1, Power-down	CLK = 11.0592 MHz		3		mA
IDD2, Power-down	CLK = 19.200 KHz		2		mA
Digital Inputs					
VIL, Input Low Voltage				.8	V
VIH, Input High Voltage					
All Inputs except Reset XTAL 1, XTAL 2		2.0			V
Reset, XTAL 1, XTAL2		3.0			V
IIH, Input High Current	VI = VIH MAX			100	µA
IIL, Input Low Current	VI = VIL MIN	-200			µA
Reset Pull-down Current	Reset = VDD	5		50	µA

* Although marked as a commercial temperature range part (0-70°C) the 73K224L operates to -40°C as with industrial temperature range rated devices.

DC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Digital Outputs					
VOH, Output High Voltage	IO = IOH Min IOUT = -0.4 mA	2.4		VDD	V
VOL, Output Low Voltage	IO = IOUT = 1.6 mA			0.4	V
VOL, CLK Output	IOUT = 3.6 mA			0.6	V
RXD Tri-State Pull-up Curr.	RXD = GND	-5		-50	µA
Capacitance					
Inputs	Capacitance, all Digital Input pins			10	pF
XTAL1, 2 Load Capacitors	Typical, depends on crystal	15		60	pF
CLK	Maximum Capacitive Load			15	pF

DYNAMIC CHARACTERISTICS AND TIMING
(TA = -40°C to +70°C, VDD = recommended range unless otherwise noted.)

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNITS
QAM/DPSK Modulator					
Carrier Suppression	Measured at TXA	55			dB
Output Amplitude	TX scrambled marks	-11.5	-10.0	-9	dBm0
FSK Modulator					
Output Freq. Error	CLK = 11.0592 MHz	-.31		+.05	%
Transmit Level	ATT = 0100 (Default) Transmit Dotting Pattern	-11.5	-10.0	-9	dBm0
Output Distortion	All products through BPF			-45	dB
Output Bias Distortion	Transmit Dotting Pattern in ALB @ RXD	-5		+5	%
2100 Hz Answer Tone Generator					
Output Amplitude	ATT = 0100 (Default Level) Not in V.21 Mode	-11.5	-10	-9	dBm0
Output Distortion	All products though BPF			-40	dB

NOTE: Parameters expressed in dBm0 refer to the following definition:

0 dB loss in the Transmit path to the line.

2 dB gain in the Receive path from the line.

Refer to the Basic Box Modem diagram in the Applications section for the DAA design.

DYNAMIC CHARACTERISTICS AND TIMING (Continued)

PARAMETERS		CONDITIONS	MIN	NOM	MAX	UNITS
DTMF Generator						
Freq. Accuracy			-.25		+.25	%
Output Amplitude		Low Band ATT = 0100	-10		-8	dBm0
Output Amplitude		High Band ATT = 0100	-8		-6	dBm0
Twist		High-Band to Low-Band	1.0	2.0	3.0	dB
Receiver Dynamic Range		Refer to Performance Curves		40		dB
Call Progress Detector		In Call Init mode				
Detect Level		460 Hz test signal	-34		0	dBm0
Reject Level					-40	dBm0
Delay Time		-70 dBm0 to -30 dBm0 STEP			25	ms
Hold Time		-30 dBm0 to -70 dBm0 STEP			25	ms
Hysteresis			2			dB
Carrier Detect						
Threshold		QAM/DPSK or FSK receive data	-48		-43	dBm0
Hysteresis		All Modes	2			
Delay Time	DPSK	-70 dBm0 to -6 dBm0	15	20	25	ms
		-70 dBm0 to -40 dBm0				
	QAM	-70 dBm0 to -60 dBm0	25	30	35	ms
		-70 dBm0 to -40 dBm0	25	33	41	ms
Hold Time	DPSK	-6 dBm0 to -? dBm0	15	22	28	ms
		-40 dBm0 to -70 dBm0	10	15	20	ms
	QAM	-6 dBm0 to -70 dBm0	44	50	56	ms
		-40 dBm0 to -70 dBm0	21	26	31	ms
Answer Tone Detectors		Call Init Mode				
Detect Level			-48		-43	dBm0
Detect Time		For signals from	7		37	ms
Hold Time		-6 to -40 dBm0, 2100 or 2225 Hz	10		48	ms
Detect Time		Demod Mode for signals from	4		26	ms
Hold Time		-6 to -40 dBm0, 2100 or 2225 Hz	11		43	ms

DYNAMIC CHARACTERISTICS AND TIMING (Continued)

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNITS
Pattern Detectors	DPSK Mode				
S1 Pattern					
Delay Time	For signals from -6 to -40 dBm0,	15		32	ms
Hold Time	-6 to -40 dBm0, Demod Mode	4		21	ms
Unscrambled Mark					
Delay Time	For signals from -6 to -40	-16		38	ms
Hold Time	Demod or call Init Mode	13		47	ms
Receive Level Indicator					
Detect On				-20	dBm0
Valid after Carrier Detect		10			ms
Output Smoothing Filter					
Output Impedance	TXA pin		200	300	Ω
Output load	TXA pin; FSK Single	10			KΩ
	Tone out for THD = -50 dB in .3 to 3.4 KHz range			50	pF
Maximum Transmitted Energy	4K Hz, Guard Tones off			-35	dBm0
	10K Hz, Guard Tones off			-60	dBm0
	12K Hz, Guard Tones off			-70	dBm0
Anti Alias Low Pass Filter	(Frequency KHz)				
Out of Band Signal Energy (Defines Hybrid Trans-	Level at RXA pin with receive Boost Enabled				
Hybrid loss requirements)	Scrambled data at 2400 bit/s in opposite band			-14	dBm
	Sinusoids out of band			-9	dBm
Transmit Attenuator					
Range of gain	Default ATT=0100 (0 dBm0)	+4		-11	dB
Step Accuracy		-0.1		+0.1	dB
Output Impedance			100		KΩ
Clock Noise	TXA pin; 153.6 KHz				
5V Version (73K224L)				1.5	mVrms
12V Version (73K224)				3	mVrms
Carrier Offset					
Capture Range	Originate or Answer		±7	±10	Hz

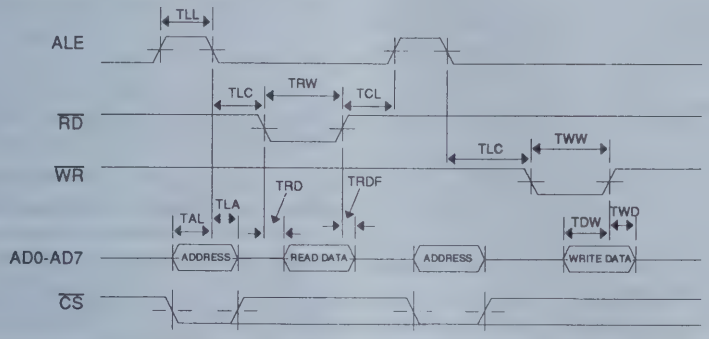
DYNAMIC CHARACTERISTICS AND TIMING (Continued)

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNITS
Recovered Clock					
Capture Range	% of frequency originate or answer	-.024		+.024	%
Guard Tone Generator					
Tone Accuracy	550 Hz			+1.18	%
	1800 Hz	-0.7			
Tone Level	550 Hz	-5.0	-3.0	-2.0	dB
(Below QAM/DPSK Output)	1800 Hz	-8.0	-6.0	-5.0	dB
Harmonic Distortion	550 Hz			-50	dB
(700 to 2900 Hz)	1800 Hz			-60	dB
Timing (Refer to Timing Diagrams)					
TAL	$\overline{CS}$/Addr. setup before ALE	30			ns
TLA	$\overline{CS}$/Addr. Hold after latch	20			ns
TLC	Latch to $\overline{RD}$/$\overline{WR}$ control	40			ns
TCL	$\overline{RD}$/$\overline{WR}$ Control to Latch	10			ns
TRD	Data out from $\overline{RD}$	0		140	ns
TLL	ALE width	60			ns
TRDF	Data float after READ	0		200	ns
TRW	READ width	200		25000	ns
TWW	WRITE width	140		25000	ns
TDW	Data setup before WRITE	150			ns
TWD	Data hold after WRITE	20			ns
TCKD	Data out after CLK			200	ns
TCKW	WRITE after CLK	150			ns
TDCK	Data setup before CLK	150			ns
TAC	Address setup before control [1]	50			ns
TCA	Address hold after control [1]	50			ns

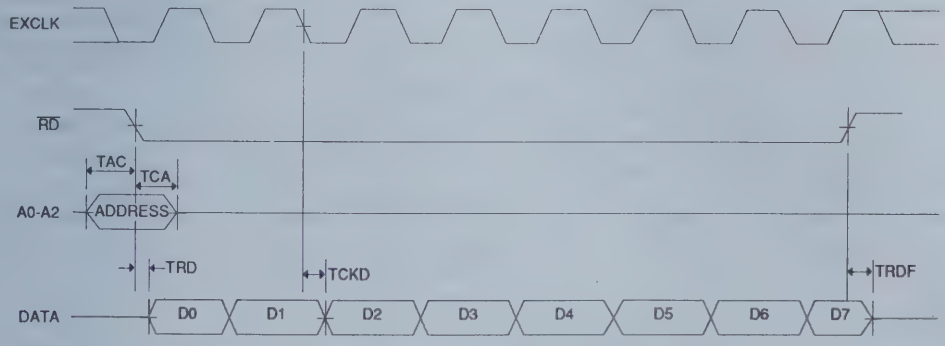
1: Control for setup is the falling edge of $\overline{RD}$ or $\overline{WR}$.
Control for hold is the falling edge of $\overline{RD}$ or the rising edge of $\overline{WR}$.

TIMING DIAGRAMS

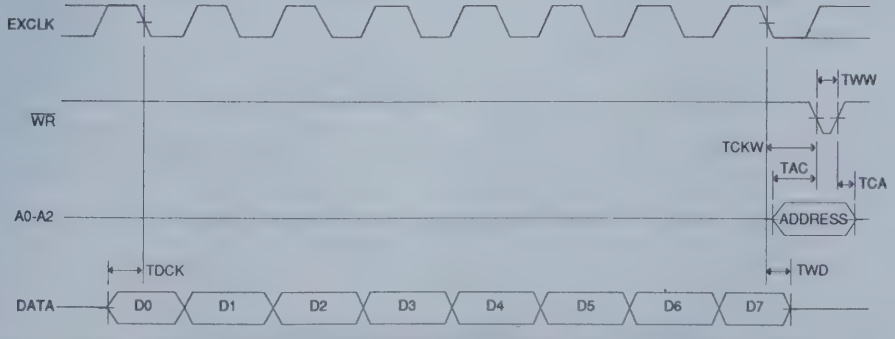
BUS TIMING DIAGRAM (PARALLEL VERSION)



READ TIMING DIAGRAM (SERIAL VERSION)



WRITE TIMING DIAGRAM (SERIAL VERSION)



APPLICATIONS INFORMATION

GENERAL CONSIDERATIONS

Figures 1 and 2 show the basic circuit diagram for K–Series modem integrated circuits. K-Series products are designed to be used in conjunction with a control processor, a UART or RS-232 serial data interface, and a DAA phone line interface to function as a typical intelligent modem. The K-Series ICs interface directly with Intel 8048 and 80C51 microprocessors for control and status monitoring purposes. Two typical DAA arrangements are shown: one for a split ±5 or ±12 volt design and one for a single 5 volt design. These diagrams are for reference only and do not represent production-ready modem designs.

K-Series devices are available in two control interface versions: one for a parallel multiplexed address/data interface, and one for a serial interface. The parallel version is intended for use with 8039/48 or 8031/51 microcontrollers from Intel or many other manufacturers. The serial interface 22-pin version can be used with other microcontrollers or in applications where only a limited number of port lines are available. The parallel versions may also be used in the serial mode, as explained in the data sheet pin description.

In most applications the controller will monitor the serial data for commands from the DTE and the received data for break signals from the far end modem. In this way, command data to the modem is sent over the same data line as the transmitted data. In other applications the RS-232 interface handshake lines are used for modem control.

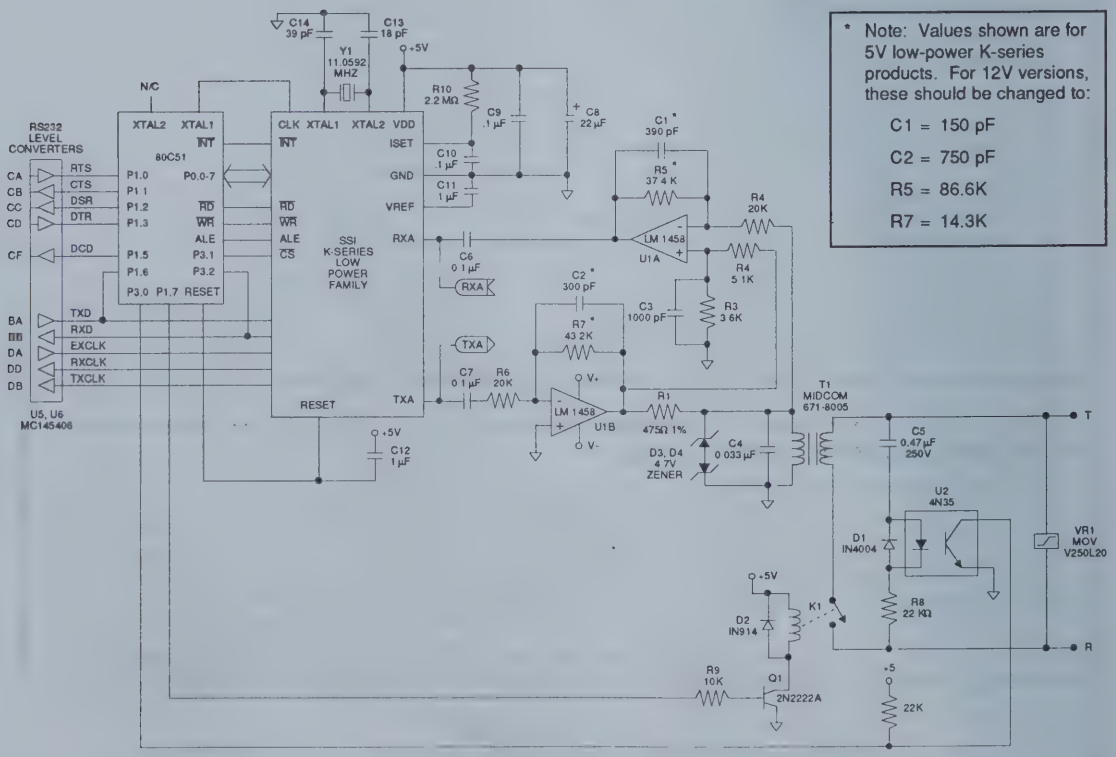


FIGURE 1: Basic Box Modem with Dual-Supply DAA

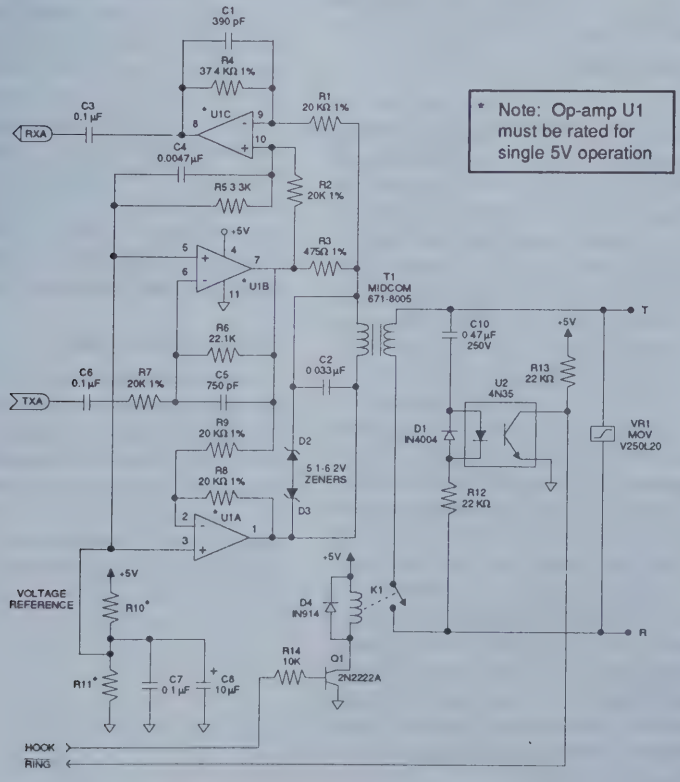
DIRECT ACCESS ARRANGEMENT (DAA)

The DAAs shown are two examples of how the "hybrid" may be implemented. The split supply design (Figure 1) is a typical two op-amp hybrid. The receive op-amp serves two purposes. It supplies gain to amplify the receive signal to the proper level for the modem's detectors and demodulator, and it removes the transmitted signal from the receive signal present at the transformer. This is done by supplying a portion of the transmitted signal to the non-inverting input of the receive op-amp at the same amplitude as the signal appearing at the transformer, making the transmit signal common mode.

The single-supply DAA is more complex than the dual-supply version described above, but its use eliminates the need for a second power supply. This DAA (Figure 2) uses a bridged drive to allow undistorted signals to be sent with a single 5 volt supply. Because DTMF tones utilize a higher amplitude than data, these signals will clip if a single-ended drive approach is used. The bridged driver uses an extra op-amp (U1A) to invert the signal coming from the gain setting op-amp (U1B) before sending it to the other leg of the transformer. Each op-amp then supplies half the drive signal to the transformer. The receive amplifier (op-amp C) picks off its signal at the junction of the impedance matching resistor and the transformer. Because the bottom leg of the transformer is being driven in one direction by U1A and the resistor is driven in the opposite direction at the same time by U1B, the summing point of the transformer and resistor remains relatively constant and the receive signal is unaffected.

DESIGN CONSIDERATIONS

Silicon Systems 1-chip modem products include all basic modem functions on a single IC, accessible from a standard bus interface. This makes these devices adaptable for use in a variety of applications, and as easy to control as conventional digital bus peripherals.



* Note: Op-amp U1 must be rated for single 5V operation

FIGURE 2: Single 5V DAA Version

Unlike digital logic circuitry, however, modem designs must properly contend with precise frequency tolerances, and very low level analog signals, to insure acceptable performance. Using good analog circuit design practices will generally result in a sound design. Folllowing are additional recommendations which should be taken into consideration when starting new designs.

CRYSTAL OSCILLATOR

The K-Series crystal oscillator requires a parallel mode (antiresonant) crystal which operates at 11.0592 MHz. It is important that this precise frequency be maintained to within ±.01% accuracy.

In order for a parallel mode crystal to operate correctly and to specification, it must have a load capacitor connected to the junction of each of the crystal and internal inverter connections, terminated to ground. The values of these capacitors depend primarily on the crystal's characteristics, and to a lesser degree on the internal inverter circuit. The values used affect the accuracy and start up characteristics of the oscillator.

LAYOUT CONSIDERATIONS

Good analog/digital design rules must be used to control system noise in order to obtain highest performance in modem designs. The more digital circuitry present on the PC board, the more this attention to noise control is needed. The modem should be treated as a high impedance analog device. A 22 µF electrolytic capacitor in parallel with a 0.1 µF ceramic capacitor between VDD and ground is recommended. Liberal use of ground planes and larger traces on power and ground are also highly favored. High speed digital circuits tend to generate a significant amount of EMI (Electro-Magnetic Interference) which must be minimized in order to meet regulatory agency limitations. To accomplish this, high speed digital devices should be locally bypassed, and the DAA and K-Series device should be located close to each other near the area of the board where the phone line connection is accessed. To avoid problems, power supply and ground traces should be routed separately to the analog and digital functions on the board, and digital signals should not be routed near low level or high impedance analog traces. The analog and digital grounds should only connect at one point near the analog supplies to avoid ground loops. The K–Series modem IC's should have both high frequency and low frequency bypassing as near to the package as possible.

MODEM PERFORMANCE CHARACTERISTICS

The curves presented here define modem IC performance under a variety of line conditions while inducing disturbances that are typical of those encountered during data transmission on public service telephone lines. Test data was taken using an AEA Electronics' "Autotest I" modem test set and line simulator, operating under computer control. All tests were run full-duplex, using a Concord Data Systems 224 as the reference modem. A 511 pseudo-random-bit pattern was used with $1X10^6$ bits transmitted for each data point. Noise was C-message weighted and all signal-to-noise (S/N) ratios reflect total power measurements similar to the CCITT V.56 measurement specification. The individual tests are defined as follows.

BER vs.S/N

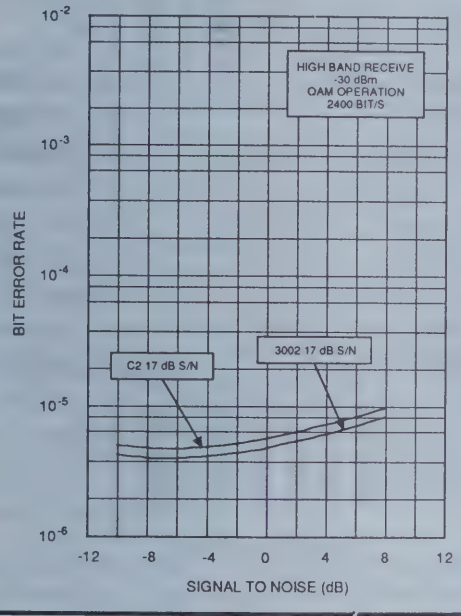
This test measures the ability of the modem to operate over noisy lines with a minimum of data-transfer errors. Since some noise is generated in the best of dial-up lines, the modem must operate with the lowest S/N ratio possible. Optimum modem performance is indicated by test curves that are closest to the zero axis. A narrow spread between curves representing the four line parameters indicates minimal variation in performance while operating over a range of aberrant operating conditions. Typically, a PSK modem will exhibit better BER-performance test curves operating in the highband range than in the lowband.

BER vs. Receive Level

This test measures the dynamic range of the modem. Because signal levels vary widely over dial-up lines, the widest possible dynamic range is desirable. The minimum Bell specification calls for 36 dB of dynamic range. S/N ratios are held constant at the indicated values while the receive level is lowered from a very high to very low signal levels. The width of the "bowl" of these curves, taken at the BER point, is the measure of dynamic range.

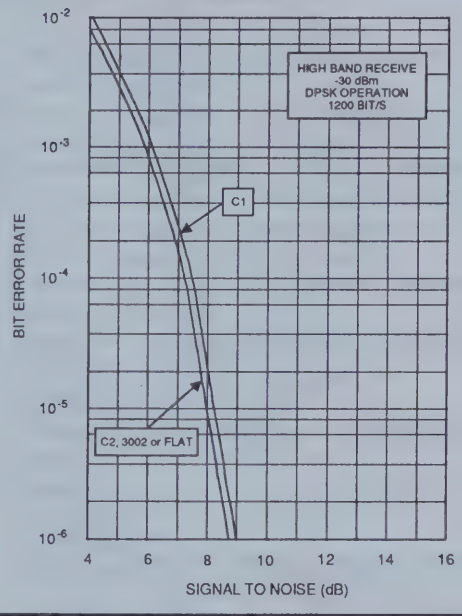
SSI 73K224L BER vs CARRIER OFFSET

PRELIMINARY



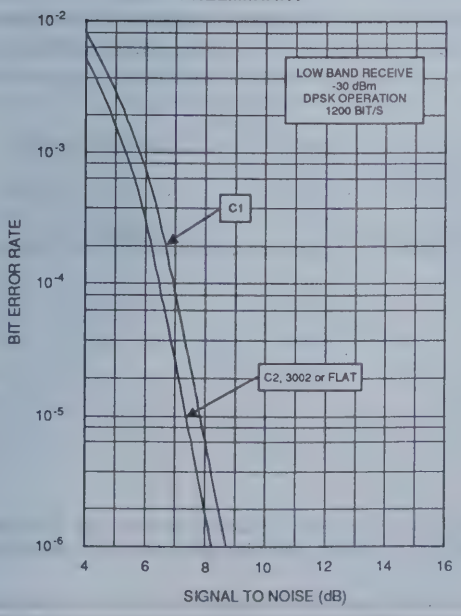
SSI 73K224L BER vs S/N

PRELIMINARY

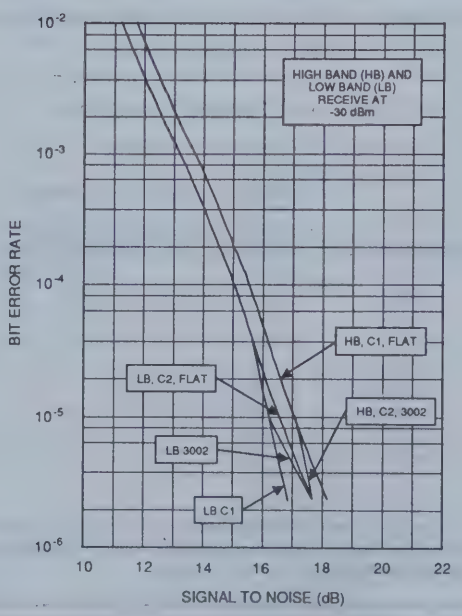


SSI 73K224L BER vsS/N

PRELIMINARY

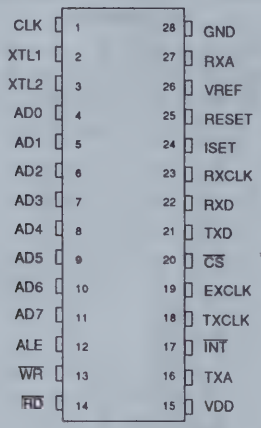


SSI 73K224L BER vs QAM

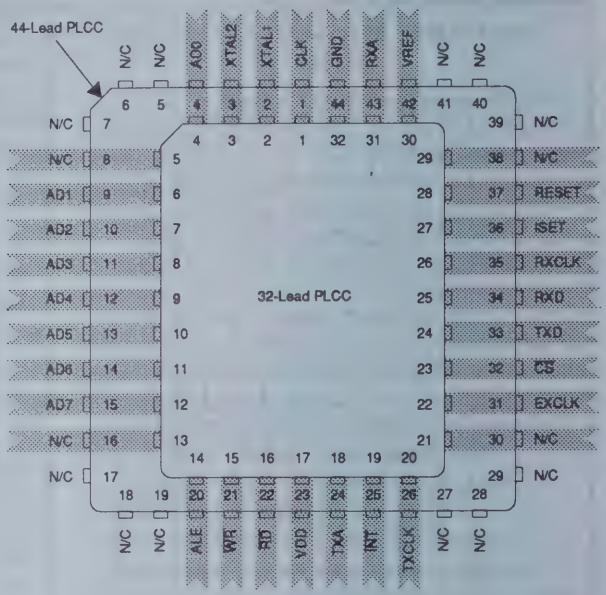


SSI 73K224L
V.22 bis/V.22/V.21, Bell 212A/103
Single-Chip Modem

PACKAGE PIN DESIGNATIONS
(TOP VIEW)



600-Mil
28-Pin DIP



32, 44-Lead PLCC

CAUTION: Use handling procedures necessary for a static sensitive component.

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 73K224L with Parallel Bus Interface		
28-Pin Plastic Dual-In-Line	SSI 73K224L – CP	73K224L – CP
32-Pin Plastic Leaded Chip Carrier	SSI 73K224L – 32CH	73K224L – 32CH
44-Pin Plastic Leaded Chip Carrier	SSI 73K224L – CH	73K224L – CH

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Patent No. (4,777,453) (4,789,995) Other Patents Pending

SSI 73K302L
Bell 212A, 103, 202 Single-Chip Modem

July, 1989

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DESCRIPTION

The SSI 73K302L is a highly integrated single-chip modem IC which provides the functions needed to construct a Bell 202, 212A and 103 compatible modem. The SSI 73K302L is an enhancement of the SSI 73K212L single-chip modem with Bell 202 mode features added. The 73K302L is capable of 1200 or 0–300 bit/s full-duplex operation over dial-up lines. 4–wire full-duplex capability and a low speed back channel are also provided in Bell 202 mode. The SSI 73K302L recognizes and generates a 900 Hz soft carrier turn-off tone, and allows 103 fallback for 300 bit/s FSK operation. The SSI 73K302L integrates analog, digital, and switched-capacitor array functions on a single substrate, offering excellent performance and a high level of functional integration in a single 28 or 22–pin DIP configuration. The SSI 73K302L operates from a single +5 volt supply with very low power consumption.

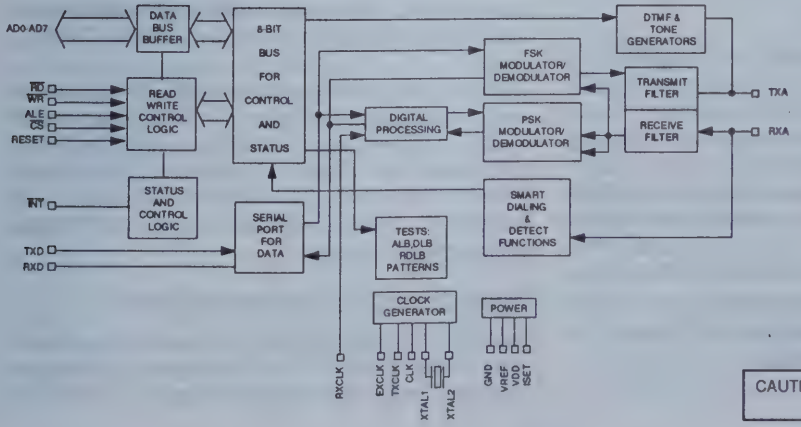
The SSI 73K302L includes the DPSK and FSK modulator/demodulator functions, call progress and handshake tone monitors, test modes, and a tone generator capable of producing DTMF, answer, and 900 Hz soft carrier turn-off tone. This device supports Bell 202, 212A and 103 modes of operation, allowing both synchronous and asynchronous communications. The SSI 73K302L is designed to appear to the systems designer as a microprocessor peripheral, and will

(Continued)

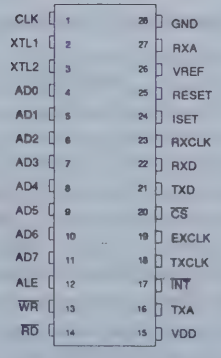
FEATURES

- **One-chip Bell 212A, 103 and 202S/T standard compatible modem**
- **Full-duplex operation at 0-300 bit/s (FSK), 1200 bit/s (DPSK) or 0-1200 bit/s (FSK) forward channel with or without 0-150 bit/s back channel**
- **Full-duplex 4-wire operation in Bell 202 mode**
- **Pin and software compatible with other SSI K–Series 1-chip modems**
- **Interfaces directly with standard microprocessors (8048, 80C51 typical)**
- **Serial (22-pin DIP) or parallel microprocessor bus (28-pin DIP) for control**
- **Serial port for data transfer**
- **Both synchronous and asynchronous modes of operation**
- **Call progress, carrier, precise answer tone (2225 Hz), soft carrier turn-off (SCT), and FSK mark detectors**
- **DTMF, answer, and SCT tone generators**
- **Test modes available: ALB, DL, RDL, Mark, Space, Alternating bit patterns**
- **Space efficient 22 or 28-pin DIP packages**
- **CMOS technology for low power consumption using 35 mW @ 5V from a single power supply**

BLOCK DIAGRAM



PIN DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

DESCRIPTION (Continued)

easily interface with popular one-chip microprocessors (80C51 typical) for control of modem functions through its 8-bit multiplexed address/data bus or via an optional serial command bus. An ALE control line simplifies address demultiplexing. Data communications occurs through a separate serial port only.

OPERATION

The SSI 73K302L is ideal for use in either free standing or integral system modem products where multi-standard data communications is desired. Its high functionality, low power consumption and efficient packaging simplify design requirements and increase system reliability. A complete modem requires only the addition of the phone line interface, a modem controller, and RS232 level converter for a typical system.

Tri-mode capability in one-chip allows full-duplex Bell 212 and 103 operation or assymetrical Bell 202 operation over the 2-wire switched telephone network. 202 mode full-duplex operation at 1200 bit/s is also possible when operating on 4-wire leased lines.

A soft carrier turn-off feature facilitates fast line turn around when using the 202 mode for half-duplex applications.

The SSI 73K302L is part of Silicon Systems K-Series family of pin and function compatible single-chip modem products. These devices allow systems to be configured for higher speeds and Bell or CCITT operation with only a single component change.

ASYNCHRONOUS MODE

Data transmission for the DPSK mode requires that data ultimately be transmitted in a synchronous fashion, The SSI 73K302L includes ASYNC/SYNC and SYNC/ASYNC converters which delete or insert stop bits in order to transmit data at a regular rate. In asynchronous mode the serial data comes from the TXD pin into the ASYNC/SYNC rate converter. The ASYNC/SYNC rate converter accepts the data provided on the TXD pin which normally must be 1200 bit/s +1.0%, 2.5%. The rate converter will then insert or delete stop bits in order to output a signal which is 1200 bit/s ± .01% (± .01% is the crystal tolerance).

The SYNC/ASYNC converter also has an overspeed mode which allows selection of an output overspeed range of either +1% or +2.3%. In the overspeed mode, some stop bits are output at 7/8 the normal width.

The serial data stream from the transmit buffer or the rate converter is passed through the data scrambler and onto the analog modulator. The data scrambler can be bypassed under processor control when unscrambled data must be transmitted. The ASYNC/SYNC rate converter and the data scrambler are bypassed in all FSK modes. If serial input data contains a break signal through one character (including start and stop bits) the break will be extended to at least $2 \cdot N + 3$ bits long (where N is the number of transmitted bits/character).

Serial data from the demodulator is passed normally first through the data descrambler and then through the SYNC/ASYNC rate converter. The ASYNC/ASYNC convertor will reinsert any deleted stop bits and transmit output data at an intra-character rate (bit-to-bit timing) of no greater than 1219 bit/s. An incoming break signal (low through two characters) will be passed through without incorrectly inserting a stop bit.

Similar to the transmit side, both the SYNC/ASYNC rate converter and the data descrambler are bypassed in the FSK modes.

SYNCHRONOUS MODE

The Bell 212A standard defines synchronous operation at 1200 bit/s. Operation is similar to that of the asynchronous mode except that data must be synchronized to a provided clock and no variation in data transfer rate is allowable. Serial input data appearing at TXD must be valid on the rising edge of TXCLK.

TXCLK is an internally derived signal in internal mode and is connected internally to the RXCLK pin in slave mode. Receive data at the RXD pin is clocked out on the falling edge of RXCLK. The ASYNCH/SYNCH converter is bypassed when synchronous mode is selected and data is transmitted out at essentially the same rate as it is input.

DPSK MODULATOR/DEMODULATOR

In DPSK mode the SSI 73K302L modulates a serial bit stream into di-bit pairs that are represented by four possible phase shifts as prescribed by the Bell 212A

standards. The base-band signal is then filtered to reduce intersymbol interference on the bandlimited 2–wire telephone line. Transmission occurs on either a 1200 Hz (originate mode) or 2400 Hz (answer mode) carrier. Demodulation is the reverse of the modulation process, with the incoming analog signal eventually decoded into di-bits and converted back to a serial bit stream. The demodulator also recovers the clock which was encoded into the analog signal during modulation. Demodulation occurs using either a 1200 Hz carrier (answer mode or ALB originate mode) or a 2400 Hz carrier (originate mode or ALB answer mode). The SSI 73K302L uses a phase locked loop coherent demodulation technique that offers inherently better performance than typical DPSK demodulators used by other manufacturers.

FSK MODULATOR/DEMODULATOR

The FSK modulator produces a frequency modulated analog output signal using two discrete frequencies to represent the binary data. Bell 103 mode uses 1270 and 1070 Hz (originate, mark and space) or 2225 and 2025 Hz (answer, mark and space). Bell 202 mode uses 1200 and 2200 Hz for the main channel and 387 and 487 Hz for the back channel. The modulation rate of the back channel is up to 150 baud. Demodulation involves detecting the received frequencies and decoding them into the appropriate binary value. The rate converter and scrambler/descrambler are automatically bypassed in the 103 or 202 modes.

PASSBAND FILTERS AND EQUALIZERS

A high and low band filter is included to shape the amplitude and phase response of the transmit and receive signals and provide compromise delay equalization and rejection of out-of-band signals in the receive channel. Amplitude and phase equalization are necessary to compensate for distortion of the transmission line and to reduce intersymbol interference in the bandlimited receive signal. The transmit signal filtering approximates a 75% square root of raised Cosine frequency response characteristic.

AGC

The automatic gain control maintains a signal level at the input to the demodulators which is constant to within 1 dB. It corrects quickly for increases in signal which would cause clipping and provides a total dynamic range of >45 dB.

PARALLEL BUS INTERFACE

Four 8-bit registers are provided for control, option select and status monitoring. These registers are addressed with the AD0, AD1, and AD2 multiplexed address lines (latched by ALE) and appear to a control microprocessor as four consecutive memory locations. Two control registers and the tone register are read/write memory. The status detect register is read only and cannot be modified except by modem response to monitored parameters. The parallel bus interface is not available in the 22-pin package.

SERIAL COMMAND INTERFACE

The serial command mode allows access to the SSI 73K302L control and status registers via a serial command port. In this mode the A0 , A1 and A2 lines provide register addresses for data passed through the data pin under control of the $\overline{RD}$ and $\overline{WR}$ lines. A read operation is initiated when the $\overline{RD}$ line is taken low. The next eight cycles of EXCLK will then transfer out eight bits of the selected address location LSB first. A write takes place by shifting in eight bits of data LSB first for eight consecutive cycles of EXCLK. $\overline{WR}$ is then pulsed low and data transfer into the selected register occurs on the rising edge of $\overline{WR}$.

SPECIAL DETECT CIRCUITRY

The special detect circuitry monitors the received analog signal to determine status or presence of carrier, answer tone and weak received signal (long loop condition), special tones such as FSK marking and the 900 Hz soft carrier turn-off tone are also detected. A highly frequency selective call progress detector provides adequate discrimination to accurately detect lower quality call progress signals.

DTMF GENERATOR

The DTMF generator will output one of 16 standard dual-tones determined by a 4-bit binary value and TX DTMF mode bit previously loaded into the tone register. Dialing is initiated when the DTMF mode is selected and the transmit enable (CR0 bit D1) is changed from 0 to 1.

SOFT CARRIER TURN-OFF TONE GENERATOR

The soft carrier turn-off tone generator will output a 900 Hz tone. When activated in Bell 202 main channel transmit mode, the output signal will shift to 900 Hz, maintaining phase continuity during the transition.

PIN DESCRIPTION

POWER

NAME	28-PIN	22-PIN	TYPE	DESCRIPTION
GND	28	1	I	System Ground.
VDD	15	11	I	Power supply input, 5V±10%. Bypass with .1 and 22 µF capacitors to ground.
Vref	26	21	O	An internally generated reference voltage. Bypass with .1 µF capacitor to ground.
Iset	24	19	I	Chip current reference. Sets bias current for op-amps. The chip current is set by connecting this pin to VDD through a 2 MΩ resistor. Iset should be bypassed to GND with a .1 µF capacitor.

PARALLEL MICROPROCESSOR INTERFACE

ALE	12	-	I	Address latch enable. The falling edge of ALE latches the address on AD0-AD2 and the chip select on $\overline{CS}$.
AD0-AD7	4-11	-	I/O	Address/data bus. These bidirectional tri-state multiplexed lines carry information to and from the internal registers.
$\overline{CS}$	20	-	I	Chip select. A low on this pin allows a read cycle or a write cycle to occur. AD0-AD7 will not be driven and no registers will be written if $\overline{CS}$ (latched) is not active. $\overline{CS}$ is latched on the falling edge of ALE.
CLK	1	2	O	Output clock. This pin is selectable under processor control to be either the crystal frequency (for use as a processor clock) or 16 x the data rate for use as a baud rate clock in DPSK modes only. The pin defaults to the crystal frequency on reset.
$\overline{INT}$	17	13	O	Interrupt. This open drain output signal is used to inform the processor that a detect flag has occurred. The processor must then read the detect register to determine which detect triggered the interrupt. $\overline{INT}$ will stay active until the processor reads the detect register or does a full reset.
$\overline{RD}$	14	-	I	Read. A "low" requests a read of the SSI 73K302L internal registers. Data cannot be output unless both $\overline{RD}$ and the latched $\overline{CS}$ are active or "low."
RESET	25	20	I	Reset. An active signal "high" on this pin will put the chip into an inactive state. All control register bits (CR0, CR1, Tone) will be reset. The output of the CLK pin will be set to the crystal frequency. An internal pull down resistor permits power on reset using a capacitor to VDD.

PIN DESCRIPTION (Continued)

PARALLEL MICROPROCESSOR INTERFACE (Continued)

NAME	28-PIN	22-PIN	TYPE	DESCRIPTION
$\overline{WR}$	13	-	I	Write. A "low" on this informs the SSI 73K302L that data is available on AD0-AD7 for writing into an internal register. Data is latched on the rising edge of $\overline{WR}$. No data is written unless both $\overline{WR}$ and the latched $\overline{CS}$ are active ("low").

SERIAL MICROPROCESSOR INTERFACE

A0-A2	-	5-7	I	Register Address Selection. These lines carry register addresses and should be valid during any read or write operation.
DATA	-	8	I/O	Serial Control Data. Data for a read/write operation is clocked in or out on the falling edge of the EXCLK pin. The direction of data flow is controlled by the $\overline{RD}$ pin. $\overline{RD}$ low outputs data. $\overline{RD}$ high inputs data.
$\overline{RD}$	-	10	I	Read. A "low" on this input informs the SSI 73K302L that data or status information is being read by the processor. The falling edge of the $\overline{RD}$ signal will initiate a read from the addressed register. The $\overline{RD}$ signal must continue for eight falling edges of EXCLK in order to read all eight bits of the referenced register. Read data is provided LSB first. Data will not be output unless the $\overline{RD}$ signal is active.
$\overline{WR}$	-	9	I	Write. A "low" on this input informs the SSI 73K302L that data or status information has been shifted in through the DATA pin and is available for writing to an internal register. The normal procedure for a write is to shift in data LSB first on the DATA pin for eight consecutive falling edges of EXCLK and then to pulse $\overline{WR}$ low. Data is written on the rising edge of $\overline{WR}$.

Note: In the serial, 22-pin version, the pins AD0-AD7, ALE and $\overline{CS}$ are removed and replaced with the pins; A0, A1, A2, DATA, and an unconnected pin. Also, the $\overline{RD}$ and $\overline{WR}$ controls are used differently.

The serial control mode is provided in the 28-pin version by tying ALE high and $\overline{CS}$ low. In this configuration AD7 becomes DATA and AD0, AD1 and AD2 become A0, A1 and A2, respectively.

PIN DESCRIPTION (Continued)

RS-232 INTERFACE

NAME	28-PIN	22-PIN	TYPE	DESCRIPTION
EXCLK	19	15	I	External Clock. This signal is used in synchronous DPSK transmission when the external timihg option has been selected. In the external timing mode the rising edge of EXCLK is used to strobe synchronous DPSK transmit data available on the TXD pin. Also used for serial control interface.
RXCLK	23	18	O	Receive Clock. The falling edge of this clock output is coincident with the transitions in the serial received DPSK data output. The rising edge of RXCLK can be used to latch the valid output data. RXCLK will be valid as long as a carrier is present. In Bell 202 mode a clock which is 16 x 1200 baud data rate is output.
RXD	22	17	O	Received Digital Data Output. Serial receive data is available on this pin. The data is always valid on the rising edge of RXCLK when in synchronous mode. RXD will output constant marks if no carrier is detected.
TXCLK	18	14	O	Transmit Clock. This signal is used in synchronous DPSK transmission to latch serial input data on the TXD pin. Data must be provided so that valid data is available on the rising edge of the TXCLK. The transmit clock is derived from different sources depending upon the synchronization mode selection. In Internal Mode the clock is 1200 Hz generated internally. In External Mode TXCLK is phase locked to the EXCLK pin. In Slave Mode TXCLK is phase locked to the RXCLK pin. TXCLK is always active. In Bell 202 mode the output is a 16 x 1200 baud clock.
TXD	21	16	I	Transmit Digital Data Input. Serial data for transmission is input on this pin. In synchronous modes, the data must be valid on the rising edge of the TXCLK clock. In asynchronous modes (1200 or 300 baud) no clocking is necessary. DPSK must be 1200 bit/s +1%, -2.5% or +2.3%, -2.5 % in overspeed mode.

ANALOG INTERFACE

RXA	27	22	I	Received modulated analog signal input from the phone line.
TXA	16	12	O	Transmit analog output to the phone line.
XTAL1 XTAL2	2 3	3 4	I I	These pins are for the internal crystal oscillator requiring a 11.0592 MHz parallel mode crystal and two load capacitors to Ground. XTAL2 can also be driven from an external clock.

REGISTER DESCRIPTIONS

Four 8-bit internal registers are accessible for control and status monitoring. The registers are accessed in read or write operations by addressing the A0 and A1 address lines in serial mode, or the AD0 and AD1 lines in parallel mode. The AD0 and AD1 lines are latched by ALE. Register CR0 controls the method by which data is transferred over the phone line. CR1 controls the interface between the microprocessor and the SSI 73K302L internal state. DR is a detect register which provides an indication of monitored modem status conditions. TR, the tone control register, controls the DTMF generator, answer and guard tones and RX output gate used in the modem initial connect sequence. All registers are read/write except for DR which is read only. Register control and status bits are identified below:

REGISTER BIT SUMMARY

	ADDRESS	DATA BIT NUMBER							
REGISTER	AD2 - AD0	D7	D6	D5	D4	D3	D2	D1	D0
CONTROL REGISTER 0 CR0	000	MODULATION OPTION		TRANSMIT MODE 3	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ANSWER/ ORIGINATE
CONTROL REGISTER 1 CR1	001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTERRUPT	BYPASS SCRAMBLER/ ADD PH. EQ. 202	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0
DETECT REGISTER DR	010			RECEIVE DATA	UNSCR. MARKS	CARRIER DETECT	SPECIAL TONE	CALL PROGRESS	LONG LOOP
TONE CONTROL REGISTER TR	011	RXD OUTPUT CONTROL	TRANSMIT SOFT CARRIER TURN-OFF TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF3	DTMF/ 202T FDX	DTMF1/ OVERSPEED	DTMF0/ SPEC. TONE SELECT
CONTROL REGISTER 2 CR2	100				THESE REGISTER LOCATIONS ARE RESERVED FOR				
CONTROL REGISTER 3 CR3	101				USE WITH OTHER K-SERIES FAMILY MEMBERS				
ID REGISTER ID	110	0	0						

NOTE: When a register containing reserved control bits is written into, the reserved bits must be programmed as 0's.

REGISTER ADDRESS TABLE

REGISTER	ADDRESS	DATA BIT NUMBER							
	AD2 - AD0	D7	D6	D5	D4	D3	D2	D1	D0
CONTROL REGISTER 0 CR0	000	MODULATION OPTION		TRANSMIT MODE 3	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ORIGINATE/ ANSWER
CONTROL REGISTER 1 CR1	001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTERRUPT	BYPASS SCRAMBLER/ ADD PH. EQ.	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0
DETECT REGISTER DR	010			RECEIVE DATA	UNSCR. MARKS	CARRIER DETECT	SPECIAL TONE	CALL PROGRESS	LONG LOOP
TONE CONTROL REGISTER TR	011	RXD OUTPUT CONTROL	TRANSMIT SOFT CARRIER TURN-OFF TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF3	DTMF2/ 202T FDX	DTMF1/ OVERSPEED	DTMF0/ SPECIAL TONE
ID REGISTER ID	110	ID 1	ID 0						

CONTROL REGISTER 0 (CR0)

- MODULATION OPTION: 0=103 FSK, 1=202 FSK
- TRANSMIT MODE 3: 0000=PWR DOWN, 1100=FSK, 0010=EXT SYNCH, 0011=SLAVE SYNCH, 0100=ASYNCH 8 BITS/CHAR, 0101=ASYNCH 9 BITS/CHAR, 0110=ASYNCH 10 BITS/CHAR, 0111=ASYNCH 11 BITS/CHAR, 1100=FSK BELL 103 OR 202
- TRANSMIT ENABLE: 0=SQUELCH ANALOG, 1=ENABLE ANALOG
- ORIGINATE/ ANSWER: IN 212, 103 MODES: 0=ANSWER, 1=ORIGINATE; IN 202 MODE: 0=RECEIVE @ 1200 BIT/S, TRANSMIT @ 150 BIT/S, 1=RECEIVE @ 150 BIT/S, TRANSMIT @ 1200 BIT/S

CONTROL REGISTER 1 (CR1)

- TRANSMIT PATTERN 1, 0: 00=TX DATA, 01=TX ALTERNATE, 10=TX MARK, 11=TX SPACE
- ENABLE DETECT INTERRUPT: 0=OFF, 1=ON
- BYPASS SCRAMBLER/ ADD PH. EQ.: 0=NORMAL, 1=BYPASS SCRAMBLER, 1=ADD EXTRA PHASE EQ. IN 202
- CLK CONTROL: 0=XTAL, 1=16 X DATA RATE OUTPUT AT CLK PIN IN DPSK MODE ONLY
- RESET: 0=NORMAL, 1=RESET
- TEST MODE 1, 0: 00=NORMAL, 01=ANALOG LOOPBACK, 10=REMOTE DIGITAL LOOPBACK, 11=LOCAL DIGITAL LOOPBACK

DETECT REGISTER (DR)

- RECEIVE DATA: OUTPUTS RECEIVED DATA STREAM
- UNSCR. MARKS, CARRIER DETECT, SPECIAL TONE, CALL PROGRESS, LONG LOOP: 0=CONDITION NOT DETECTED, 1=CONDITION DETECTED

TONE CONTROL REGISTER (TR)

- RXD OUTPUT CONTROL: RXD PIN 0=NORMAL, 1=TRI STATE
- TRANSMIT SOFT CARRIER TURN-OFF TONE: 0=OFF, 1=ON
- TRANSMIT ANSWER TONE: 0=OFF, 1=ON
- TRANSMIT DTMF: 0=DATA, 1=TX DTMF
- DTMF3, DTMF2/ 202T FDX: 4 BIT CODE FOR 1 OF 16 DUAL TONE COMBINATIONS. OVERIDES OTHER TRANSMIT MODES
  - 0=NORMAL OPERATION, 1=FULL DUPLEX IN 202 MODE
- DTMF1/ OVERSPEED: 0=1%, 1=2.5%
- DTMF0/ SPECIAL TONE: 0=900 HZ SCT TONE IF IN ANSWER MODE =2225 HZ ANSWER TONE IN 103 OR 212 ORIGINATE MODES, 1=FSK MARK

ID REGISTER

- ID 1, ID 0: 00=73K212 US 212/103 OR 73K322 V.23/V 22/V.21, 01=73K221 EUROPEAN V.22/V.21 or 73K302 212A/103/202, 10=73K222 BELL 212/103 AND V.22/V.21, 11=73K224 BELL 212/103 AND V.22 bis/V.22/V 21

CONTROL REGISTER 0

	D7	D6	D5	D4	D3	D2	D1	D0
CR0 000	MODUL. OPTION		TRANSMIT MODE 3	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ANSWER/ ORIGINATE

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	Answer/ Originate	0	Selects answer mode (transmit in high band, receive in low band or in Bell 202 mode, receive at 1200 bit/s and transmit at 150 bit/s).
		1	Selects originate mode (transmit in low band,receive in high band or in Bell 202 mode, receive at 150 bit/s and transmit at 1200 bit/s).
			Note: This bit works with TR bit D0 to program special tones detected in Tone Register. See detect and tone registers.
D1	Transmit Enable	0	Disables transmit output at TXA.
		1	Enables transmit output at TXA.
			Note: Answer tone and DTMF TX control require TX enable.
D5, D4,D3, D2	Transmit Mode	D5 D4 D3 D2	
		0 0 0 0	Selects power down mode. All functions disabled except digital interface.
		0 0 0 1	Internal synchronous mode. In this mode TXCLK is an internally derived 1200 Hz signal. Serial input data appearing at TXD must be valid on the rising edge of TXCLK. Receive data is clocked out of RXD on the falling edge of RXCLK.
		0 0 1 0	External synchronous mode. Operation is identical to internal synchronous, but TXCLK is connected internally to EXCLK pin, and a 1200 Hz clock must be supplied externally.
		0 0 1 1	Slave synchronous mode. Same operation as other synchronous modes. TXCLK is connected internally to the RXCLK pin in this mode.
		0 1 0 0	Selects PSK asynchronous mode - 8 bits/character (1 start bit, 6 data bits, 1 stop bit).
		0 1 0 1	Selects PSK asynchronous mode - 9 bits/character (1 start bit, 7 data bits, 1 stop bit).
		0 1 1 0	Selects PSK asynchronous mode - 10 bits/character (1 start bit, 8 data bits, 1 stop bit).
		0 1 1 1	Selects PSK asynchronous mode - 11 bits/character (1 start bit, 8 data bits, Parity and/or 1 or 2 stop bits).
		1 1 0 0	Selects 103 or 202 FSK operation.

CONTROL REGISTER 0 (Continued)

	D7	D6	D5	D4	D3	D2	D1	D0
CR0 000	MODUL. OPTION		TRANSMIT MODE 3	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ANSWER/ ORIGINATE

BIT NO.	NAME	CONDITION	DESCRIPTION
D6		0	Not used; must be written as a "0."
D7	Modulation Option	D7 D5 D4	Selects:
		X 0 X	DPSK asynchronous mode at 1200 bit/s.
		0 1 1	FSK Bell 103 mode.
		1 1 1	FSK Bell 202 mode.

CONTROL REGISTER 1

	D7	D6	D5	D4	D3	D2	D1	D0
CR1 001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTER.	BYPASS SCRAMB/ ADD PH. EQ.	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0

BIT NO.	NAME	CONDITION	DESCRIPTION
D1, D0	Test Mode	D1 D0	
		0 0	Selects normal operating mode.
		0 1	Analog loopback mode. Loops the transmitted analog signal back to the receiver, and causes the receiver to use the same center frequency as the transmitter. To squelch the TXA pin, transmit enable must be forced low. Not supported in FDX202 mode.
		1 0	Selects remote digital loopback. Received data is looped back to transmit data internally, and RXD is forced to a mark. Data on TXD is ignored.
		1 1	Selects local digital loopback. Internally loops TXD back to RXD and continues to transmit data from TXA pin.
D2	Reset	0	Selects normal operation.
		1	Resets modem to power down state. All control register bits (CR0, CR1, Tone) are reset to zero. The output of the clock pin will be set to the crystal frequency.

CONTROL REGISTER 1 (Continued)

	D7	D6	D5	D4	D3	D2	D1	D0
CR1 001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTER.	BYPASS SCRAMB/ ADD PH. EQ.	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0

BIT NO.	NAME	CONDITION	DESCRIPTION
D3	CLK Control (Clock Control)	0	Selects 11.0592 MHz crystal echo output at CLK pin.
		1	Selects 16 X the data rate, output at CLK pin in DPSK modes only.
D4*	Bypass Scrambler/ Add Ph. Eq.	0	Selects normal operation. DPSK data is passed through scrambler.
		1	Selects Scrambler Bypass. Bypass DPSK data is routed around scrambler in the transmit path. In Bell 202 mode, additional phase equalization is added to the main channel filters when D4 is set to 1.
D5	Enable Detect Interrupt	0	Disables interrupt at $\overline{INT}$ pin. All interrupts are normally disabled in power down modes.
		1	Enables $\overline{INT}$ output. An interrupt will be generated with a change in status of DR bits D1-D4. The special tone and call progress detect interrupts are masked when the TX enable bit is set. Carrier detect is masked when TX DTMF is activated. All interrupts will be disabled if the device is in power down mode.
D7, D6	Transmit Pattern	D7 D6	
		0 0	Selects normal data transmission as controlled by the state of the TXD pin.
		0 1	Selects an alternating mark/space transmit pattern for modem testing.
		1 0	Selects a constant mark transmit pattern.
		1 1	Selects a constant space transmit pattern.

* D4 should always be set to 1 when receiving 1200 bit/s data and to 0 when transmitting 1200 bit/s data in 202 mode.

DETECT REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
DR 010			RECEIVE DATA	UNSCR. MARK	CARR. DETECT	SPECIAL TONE	CALL PROG.	LONG LOOP

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	Long Loop	0	Indicates normal received signal.
		1	Indicates low received signal level.
D1	Call Progress Detect	0	No call progress tone detected.
		1	Indicates presence of call progress tones. The call progress detection circuitry is activated by energy in the normal 350 to 620 Hz call progress bandwidth.
D2	Special Tone Detect	0	No special tone detected as programmed by CR0 bit D0 and Tone Register bit D0.
		1	Special tone detected. The detected tone is:
			(1) 2225 Hz answer tone if D0 of TR=0 and the device is in Bell 103 or 212A originate mode.
			(2) Soft carrier turn-off tone if D0 of TR=0 and the device is in Bell 202 answer mode.
			(3) an FSK mark in the mode the device is set to receive if D0 of TR is set to 1.
			Tolerance on special tones is ±3%.
D3	Carrier Detect	0	No carrier detected in the receive channel.
		1	Indicated carrier has been detected in the received channel.
D4	Unscr. Mark (Unscrambled Mark)	0	No unscrambled mark.
		1	(DPSK only) Indicates detection of unscrambled marks in the received data. A valid indication requires that unscrambled marks be received for > 165.5 ± 6.5 ms.
D5	Receive Data		Continuously outputs the received data stream. This data is the same as that output on the RXD pin, but it is not disabled when RXD is tri-stated.
D6, D7			Not used.

TONE REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
TR 011	RXD OUTPUT CONTR.	TRANSMIT SOFT CARRIER TURN-OFF TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF 3	DTMF 2/ 202 FDX	DTMF 1/ OVER-SPEED	DTMF 0/ SPECIAL TONE SEL

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	DTMF 0 Special Tone Detect Select	D4 D0	D0 interacts with bits D6, D4, and CR0 as shown.
		1 X	Transmit DTMF tones.
		0 0	2225 Hz answer tone will be detected in D2 of DR if originate mode is selected in CR0.
			900 Hz SCT tone will be detected in D2 of DR if Bell 202 answer mode is selected in CR0.
		0 1	Mark of an FSK mode selected in CR0 is to be detected in D2 of DR.
D1	DTMF 1/ Overspeed	D4 D1	D1 interacts with D4 as shown.
		0 0	Asynchronous DPSK 1200 bit/s +1.0% -2.5%.
		0 1	Asynchronous DPSK 1200 bit/s +2.3% -2.5%.
D3, D2, D1, D0	DTMF 3, 2, 1, 0	D3 D2 D1 D0 0 0 0 0 - 1 1 1 1	Programs 1 of 16 DTMF tone pairs that will be transmitted when TX DTMF and TX enable bit (CR0, bit D1) is set. Tone encoding is shown below:

KEYBOARD EQUIVALENT	DTMF CODE D3 D2 D1 D0	TONES LOW HIGH
1	0 0 0 1	697 1209
2	0 0 1 0	697 1336
3	0 0 1 1	697 1477
4	0 1 0 0	770 1209
5	0 1 0 1	770 1336
6	0 1 1 0	770 1477
7	0 1 1 1	852 1209
8	1 0 0 0	852 1336
9	1 0 0 1	852 1477
0	1 0 1 0	941 1336

D2	202T	0	Enables 202 half-duplex operation if D4=0
	FDX	1	Enables 202 full-duplex operation if D4=0

TONE REGISTER (Continued)

	D7	D6	D5	D4	D3	D2	D1	D0
TR 011	RXD OUTPUT CONTR.	TRANSMIT SOFT CARRIER TURN-OFF TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF 3	DTMF 2/ 202T FDX	DTMF 1/ OVER-SPEED	DTMF 0/ SPECIAL TONE SEL

BIT NO.	NAME	CONDITION	DESCRIPTION
D3, D2, D1, D0 (cont.)			KEYBOARD EQUIVALENT / DTMF CODE D3 D2 D1 D0 / TONES LOW HIGH
			* 1 0 1 1 941 1209
			# 1 1 0 0 941 1477
			A 1 1 0 1 697 1633
			B 1 1 1 0 770 1633
			C 1 1 1 1 852 1633
			D 0 0 0 0 941 1633
D4	TX DTMF (Transmit DTMF)	0	Disables DTMF.
		1	Activates DTMF. The selected DTMF tones are transmitted continuously when this bit is high. TX DTMF overrides all other transmit functions.
D5	TX ANS (Transmit Answer tone)	0	Disables answer tone generator.
		1	Enables answer tone generator. A 2225 Hz answer tone will be transmitted continuously when the transmit enable bit is set. To transmit answer tone, the device must be in answer mode.
D6	Transmit SCT Tone	0	Disables SCT tone generator.
		1	Transmit SCT tone in Bell 202 mode.
D7	RXD Output Control	0	Enables RXD pin. Receive data will be output on RXD.
		1	Disables RXD pin. The RXD pin reverts to a high impedance with internal weak pull-up resistor.

Notes for Tone Register use:

1. To detect SCT tone, 202 answer mode must be selected. To transmit SCT tone, 202 originate mode must be selected.
2. For answer tone detection, 103 or 212 originate mode must be active. To transmit answer tone, the 73K302 must be in 103 or 212 answer mode.
3. After completion of DTMF dialing, bit D2 should be reset unless 202 full-duplex mode is selected.

ID REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
ID 110	ID 1	ID 0						

BIT NO.	NAME	CONDITION	DESCRIPTION
D7, D6	Device Identification Signature	D7 D6	Indicates Device:
		0 0	SSI 73K212 or 73K322L
		0 1	SSI 73K221 or 73K302L
		1 0	SSI 73K222
		1 1	SSI 73K224

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
VDD Supply Voltage	14	V
Storage Temperature	-65 to 150	°C
Soldering Temperature (10 sec.)	260	°C
Applied Voltage	-0.3 to VDD+0.3	V

Note: All inputs and outputs are protected from static charge using built-in, industry standard protection devices and all outputs are short-circuit protected.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
VDD Supply Voltage					
5V Version (73K302L)		4.5	5	5.5	V
Digital Pins					
VIH, Input High Voltage					
Reset, XTAL 1, XTAL 2		3.0		VDD	V
All other inputs		2.0		VDD	V
VIL, Input Low Voltage		0		0.8	V
IOH, Output High Current		-0.4			mA
IOL, Output Low Current				1.6	mA
TA, Operating Free-Air Temperature		-40		+85	°C

RECOMMENDED OPERATING CONDITIONS (Continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
External Component (Refer to Application section for placement.)					
VREF Bypass capacitor	(External to GND)	0.1			µF
Bias setting resistor	(Placed between VDD and ISET pins)	1.8	2	2.2	MΩ
ISET Bypass capacitor	(ISET pin to GND)	0.1			µF
VDD Bypass capacitor 1	(External to GND)	0.1			µF
VDD Bypass capacitor 2	(External to GND)	22			µF
Clock Variation	(11.0592 MHz) Crystal or external clock	-0.01		+0.01	%

DC ELECTRICAL CHARACTERISTICS
(TA = -40°C to 85°C, VDD = recommended range unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
IDD, Supply Current	ISET Resistor = 2 MΩ				
IDDA, Active	CLK = 11.0592 MHz		7	10	mA
IDD1, Power-down	CLK = 11.0592 MHz			4	mA
IDD2, Power-down	CLK = 19.200 KHz			3	mA
Digital Inputs					
IIH, Input High Current	VI = VIH Max			100	µA
IIL, Input Low Current	VI = VIL Min	-200			µA
Reset Pull-down Current	Reset = VDD	1		50	µA
Digital Outputs					
VOH, Output High Voltage	IO = IOH MIN	2.4		VDD	V
VOL, Output Low Voltage	IO = IO MAX			0.4	V
VOL, CLK Output	IO = 3.6 mA			0.6	V
RXD Tri-State Pull-up Curr.	RXD = GND	-1		-50	µA

DC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNITS
Capacitance					
Inputs	Capacitance, all Digital Input pins			10	pF
XTAL1, 2 Load Capacitors	Depends on crystal	15		60	pF
CLK	Maximum Capacitive Load			15	pF

DYNAMIC CHARACTERISTICS AND TIMING
(TA = -40°C to +85°C, VDD = Recommended range unless otherwise noted.)

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNITS
PSK Modulator					
Carrier Suppression	Measured at TXA	55			dB
Output Amplitude	TX scrambled marks	-11	-10	-9	dBm0
FSK Modulator					
Output Freq. Error	CLK = 11.0592 MHz	-0.35		+.35	%
Transmit Level	Transmit Dotting Pattern	-11	-10	-9	dBm0
Harmonic Distortion in 700-2900 Hz band	THD in the alternate band DPSK or FSK		-60	-50	dB
Output Bias Distortion	Transmit Dotting Pattern In ALB @ RXD		±8		%
Total Output Jitter	Randçm Input in ALB @ RXD	-10		+10	%
DTMF Generator					
Freq. Accuracy		-.25		+.25	%
Output Amplitude	Low Band	-10	-9	-8	dBm0
Output Amplitude	High Band	-8	-7	-6	dBm0
Twist	High-Band to Low-Band	1.0	2.0	3.0	dB
Long Loop Detect	DPSK	-38		-28	dBm0
Dynamic Range	Refer to Performance Curves		45		dB

Note: Parameters expressed in dBm0 refer to the following definition:

5V Version:
0 dB loss in the Transmit path to the line.
2 dB gain in the Receive path from the line.

Refer to the Basic Box Modem diagram in the Applications section for the DAA design.

DYNAMIC CHARACTERISTICS AND TIMING (Continued)

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNITS
Call Progress Detector					
Detect Level	-3 dB points in 285 and 675 Hz	-38			dBm0
Reject Level	Test signal is a 460 Hz sinusoid			-45	dBm0
Delay Time	-70 dBm0 to -30 dBm0 STEP	20		40	ms
Hold Time	-30 dBm0 to -70 dBm0 STEP	20		40	ms
Hysteresis		2			dB
Carrier Detect					
Threshold	DPSK or FSK receive data	-49		-42	dBm0
Delay Time					
Bell 103		10		20	ms
Bell 212A		15		32	ms
Bell 202 Forward Channel		7		12	ms
Bell 202 Back Channel		25		40	ms
Hold Time					
Bell 103		6		20	ms
Bell 212A		10		24	ms
Bell 202 Forward Channel		4		8	ms
Bell 202 Back Channel		20		30	ms
Hysteresis		2			dB
Special Tone Detectors					
Detect Level	See definitions for TR bit D0 mode	-49		-42	dBm0
Delay Time					
Answer tone		15		30	ms
900 Hz SCT tone	Preceded by valid carrier	4		8	ms
387 Hz Back channel mark		25		60	ms
1270 or 2225 Hz marks		15		30	ms

DYNAMIC CHARACTERISTICS AND TIMING (Continued)

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNITS
Special Tone Detectors (Continued)					
Hold Time					
Answer tone		4		24	ms
900 Hz SCT tone		2		4	ms
387 Hz Back channel mark		20		30	ms
1270 or 2225 Hz marks		15		30	ms
Hysteresis		2			dB
Detect Freq. Range	Any Special Tone	-3		+3	%
Output Smoothing Filter					
Output load	TXA pin; FSK Single Tone out for THD = -50 dB in .3 to 3.4 KHz	10		 50	KΩ pF
Out of Band Energy	Frequency >12KHz in all modes See Transmit Energy Spectrum			-70	dBm0
Output Impedance	TXA pin		200	300	Ω
Clock Noise	TXA pin; 76.8 KHz or 122.88 KHz in 202 main channel			0.4	mVrms
Carrier VCO					
Capture Range	Originate or Answer	-10		+10	Hz
Capture Time	-10 Hz to +10 Hz Carrier Frequency Change		40	100	ms
Recovered Clock					
Capture Range	% of frequency center frequency (center at 1200 Hz)	-625		+625	ppm
Data Delay Time	Analog data in at RXA pin to receive data valid at RXD pin		30	50	ms
Tone Generator					
Tone Accuracy	DTMF or FSK tones	-5		+5	Hz
Tone Level		-1		+1	dB

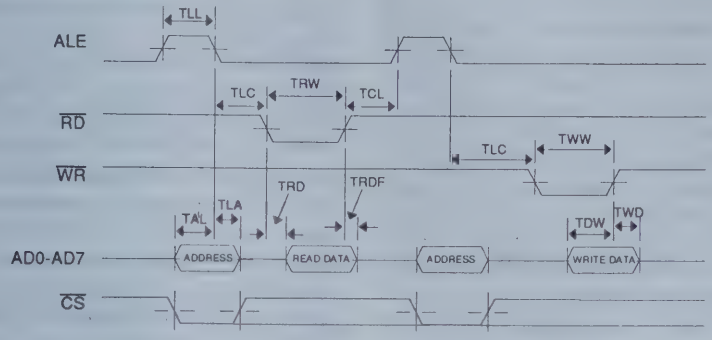
DYNAMIC CHARACTERISTICS AND TIMING (Continued)

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNITS
Timing (Refer to Timing Diagrams)					
TAL	$\overline{CS}$/Addr. setup before ALE	30			ns
TLA	$\overline{CS}$/Addr. Hold after latch	20			ns
TLC	Latch to $\overline{RD}/\overline{WR}$ control	40			ns
TCL	$\overline{RD}/\overline{WR}$ Control to Latch	10			ns
TRD	Data out from $\overline{RD}$	0		160	ns
TLL	ALE width	60			ns
TRDF	Data float after READ	0		80	ns
TRW	READ width	200		25000	ns
TWW	WRITE width	140		25000	ns
TDW	Data setup before WRITE	150			ns
TWD	Data hold after WRITE	20			ns
TCKD	Data out after CLK			200	ns
TCKW	WRITE after CLK	150			ns
TDCK	Data setup before CLK	150			ns
TAC	Address setup before control [1]	50			ns
TCA	Address hold after control [1]	50			ns

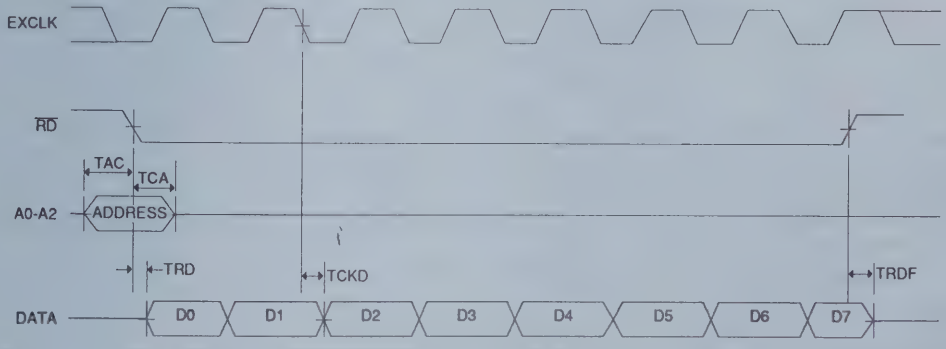
1: Control for setup is the falling edge of $\overline{RD}$ or $\overline{WR}$.
Control for hold is the falling edge of $\overline{RD}$ or the rising edge of $\overline{WR}$.

TIMING DIAGRAMS

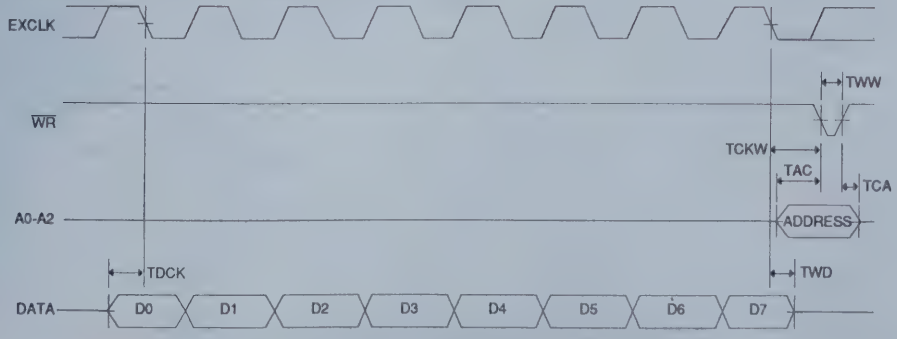
BUS TIMING DIAGRAM (PARALLEL VERSION)



READ TIMING DIAGRAM (SERIAL VERSION)



WRITE TIMING DIAGRAM (SERIAL VERSION)



APPLICATIONS INFORMATION

GENERAL CONSIDERATIONS

Figures 1 and 2 show the basic circuit diagram for K–Series modem integrated circuits. K-Series products are designed to be used in conjunction with a control processor, a UART or RS232 serial data interface, and a DAA phone line interface to function as a typical intelligent modem. The K-Series ICs interface directly with Intel 8048 and 80C51 microprocessors for control and status monitoring purposes. Two typical DAA arrangements are shown: one for a split ±5 or ±12 volt design and one for a single 5 volt design. These diagrams are for reference only and do not represent production-ready modem designs.

K-Series devices are available in two control interface versions: one for a parallel multiplexed address/data interface, and one for a serial interface. The parallel version is intended for use with 8039/48 or 8031/51 microcontrollers from Intel or many other manufacturers. The serial interface 22-pin version can be used with other microcontrollers or, in applications where only a limited number of port lines are available. The parallel versions may also be used in the serial mode, as explained in the data sheet pin description.

In most applications the controller will monitor the serial data for commands from the DTE and the received data for break signals from the far end modem. In this way, command data to the modem is sent over the same data line as the transmitted data. In other applications the RS232 interface handshake lines are used for modem control.

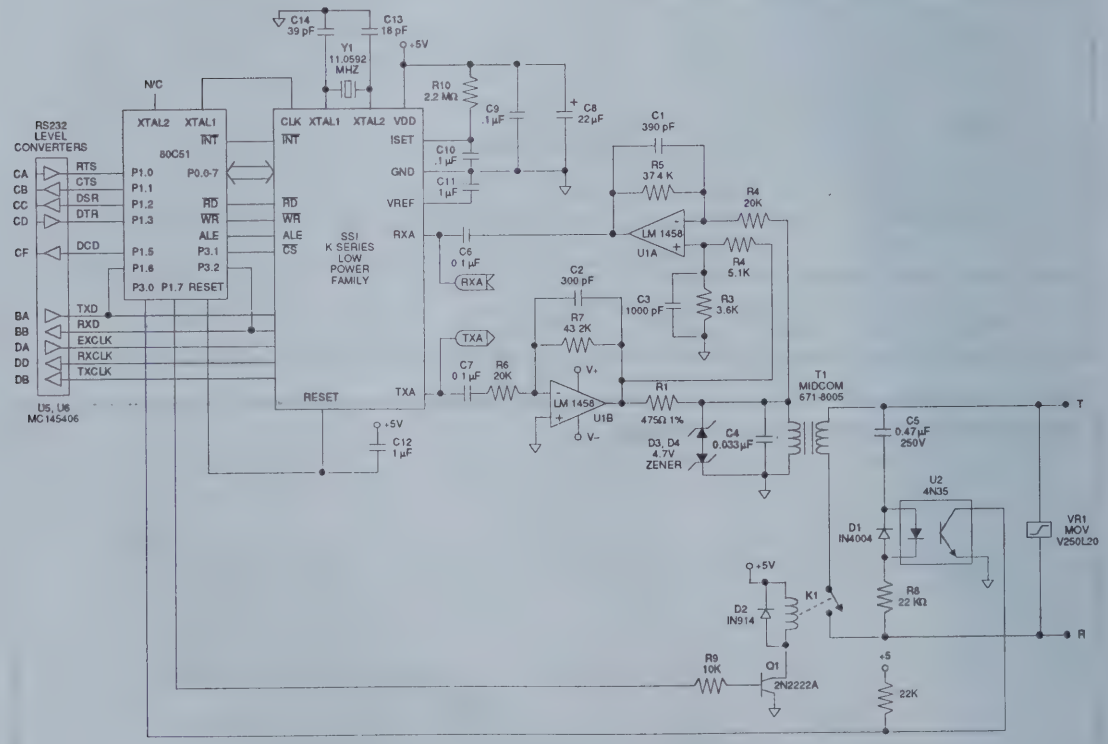


FIGURE 1: Basic Box Modem with Dual-Supply DAA

DIRECT ACCESS ARRANGEMENT (DAA)

The DAAs shown are two examples of how the "hybrid" may be implemented. The split supply design (Figure 1) is a typical two op-amp hybrid. The receive op-amp serves two purposes. It supplies gain to amplify the receive signal to the proper level for the modem's detectors and demodulator, and it removes the transmitted signal from the receive signal present at the transformer. This is done by supplying a portion of the transmitted signal to the non-inverting input of the receive op-amp at the same amplitude as the signal appearing at the transformer, making the transmit signal common mode.

The single-supply DAA is more complex than the dual-supply version described above, but its use eliminates the need for a second power supply. This DAA (Figure 2) uses a bridged drive to allow undistorted signals to be sent with a single 5 volt supply. Because DTMF tones utilize a higher amplitude than data, these signals will clip if a single-ended drive approach is used. The bridged driver uses an extra op-amp (U1A) to invert the signal coming from the gain setting op-amp (U1B) before sending it to the other leg of the transformer. Each op-amp then supplies half the drive signal to the transformer. The receive amplifier (op–amp C) picks off its signal at the junction of the impedance matching resistor and the transformer. Because the bottom leg of the transformer is being driven in one direction by U1A and the resistor is driven in the opposite direction at the same time by U1B, the summing point of the transformer and resistor remains relatively constant and the receive signal is unaffected.

DESIGN CONSIDERATIONS

Silicon Systems 1-chip modem products include all basic modem functions on a single IC, accessible from a standard bus interface. This makes these devices adaptable for use in a variety of applications, and as easy to control as conventional digital bus peripherals.

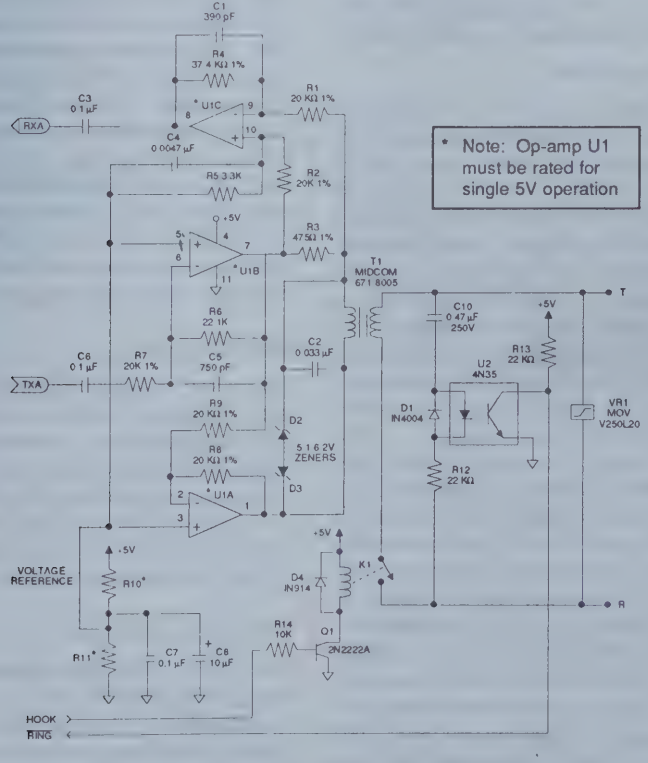


FIGURE 2: Single 5V DAA Version

Unlike digital logic circuitry, however, modem designs must properly contend with precise frequency tolerances, and very low level analog signals, to insure acceptable performance. Using good analog circuit design practices will generally result in a sound design. Folllowing are additional recommendations which should be taken into consideration when starting new designs.

CRYSTAL OSCILLATOR

The K-Series crystal oscillator requires a parallel mode (antiresonant) crystal which operates at 11.0592 MHz. It is important that this precise frequency be maintained to within ±.01% accuracy.

In order for a parallel mode crystal to operate correctly and to specification, it must have a load capacitor connected to the junction of each of the crystal and internal inverter connections, terminated to ground. The values of these capacitors depend primarily on the crystal's characteristics, and to a lesser degree on the internal inverter circuit. The values used affect the accuracy and start up characteristics of the oscillator.

LAYOUT CONSIDERATIONS

Good analog/digital design rules must be used to control system noise in order to obtain highest performance in modem designs. The more digital circuitry present on the PC board, the more this attention to noise control is needed. The modem should be treated as a high impedance analog device. A 22 µF electrolytic capacitor in parallel with a 0.1µF ceramic capacitor between VDD and ground is recommended for supply bypassing. Liberal use of ground planes and larger traces on power and ground are also highly favored. High speed digital circuits tend to generate a significant amount of EMI (Electro-Magnetic Interference) which must be minimized in order to meet regulatory agency limitations. To accomplish this, high speed digital devices should be locally bypassed, and the DAA and K-Series device should be located close to each other near the area of the board where the phone line connection is accessed. To avoid problems, power supply and ground traces should be routed separately to the analog and digital functions on the board, and digital signals should not be routed near low level or high impedance analog traces. The analog and digital grounds should only connect at one point near the analog supplies to avoid ground loops. The K–Series modem IC's should have both high frequency and low frequency bypassing as near to the package as possible.

MODEM PERFORMANCE CHARACTERISTICS

The curves presented here define modem IC performance under a variety of line conditions while inducing disturbances that are typical of those encountered during data transmission on public service telephone lines. Test data was taken using an AEA Electronics' "Autotest I" modem test set and line simulator, operating under computer control. All tests were run full-duplex, using a Concord Data Systems 224 as the reference modem. A 511 pseudo-random-bit pattern was used with $1X10^6$ bits transmitted for each data point. Noise was C-message weighted and all signal-to-noise (S/N) ratios reflect total power measurements similar to the CCITT V.56 measurement specification. The individual tests are defined as follows.

BER vs.S/N

This test measures the ability of the modem to operate over noisy lines with a minimum of data-transfer errors. Since some noise is generated in the best of dial-up lines, the modem must operate with the lowest S/N ratio possible. Optimum modem performance is indicated by test curves that are closest to the zero axis. A narrow spread between curves representing the four line parameters indicates minimal variation in performance while operating over a range of aberrant operating conditions. Typically, a PSK modem will exhibit better BER-performance test curves operating in the highband range than in the lowband.

Ideal Receivers

The modem transmit function is easier to implement than the receive function. Because of this, it is generally assumed that only the receiver needs to be analyzed, but in practice this is not the case. Transmitter variations from unit to unit can affect overall modem performance. In this graph, the curve indicates the effect of the transmitter on the highband receive performance of an ideal receiver.

BER vs. Receive Level

This test measures the dynamic range of the modem. Because signal levels vary widely over dial-up lines, the widest possible dynamic range is desirable. The minimum Bell specification calls for 36 dB of dynamic range. S/N ratios are held constant at the indicated

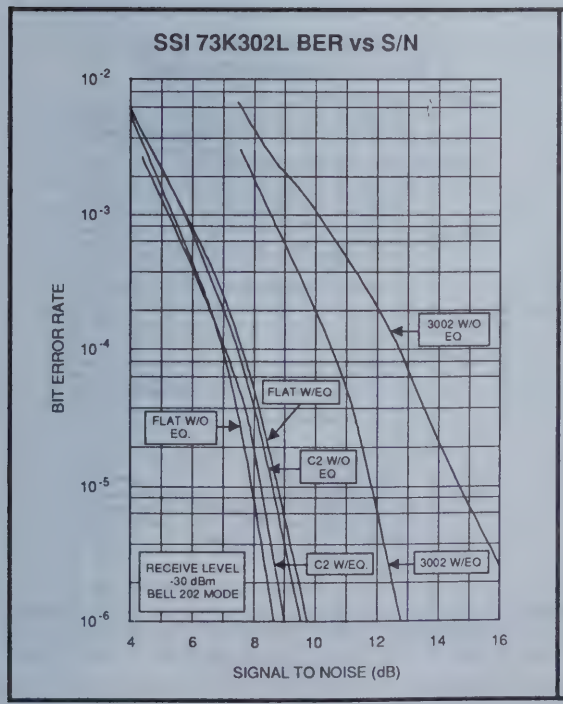
values while the receive level is lowered from a very high to very low signal levels. The width of the "bowl" of these curves, taken at the BER point, is the measure of dynamic range.

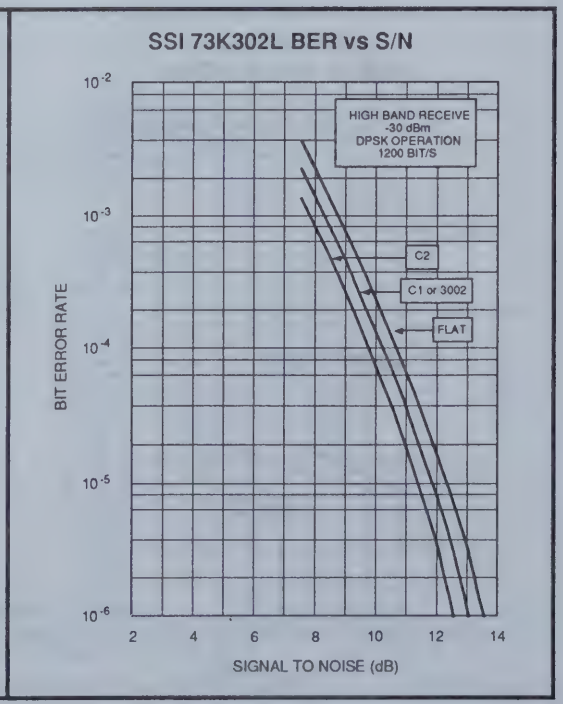
BER vs. Phase Jitter

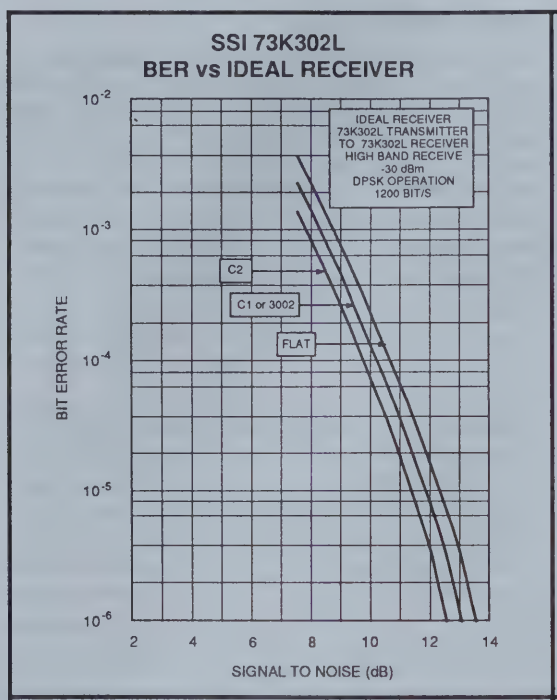
PSK and QAM modulation is sensitive to phase jitter. Modems using these techniques need to be as tolerant as possible of phase jitter on the line. In this test, relatively flat curves indicate minimal degradation of performance when phase jitter is encountered on the line.

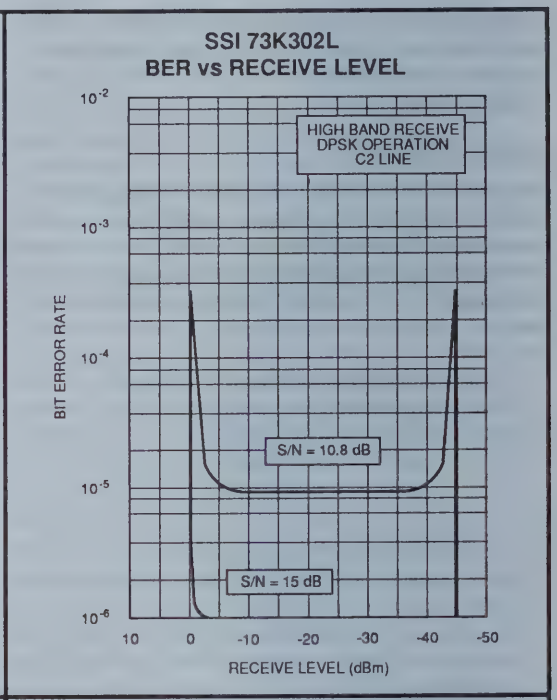
BER vs. Carrier Offset

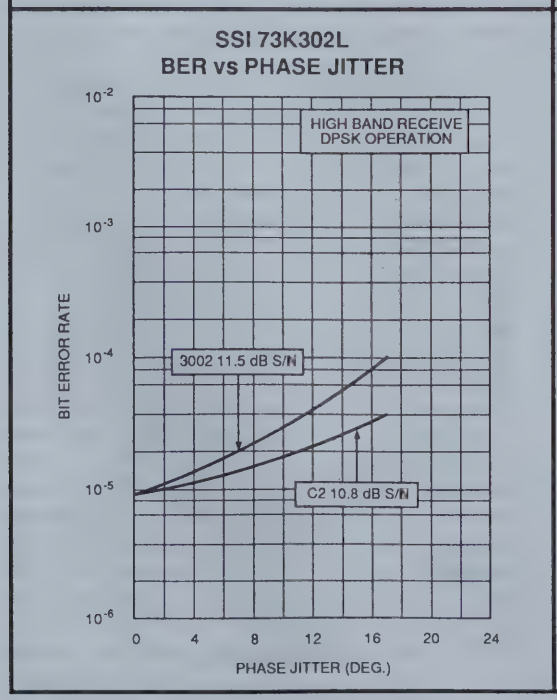
This parameter indicates how the modem's performance is affected by the shifts in frequency encountered in normal public telephone network operation. Flat curves are an indication that there is no performance degradation from frequency offsets. The SSI K-Series modem ICs use a second-order, carrier-tracking phase-lock-loop that is insensitive to carrier offsets in excess of 10 Hz. Both the Bell and European/Japanese CCITT specifications allow as much as 7-Hz offset.

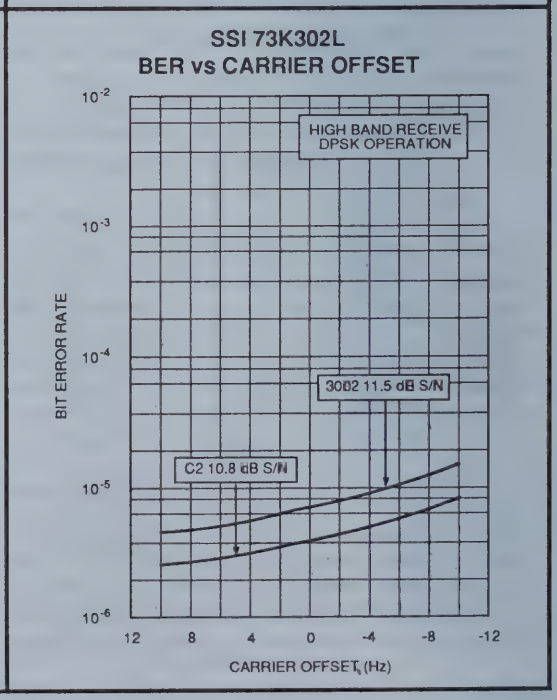





SSI 73K302L
BER vs IDEAL RECEIVER
IDEAL RECEIVER
73K302L TRANSMITTER
TO 73K302L RECEIVER
HIGH BAND RECEIVE
-30 dBm
DPSK OPERATION
1200 BIT/S
C2
C1 or 3002
FLAT
BIT ERROR RATE
SIGNAL TO NOISE (dB)

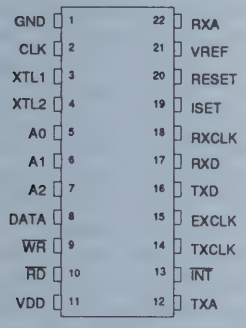

SSI 73K302L
BER vs RECEIVE LEVEL
HIGH BAND RECEIVE
DPSK OPERATION
C2 LINE
S/N = 10.8 dB
S/N = 15 dB
BIT ERROR RATE
RECEIVE LEVEL (dBm)


SSI 73K302L
BER vs PHASE JITTER
HIGH BAND RECEIVE
DPSK OPERATION
3002 11.5 dB S/N
C2 10.8 dB S/N
BIT ERROR RATE
PHASE JITTER (DEG.)

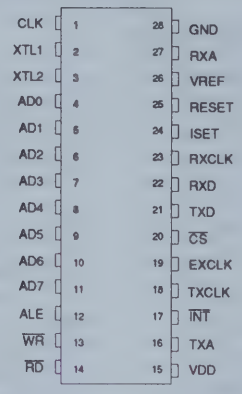

SSI 73K302L
BER vs CARRIER OFFSET
HIGH BAND RECEIVE
DPSK OPERATION
3002 11.5 dB S/N
C2 10.8 dB S/N
BIT ERROR RATE
CARRIER OFFSET (Hz)

PACKAGE PIN DESIGNATIONS

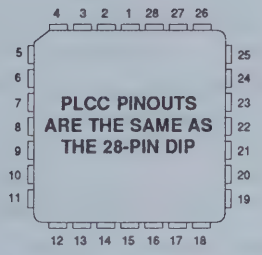
(TOP VIEW)



400-Mil
22-Pin DIP



600-Mil
28-Pin DIP



28-Lead
PLCC

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 73K302L with Parallel Bus Interface 28-Pin 5 Volt Supply		
Plastic Dual-In-Line	SSI 73K302L - IP	73K302L - IP
Plastic Leaded Chip Carrier	SSI 73K302L - IH	73K302L - IH
SSI 73K302L with Serial Interface 22-Pin 5 Volt Supply		
Plastic Dual-In-Line	SSI 73K302SL - IP	73K302SL - IP

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NOTES:

SSI 73K321L
CCITT V.23, V.21 Single-Chip Modem

July, 1989

1

DESCRIPTION

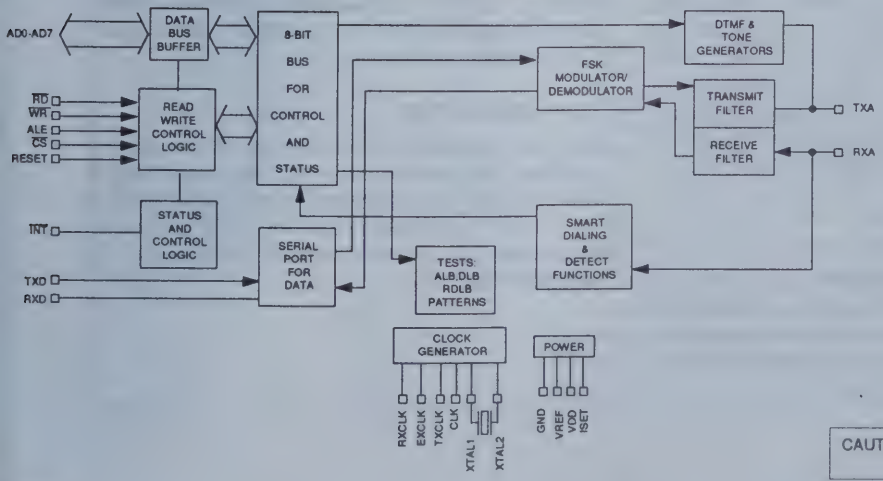
The SSI 73K321L is a highly integrated single-chip modem IC which provides the functions needed to construct a CCITT V.23 and V.21 compatible modem, capable of 0-300 bit/s full-duplex or 0-1200 bit/s half-duplex operation over dial-up telephone lines. The 73K321L provides 1200 bit/s operation in V.23 mode and allows 300 bit/s fallback in V.21 mode. The SSI 73K321L also can both detect and generate the 2100 Hz answer tone needed for call initiation. The SSI 73K321L integrates analog, digital, and switched-capacitor array functions on a single substrate,offering excellent performance and a high level of functional integration in a single 28- or 22-pin DIP configuration. The SSI 73K321L operates from a single +5 volt supply with very low power consumption.

The SSI 73K321L includes the FSK modulator/demodulator functions, call progress and handshake tone monitor test modes, and a tone generator capable of producing DTMF, answer, calling tones. The SSI 73K321L is designed to appear to the systems designer as a microprocessor peripheral, and will easily interface with popular one-chip microprocessors (80C51 typical) for control of modem functions through its 8-bit multiplexed address/data bus or via an optional serial command bus. An ALE control line simplifies address demultiplexing. Data communications occurs through a separate serial port only.

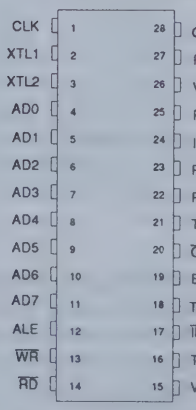
FEATURES

- One-chip CCITT V.23 and V.21 standard compatible modem
- Full-duplex operation at 0-300 bit/s (V.21) or 0–1200 bit/s (V.23) forward channel with or without 0–75 bits/s back channel
- Full Duplex 0-1200 bit/s (V.23) in 4-wire mode
- Pin and software compatible with other SSi K–Series 1-chip modems
- Interfaces directly with standard microprocessors (8048, 80C51 typical)
- Serial (22-pin DIP) or parallel microprocessor bus (28-pin DIP) for control
- Serial port for data transfer
- Call progress, carrier, precise answer tone (2100 Hz), calling tone (1300 Hz) and FSK mark detectors
- DTMF generator
- Test modes available: ALB, DL, RDL, Mark, Space, Alternating bit patterns
- Precise automatic gain control allows 45 dB dynamic range
- Space efficient 22- or 28-pin DIP packages
- CMOS technology for low power consumption using 30 mW @ 5V from a single power supply

BLOCK DIAGRAM



PIN DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

SSI 73K321L
CCITT V.23, V.21
Single-Chip Modem

OPERATION

The SSI 73K321L is ideal for either free standing or integral system modem applications where multi-standard data communications over the 2-wire switched telephone network is desired. Typical uses include videotex terminals, low-cost integral modems and built-in diagnostics for office automation or industrial control systems. The 73K321L's high functionality, low power consumption and efficient packaging simplify design requirements and increase system reliability in these applications. A complete modem requires only the addition of the phone line interface, a control microprocessor, and RS-232 level converter for a typical system. The SSI 73K321L is part of Silicon Systems K-Series family of pin and function compatible single-chip modem products. These devices allow systems to be configured for higher speeds and Bell or CCITT operation with only a single component change.

FSK MODULATOR/DEMODULATOR

The FSK modulator produces a frequency modulated analog output signal using two discrete frequencies to represent the binary data. V.21 mode uses 980 and 1180 Hz (originate, mark and space) or 1650 and 1850 Hz (answer, mark and space). V.23 mode uses 1300 and 2100 Hz for the main channel and 390 and 450 Hz for the back channel. The modulation rate of the back channel is up to 75 baud. Demodulation involves detecting the received frequencies and decoding them into the appropriate binary value.

PASSBAND FILTERS AND EQUALIZERS

A high and low band filter is included to shape the amplitude and phase response of the transmit and receive signals and provide compromise delay equalization and rejection of out-of-band signals in the receive channel. Amplitude and phase equalization are necessary to compensate for distortion of the transmission line and to reduce intersymbol interference in the bandlimited receive signal.

AGC

The automatic gain control maintains a signal level at the input to the demodulators which is constant to within 1 dB. It corrects quickly for increases in signal which would cause clipping and provides a total dynamic range of >45 dB.

PARALLEL BUS INTERFACE

Four 8-bit registers are provided for control, option select and status monitoring. These registers are addressed with the AD0, AD1, and AD2 multiplexed address lines (latched by ALE) and appear to a control microprocessor as four consecutive memory locations. Two control registers and the tone register are read/write memory. The status detect register is read only and cannot be modified except by modem response to monitored parameters. The parallel bus interface is not available with the 22-pin package.

SERIAL COMMAND INTERFACE

The serial command mode allows access to the SSI 73K321L control and status registers via a serial command port. In this mode the A0 , A1 and A2 lines provide register addresses for data passed through the data pin under control of the $\overline{RD}$ and $\overline{WR}$ lines. A read operation is initiated when the $\overline{RD}$ line is taken low. The next eight cycles of EXCLK will then transfer out eight bits of the selected address location LSB first. A write takes place by shifting in eight bits of data LSB first for eight consecutive cycles of EXCLK. $\overline{WR}$ is then pulsed low and data transferred into the selected register occurs on the rising edge of $\overline{WR}$.

SPECIAL DETECT CIRCUITRY

The special detect circuitry monitors the received analog signal to determine status or presence of carrier, answer tone and weak received signal (long loop condition), special tones such as FSK marking and the 1300 Hz calling tone are also detected. A highly frequency selective call progress detector provides adequate discrimination to accurately detect European call progress signals.

DTMF GENERATOR

The DTMF generator will output one of 16 standard dual-tones determined by a 4-bit binary value and TX DTMF mode bit previously loaded into the tone register. Dialing is initiated when the DTMF mode is selected and the transmit enable (CR0 bit D1) is changed from 0 to 1.

PIN DESCRIPTION

POWER

NAME	28-PIN	22-PIN	TYPE	DESCRIPTION
GND	28	1	I	System Ground.
VDD	15	11	I	Power supply input, 5V ±10%. Bypass with 0.1 and 22 µF capacitors to ground.
Vref	26	21	O	An internally generated reference voltage. Bypass with 0.1 µF capacitor to ground.
Iset	24	19	I	Chip current reference. Sets bias current for op-amps. The chip current is set by connecting this pin to VDD through a 2 MΩ resistor. Iset should be bypassed to GND with a 0.1 µF capacitor.

PARALLEL MICROPROCESSOR INTERFACE

ALE	12	-	I	Address latch enable. The falling edge of ALE latches the address on AD0-AD2 and the chip select on $\overline{CS}$.
AD0-AD7	4-11	-	I/O	Address/data bus. These bidirectional tri-state multiplexed lines carry information to and from the internal registers.
$\overline{CS}$	20	-	I	Chip select. A low on this pin allows a read cycle or a write cycle to occur. AD0-AD7 will not be driven and no registers will be written if $\overline{CS}$ (latched) is not active. $\overline{CS}$ is latched on the falling edge of ALE.
CLK	1	2	O	Output clock. This pin is selectable under processor control to be either the crystal frequency (for use as a processor clock) or 16 x the data rate for use as a baud rate clock. The pin defaults to the crystal frequency on reset.
$\overline{INT}$	17	13	O	Interrupt. This open drain output signal is used to inform the processor that a detect flag has occurred. The processor must then read the detect register to determine which detect triggered the interrupt. $\overline{INT}$ will stay active until the processor reads the detect register or does a full reset.
$\overline{RD}$	14	-	I	Read. A "low" requests a read of the SSI 73K321L internal registers. Data cannot be output unless both $\overline{RD}$ and the latched $\overline{CS}$ are active or "low."
RESET	25	20	I	Reset. An active signal "high" on this pin will put the chip into an inactive state. All control register bits (CR0, CR1, Tone) will be reset. The output of the CLK pin will be set to the crystal frequency. An internal pull down resistor permits power on reset using a capacitor to VDD.

PIN DESCRIPTION (Continued)

PARALLEL MICROPROCESSOR INTERFACE (Continued)

NAME	28-PIN	22-PIN	TYPE	DESCRIPTION
$\overline{WR}$	13	-	I	Write. A "low" on this informs the SSI 73K321L that data is available on AD0-AD7 for writing into an internal register. Data is latched on the rising edge of $\overline{WR}$. No data is written unless both $\overline{WR}$ and the latched $\overline{CS}$ are active ("low").

SERIAL MICROPROCESSOR INTERFACE

A0-A2	-	5-7	I	Register Address Selection. These lines carry register addresses and should be valid during any read or write operation.
DATA	-	8	I/O	Serial Control Data. Data for a read/write operation is clocked in or out on the falling edge of the EXCLK pin. The direction of data flow is controlled by the $\overline{RD}$ pin. $\overline{RD}$ low outputs data. $\overline{RD}$ high inputs data.
$\overline{RD}$	-	10	I	Read. A "low" on this input informs the SSI 73K321L that data or status information is being read by the processor. The falling edge of the $\overline{RD}$ signal will initiate a read from the addressed register. The $\overline{RD}$ signal must continue for eight falling edges of EXCLK in order to read all eight bits of the referenced register. Read data is provided LSB first. Data will not be output unless the $\overline{RD}$ signal is active.
$\overline{WR}$	-	9	I	Write. A "low" on this input informs the SSI 73K321L that data or status information has been shifted in through the DATA pin and is available for writing to an internal register. The normal procedure for a write is to shift in data LSB first on the DATA pin for eight consecutive falling edges of EXCLK and then to pulse $\overline{WR}$ low. Data is written on the rising edge of $\overline{WR}$.

Note: In the serial, 22-pin version, the pins AD0-AD7, ALE and $\overline{CS}$ are removed and replaced with the pins; A0, A1, A2, DATA, and an unconnected pin. Also, the $\overline{RD}$ and $\overline{WR}$ controls are used differently.

The serial control mode is provided in the 28-pin version by tying ALE high and $\overline{CS}$ low. In this configuration AD7 becomes DATA and AD0, AD1 and AD2 become A0, A1 and A2, respectively.

RS-232 INTERFACE

NAME	28-PIN	22-PIN	TYPE	DESCRIPTION
EXCLK	19	15	I	External Clock. Used for serial control interface to clock control data in or out of the 73K321L.
RXCLK	23	18	O	Receive Clock. A clock which is 16 x1200 or 16 x 300 baud data rate is output in either V.23 or V.21, respectively.
RXD	22	17	O	Received Digital Data Output. Serial receive data is available on this pin. The data is always valid on the rising edge of RXCLK when in synchronous mode. RXD will output constant marks if no carrier is detected.
TXCLK	18	14	O	Transmit Clock. TXCLK is always active. In V.23 or V.21 mode the output is either a 16 x 1200 baud clock or 16 x 300 baud clock, respectively.
TXD	21	16	I	Transmit Digital Data Input. Serial data for transmission is input on this pin. In asynchronous modes (1200 or 300 baud) no clocking is necessary.

ANALOG INTERFACE

RXA	27	22	I	Received modulated analog signal input from the phone line.
TXA	16	12	O	Transmit analog output to the phone line.
XTAL1 XTAL2	2 3	3 4	I I, O	These pins are for the internal crystal oscillator requiring a 11.0592 MHz parallel mode crystal and two load capacitors to Ground. XTAL2 can also be driven from an external clock.

REGISTER DESCRIPTIONS

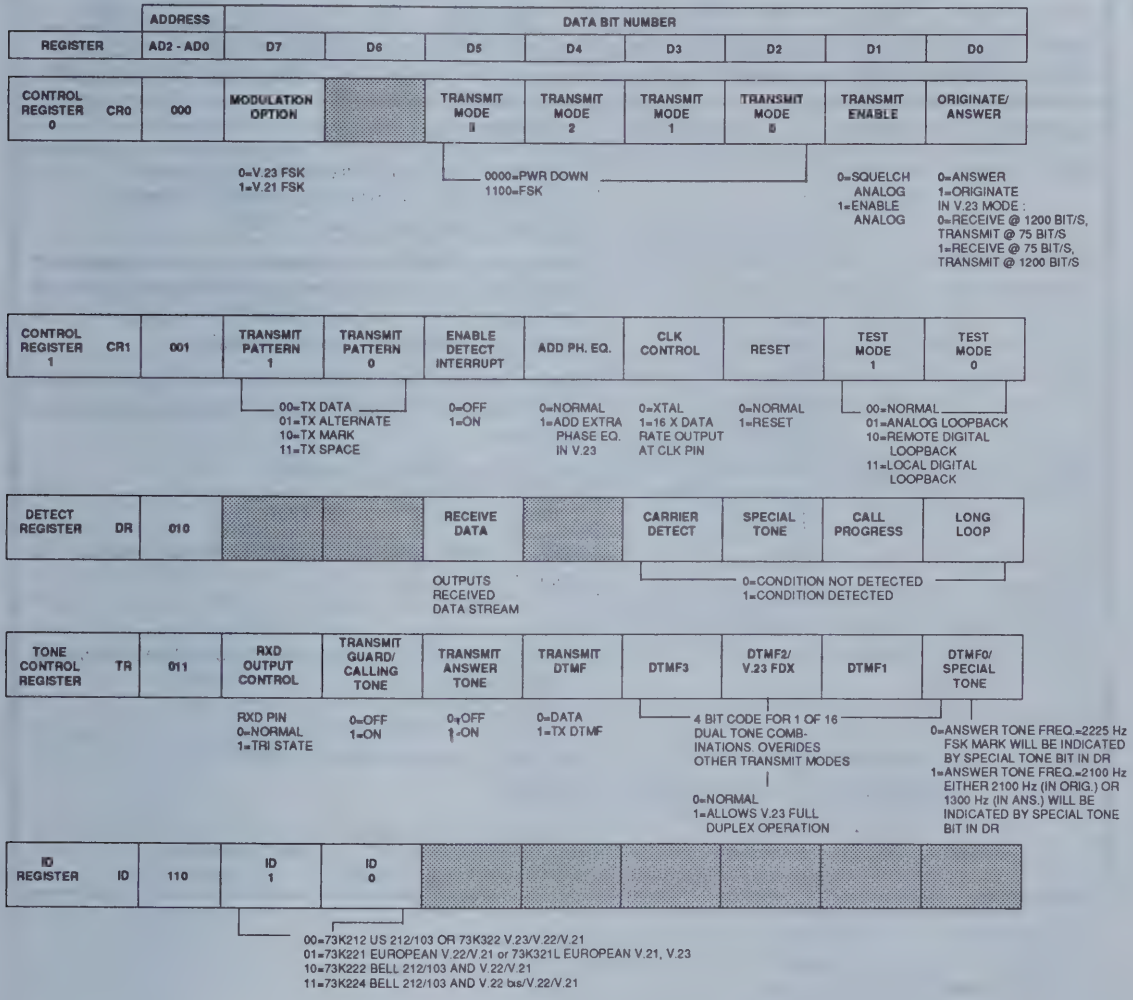
Four 8-bit internal registers are accessible for control and status monitoring. The registers are accessed in read or write operations by addressing the A0 and A1 address lines in serial mode, or the AD0 and AD1 lines in parallel mode. The AD0 and AD1 lines are latched by ALE. Register CR0 controls the method by which data is transferred over the phone line. CR1 controls the interface between the microprocessor and the SSI 73K321L internal state. DR is a detect register which provides an indication of monitored modem status conditions. TR, the tone control register, controls the DTMF generator, answer and guard tones and RX output gate used in the modem initial connect sequence. All registers are read/write except for DR which is read only. Register control and status bits are identified below:

REGISTER BIT SUMMARY

		ADDRESS	DATA BIT NUMBER							
REGISTER		AD2 - AD0	D7	D6	D5	D4	D3	D2	D1	D0
CONTROL REGISTER 0	CR0	000	MODULATION OPTION		TRANSMIT MODE 3	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ANSWER/ ORIGINATE
CONTROL REGISTER 1	CR1	001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTERRUPT	ADD PH. EQ. (V.23)	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0
DETECT REGISTER	DR	010			RECEIVE DATA		CARRIER DETECT	SPECIAL TONE	CALL PROGRESS	LONG LOOP
TONE CONTROL REGISTER	TR	011	RXD OUTPUT CONTROL	TRANSMIT CALLING TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF3	DTMF2	DTMF1	DTMF0/ ANSWER/SPEC. TONE SELECT
CONTROL REGISTER 2	CR2	100				THESE REGISTER LOCATIONS ARE RESERVED FOR				
CONTROL REGISTER 3	CR3	101				USE WITH OTHER K-SERIES FAMILY MEMBERS				
ID REGISTER	ID	110	0	0						

NOTE: When a register containing reserved control bits is written into, the reserved bits must be programmed as 0's.

REGISTER ADDRESS TABLE



CONTROL REGISTER 0

	D7	D6	D5	D4	D3	D2	D1	D0
CR0 000	MODUL. OPTION		TRANSMIT MODE 3	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ANSWER/ ORIGINATE

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	Answer/ Originate	0	Selects answer mode (transmit in high band, receive in low band or in V.23 mode, receive at 1200 bit/s and transmit at 75 bit/s).
		1	Selects originate mode (transmit in low band,receive in high band or in V.23 mode, receive at 75 bps and transmit at 1200 bit/s). If in V.23 and D2 of TR=1, selects V.23 full duplex operation in 4-wire configuration.
			Note: This bit works with TR bit D0 to program special tones detected in Tone Register. See detect and tone registers.
D1	Transmit Enable	0	Disables transmit output at TXA.
		1	Enables transmit output at TXA.
			Note: Answer tone and DTMF TX control require TX enable.
D5, D4,D3, D2	Transmit Mode	D5 D4 D3 D2	
		0 0 0 0	Selects power down mode. All functions disabled except digital interface.
		1 1 0 0	Selects FSK operation.
D6	Unused	0	Not used; must be written as a "0."
D7	Modulation Option	D7 D5 D4	Selects:
		0 1 1	FSK CCITT V.23 mode.
		1 1 1	FSK CCITT V.21 mode.

CONTROL REGISTER 1

	D7	D6	D5	D4	D3	D2	D1	D0
CR1 001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTER.	ADD PH. EQ.	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0

BIT NO.	NAME	CONDITION	DESCRIPTION
D1, D0	Test Mode	D1 D0	
		0 0	Selects normal operating mode.
		0 1	Analog loopback mode. Loops the transmitted analog signal back to the receiver, and causes the receiver to use the same center frequency as the transmitter. To squelch the TXA pin, transmit enable must be forced low.
		1 0	Selects remote digital loopback. Received data is looped back to transmit data internally, and RXD is forced to a mark. Data on TXD is ignored.
		1 1	Selects local digital loopback. Internally loops TXD back to RXD and continues to transmit data from TXA pin.
D2	Reset	0	Selects normal operation.
		1	Resets modem to power down state. All control register bits (CR0, CR1, Tone) are reset to zero. The output of the clock pin will be set to the crystal frequency.
D3	CLK Control (Clock Control)	0	Selects 11.0592 MHz crystal echo output at CLK pin.
		1	Selects 16 X the data rate. (16 x 75 or 300 or 1200 Hz.)
D4	Add Ph. Eq.	0	Selects normal equalization.
		1	In V.23 mode, additional phase equalization is added to the main channel filters when D4 is set to 1.
D5	Enable Detect Interrupt	0	Disables interrupt at $\overline{INT}$ pin. All interrupts are normally disabled in power down modes.
		1	Enables $\overline{INT}$ output. An interrupt will be generated with a change in status of DR bits D1-D3. The special tone and call progress detect interrupts are masked when the TX enable bit is set. Carrier detect is masked when TX DTMF is activated. All interrupts will be disabled if the device is in power down mode.
D7, D6	Transmit Pattern	D7 D6	
		0 0	Selects normal data transmission as controlled by the state of the TXD pin.
		0 1	Selects an alternating mark/space transmit pattern for modem testing.
		1 0	Selects a constant mark transmit pattern.
		1 1	Selects a constant space transmit pattern.

DETECT REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
DR 010			RECEIVE DATA		CARR. DETECT	SPECIAL TONE	CALL PROG.	LONG LOOP

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	Long Loop	0	Indicates normal received signal.
		1	Indicates low received signal level.
D1	Call Progress Detect	0	No call progress tone detected.
		1	Indicates presence of call progress tones. The call progress detection circuitry is activated by energy in the normal 350 to 620 Hz call progress band.
D2	Special Tone Detect	0	No special tone detected as programmed by CR0 bit D0 and Tone Register bit D0.
		1	Special tone detected. The detected tone is:
			(1) 2100 Hz answer tone if D0 of TR=1 and the device is in V.21 originate mode.
			(2) 1300 Hz calling tone if D0 of TR=1 and the device is in V.21 or V.23 answer mode.
			(3) an FSK mark for the mode the device is set to receive in if D0 of TR = 0.
			NOTE: Tolerance on special tones is ±3%.
D3	Carrier Detect	0	No carrier detected in the receive channel.
		1	Indicated carrier has been detected in the received channel.
D4	Unused		Not used in the 73K321L.
D5	Receive Data		Continuously outputs the received data stream. This data is the same as that output on the RXD pin, but it is not disabled when RXD is tri-stated.
D6, D7			Not used.

TONE REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
TR 011	RXD OUTPUT CONTR.	TRANSMIT CALLING TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF 3	DTMF 2	DTMF 1	DTMF 0/ ANS. TONE/ SPECIAL TONE/ SEL

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	DTMF 0/	D6 D5 D4 D0	D0 interacts with bits D6, D5, D4, and CR0 as shown.
	Answer Tone/	X X 1 X	Transmit DTMF tones.
	Special Tone/ Detect/Select	X X 0 0	Mark of an FSK mode selected in CR0 is to be detected in D2 of DR.
		X X 0 1	2100 Hz answer tone will be detected in D2 of DR if V.21 originate mode is selected in CR0.
			1300 Hz calling tone will be detected in D2 of DR if V.21 or V.23 answer mode is selected in CR0.
		X 1 0 0	Transmit 2225 Hz answer tone in answer mode.
		X 1 0 1	Transmit 2100 Hz answer tone in answer mode.
D3, D2, D1, D0	DTMF 3, 2, 1, 0	D3 D2 D1 D0	
		0 0 0 0 - 1 1 1 1	Programs 1 of 16 DTMF tone pairs that will be transmitted when TX DTMF and TX enable bit (CR0, bit D1) is set. Tone encoding is shown below:

KEYBOARD EQUIVALENT	DTMF CODE D3 D2 D1 D0	TONES LOW	HIGH
1	0 0 0 1	697	1209
2	0 0 1 0	697	1336
3	0 0 1 1	697	1477
4	0 1 0 0	770	1209
5	0 1 0 1	770	1336
6	0 1 1 0	770	1477
7	0 1 1 1	852	1209
8	1 0 0 0	852	1336
9	1 0 0 1	852	1477
0	1 0 1 0	941	1336

TONE REGISTER (Continued)

BIT NO.	NAME	CONDITION	DESCRIPTION					
D3, D2, D1, D0 (Cont.)			KEYBOARD EQUIVALENT	DTMF CODE D3	D2	D1	D0	TONES LOW	HIGH
			*	1	0	1	1	941	1209
			#	1	1	0	0	941	1477
			A	1	1	0	1	697	1633
			B	1	1	1	0	770	1633
			C	1	1	1	1	852	1633
			D	0	0	0	0	941	1633
D4	TX DTMF (Transmit DTMF)	0	Disabled DTMF.						
		1	Activates DTMF. The selected DTMF tones are transmitted continuously when this bit is high. TX DTMF overrides all other transmit functions.						
D5	TX ANS (Transmit Answer tone)	0	Disables answer tone generator.						
		1	Enables answer tone generator. A 2100 Hz answer tone will be transmitted continuously when the transmit enable bit is set. The device must be in answer mode.						
D6	TX Calling Tone (Transmit Calling Tone)	0	Disables calling tone generator.						
		1	Transmit calling tone in either mode.						
D7	RXD Output Control	0	Enables RXD pin. Receive data will be output on RXD.						
		1	Disables RXD pin. The RXD pin reverts to a high impedance with internal weak pull-up resistor.						

ID REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
ID 110	ID 1	ID 0						

BIT NO.	NAME	CONDITION	DESCRIPTION
D7, D6	Device Identification Signature	D7 D6	Indicates Device:
		0 0	SSI 73K212(L) or 73K322L
		0 1	SSI 73K221(L) or 73K321L
		1 0	SSI 73K222(L)
		1 1	SSI 73K224(L)

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
VDD Supply Voltage	14	V
Storage Temperature	-65 to 150	°C
Soldering Temperature (10 sec.)	260	°C
Applied Voltage	-0.3 to VDD+0.3	V

Note: All inputs and outputs are protected from static charge using built-in, industry standard protection devices and all outputs are short-circuit protected.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
VDD Supply Voltage		4.5	5	5.5	V
Digital Pins					
VIH, Input High Voltage					
Reset, XTAL 1		3.0		VDD	V
All other inputs		2.0		VDD	V
VIL, Input Low Voltage		0		0.8	V
IOH, Output High Current		-0.4			mA
IOL, Output Low Current				1.6	mA
TA, Operating Free-Air Temperature		-40		+85	°C
External Components*					
VREF Bypass capacitor	(External to GND)	0.1			µF
Bias setting resistor	(Placed between VDD and ISET pins)	1.8	2	2.2	MΩ
ISET Bypass capacitor	(ISET pin to GND)	0.1			µF
VDD Bypass capacitor 1	(External to GND)	0.1			µF
VDD Bypass capacitor 2	(External to GND)	22			µF

*Refer to Application section for placement.

DC ELECTRICAL CHARACTERISTICS

(TA = -40°C to 85°C, VDD = recommended range unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
IDD, Supply Current	CLK = 11.0592 MHz				
IDDA, Active	ISET Resistor = 2 MΩ		7	10	mA
IDD1, Power-down	CLK = 11.0592 MHz			4	mA
IDD2, Power-down	CLK = 19.200 KHz			3	mA
Digital Inputs					
IIH, Input High Current	VI = VIH Max			100	µA
IIL, Input Low Current	VI = VIL Min	-200			µA
Reset Pull-down Current	Reset = VDD	1		50	µA
Digital Outputs					
VOH, Output High Voltage	IO = IOH MIN	2.4		VDD	V
VOL, Output Low Voltage	IO = IO MAX			0.4	V
VOL, CLK Output	IO = 3.6 mA			0.6	V
RXDTri-State Pull-up Curr.	RXD = GND	-1		-50	µA
Capacitance					
Inputs	Capacitance, all Digital Input pins			10	pF
XTAL1, 2 Load Capacitors	Depends on crystal	15		60	pF
CLK	Maximum Capacitive Load			15	pF

DYNAMIC CHARACTERISTICS AND TIMING

(TA = -40°C to +85°C, VDD = Recommended range unless otherwise noted.)

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNITS
FSK Modulator					
Output Freq. Error	CLK = 11.0592 MHz	-0.35		+.35	%
Transmit Level	Transmit Dotting Pattern	-11	-10	-9	dBm0
Harmonic Distortion in 700-2900 Hz band	THD in the alternate band FSK		-60	-50	dB
Output Bias Distortion	Transmit Dotting Pattern In ALB @ RXD		±8		%
Total Output Jitter	Random Input in ALB @ RXD	-10		+10	%

NOTE: Parameters expressed in dBm0 refer to the following definition:

0 dB loss in the Transmit path to the line.

2 dB gain in the Receive path from the line.

Refer to the Basic Box Modem diagram in the Applications section for the DAA design.

DYNAMIC CHARACTERISTICS AND TIMING (Continued)

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNITS
DTMF Generator					
Freq. Accuracy		-.25		+.25	%
Output Amplitude	Low Band	-10	-9	-8	dBm0
Output Amplitude	High Band	-8	-7	-6	dBm0
Twist	High-Band to Low-Band	1.0	2.0	3.0	dB
Long Loop Detect	Not valid for V.23 back channel	-38		-28	dBm0
Dynamic Range	Refer to Performance Curves		45		dB
Call Progress Detector					
Detect Level	-3 dB points in 285 and 675 Hz	-38			dBm0
Reject Level	Test signal is a 460 Hz sinusoid			-45	dBm0
Delay Time	-70 dBm0 to -30 dBm0 STEP	20		40	ms
Hold Time	-30 dBm0 to -70 dBm0 STEP	20		40	ms
Hysteresis		2			dB
Carrier Detect					
Threshold	Single Tone	-49		-42	dBm0
Delay Time					
V.21		13		20	ms
V.23 Forward Channel		7		12	ms
V.23 Back Channel		25		40	ms
Hold Time					
V.21		7		20	ms
V.23 Forward Channel		4		8	ms
V.23 Back Channel		20		30	ms
Hysteresis		2			dB

DYNAMIC CHARACTERISTICS AND TIMING (Continued)

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNITS
Special Tone Detectors					
Detect Level	See definitions for TR bit D0 mode	-48		-43	dBm0
Delay Time					
2100 Hz answer tone		15		35	ms
1300 Hz calling tone		13		20	ms
390 Hz V.23 back channel mark		25		60	ms
980 or 1650 Hz V.21 marks		15		30	ms
Hold Time					
2100 Hz answer tone		4		24	ms
1300 Hz calling tone		4		24	ms
390 Hz V.23 back channel mark		20		30	ms
980 or 1650 Hz V.21 marks		7		20	ms
Hysteresis		2			dB
Detect Freq. Range	Any Special Tone	-3		+3	%
Output Smoothing Filter					
Output load	TXA pin; FSK Single Tone out for THD = -50 dB in .3 to 3.4 KHz	10		 50	KΩ pF
Out of Band Energy	Frequency >12KHz in all modes			-70	dBm0
Output Impedance	TXA pin		200	300	Ω
Clock Noise	TXA pin; 76.8 KHz or 122.88 KHz inV.23 main channel			0.4	mVrms

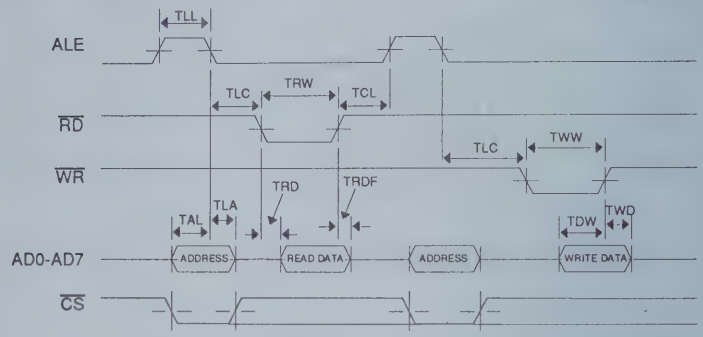
DYNAMIC CHARACTERISTICS AND TIMING (Continued)

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNITS
Timing (Refer to Timing Diagrams)					
TAL	$\overline{CS}$/Addr. setup before ALE	30			ns
TLA	$\overline{CS}$/Addr. Hold after latch	20			ns
TLC	Latch to $\overline{RD}$/$\overline{WR}$ control	40			ns
TCL	$\overline{RD}$/$\overline{WR}$ Control to Latch	10			ns
TRD	Data out from $\overline{RD}$	0		160	ns
TLL	ALE width	60			ns
TRDF	Data float after READ	0		80	ns
TRW	READ width	200		25000	ns
TWW	WRITE width	140		25000	ns
TDW	Data setup before WRITE	150			ns
TWD	Data hold after WRITE	20			ns
TCKD	Data out after CLK			200	ns
TCKW	WRITE after CLK	150			ns
TDCK	Data setup before CLK	150			ns
TAC	Address setup before control [1]	50			ns
TCA	Address hold after control [1]	50			ns

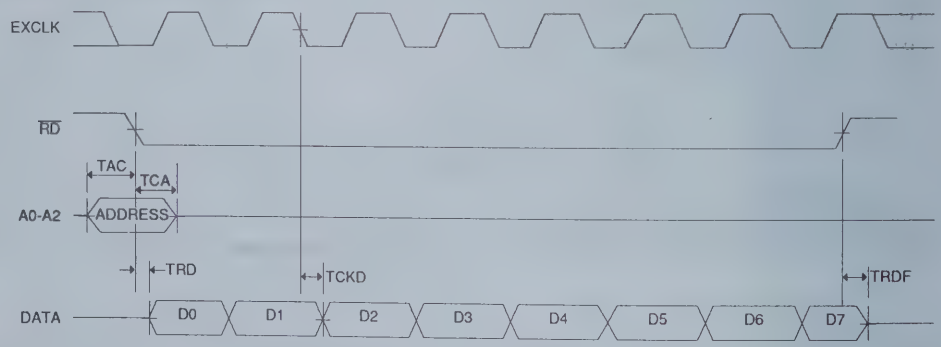
[1]Control for setup is the falling edge of $\overline{RD}$ or $\overline{WR}$.
Control for hold is the falling edge of $\overline{RD}$ or the rising edge of $\overline{WR}$.

TIMING DIAGRAMS

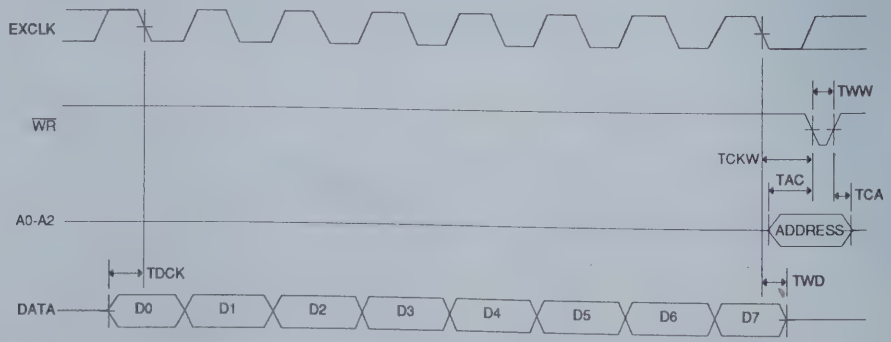
BUS TIMING DIAGRAM (PARALLEL VERSION)



READ TIMING DIAGRAM (SERIAL VERSION)



WRITE TIMING DIAGRAM (SERIAL VERSION)



APPLICATIONS INFORMATION

GENERAL CONSIDERATIONS

Figures 1 and 2 show the basic circuit diagram for K–Series modem integrated circuits. K-Series products are designed to be used in conjunction with a control processor, a UART or RS-232 serial data interface, and a DAA phone line interface to function as a typical intelligent modem. The K-Series ICs interface directly with Intel 8048 and 80C51 microprocessors for control and status monitoring purposes. Two typical DAA arrangements are shown: one for a split ±5 or ±12 volt design and one for a single 5 volt design. These diagrams are for reference only and do not represent production-ready modem designs.

K-Series devices are available in two control interface versions: one for a parallel multiplexed address/data interface, and one for a serial interface. The parallel version is intended for use with 8039/48 or 8031/51 microcontrollers from Intel or many other manufacturers. The serial interface 22-pin version can be used with other microcontrollers or in applications where only a limited number of port lines are available. The parallel versions may also be used in the serial mode, as explained in the data sheet pin description.

In most applications the controller will monitor the serial data for commands from the DTE and the received data for break signals from the far end modem. In this way, command data to the modem is sent over the same data line as the transmitted data. In other applications the RS-232 interface handshake lines are used for modem control.

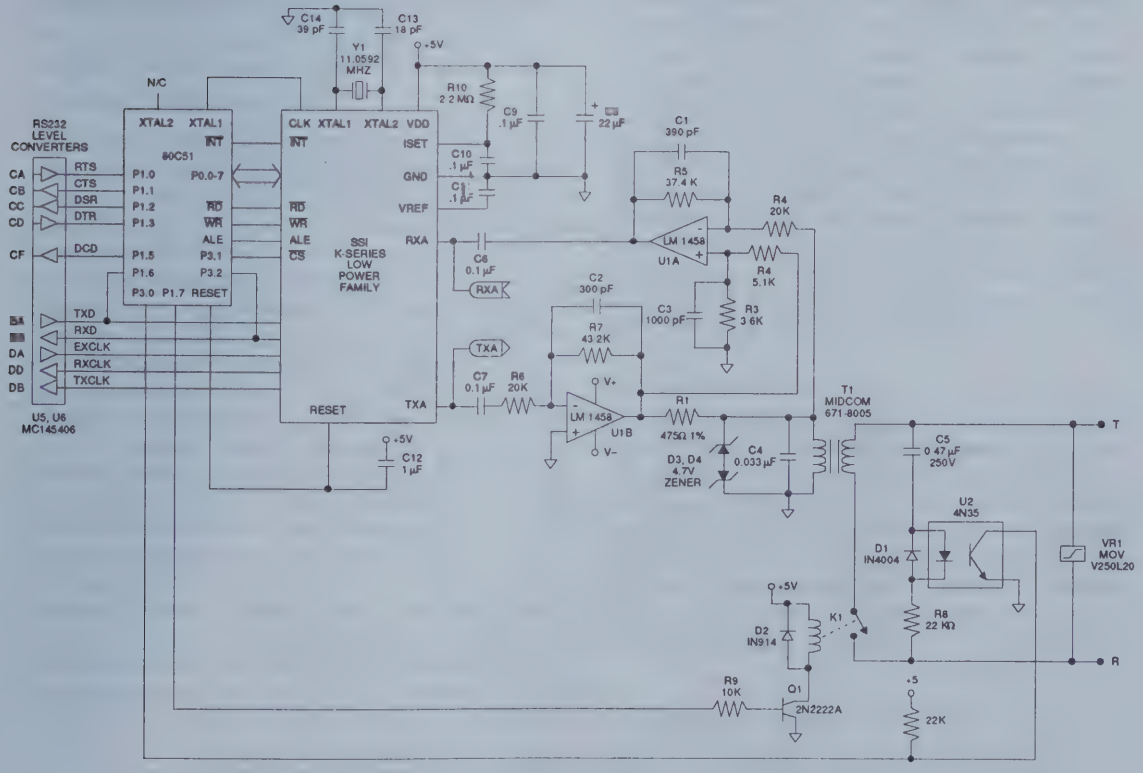


FIGURE 1: Basic Box Modem with Dual-Supply DAA

DIRECT ACCESS ARRANGEMENT (DAA)

The DAAs shown are two examples of how the "hybrid" may be implemented. The split supply design (Figure 1) is a typical two op-amp hybrid. The receive op-amp serves two purposes. It supplies gain to amplify the receive signal to the proper level for the modem's detectors and demodulator, and it removes the transmitted signal from the receive signal present at the transformer. This is done by supplying a portion of the transmitted signal to the non-inverting input of the receive op-amp at the same amplitude as the signal appearing at the transformer, making the transmit signal common mode.

The single-supply DAA is more complex than the dual-supply version described above, but its use eliminates the need for a second power supply. This DAA (Figure 2) uses a bridged drive to allow undistorted signals to be sent with a single 5 volt supply. Because DTMF tones utilize a higher amplitude than data, these signals will clip if a single-ended drive approach is used. The bridged driver uses an extra op-amp (U1A) to invert the signal coming from the gain setting op-amp (U1B) before sending it to the other leg of the transformer. Each op-amp then supplies half the drive signal to the transformer. The receive amplifier (op-amp C) picks off its signal at the junction of the impedance matching resistor and the transformer. Because the bottom leg of the transformer is being driven in one direction by U1A and the resistor is driven in the opposite direction at the same time by U1B, the summing point of the transformer and resistor remains relatively constant and the receive signal is unaffected.

DESIGN CONSIDERATIONS

Silicon Systems 1-chip modem products include all basic modem functions on a single IC, accessible from a standard bus interface. This makes these devices adaptable for use in a variety of applications, and as easy to control as conventional digital bus peripherals.

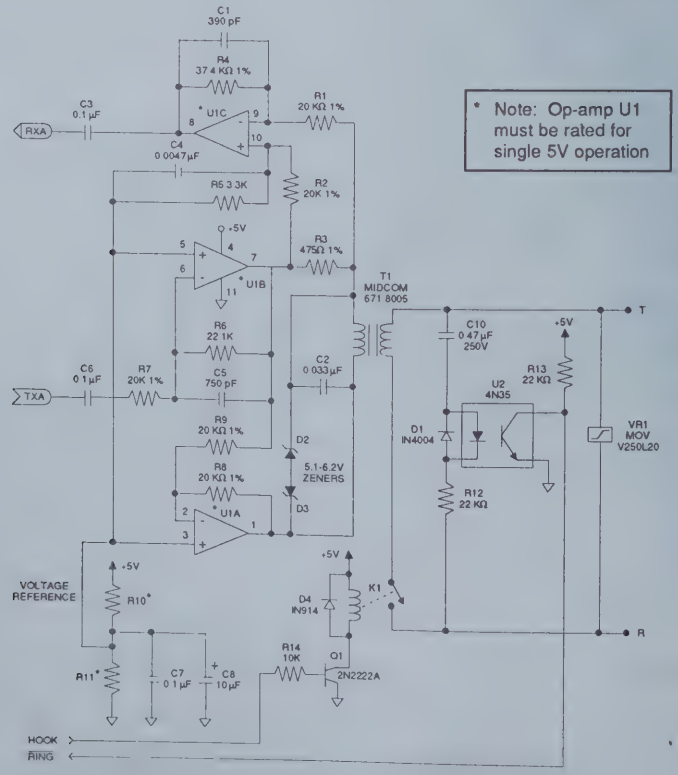


FIGURE 2: Single 5V DAA Version

Unlike digital logic circuitry, however, modem designs must properly contend with precise frequency tolerances, and very low level analog signals, to insure acceptable performance. Using good analog circuit design practices will generally result in a sound design. Folllowing are additional recommendations which should be taken into consideration when starting new designs.

CRYSTAL OSCILLATOR

The K-Series crystal oscillator requires a parallel mode (antiresonant) crystal which operates at 11.0592 MHz. It is important that this precise frequency be maintained to within ±.01% accuracy.

In order for a parallel mode crystal to operate correctly and to specification, it must have a load capacitor connected to the junction of each of the crystal and internal inverter connections, terminated to ground. The values of these capacitors depend primarily on the crystal's characteristics, and to a lesser degree on the internal inverter circuit. The values used affect the accuracy and start up characteristics of the oscillator.

LAYOUT CONSIDERATIONS

Good analog/digital design rules must be used to control system noise in order to obtain highest performance in modem designs. The more digital circuitry present on the PC board, the more this attention to noise control is needed. The modem should be treated as a high impedance analog device. A 10 µF electrolytic capacitor in parallel with a 0.1 µF ceramic capacitor between VDD and ground is recommended. Liberal use of ground planes and larger traces on power and ground are also highly favored. High speed digital circuits tend to generate a significant amount of EMI (Electro-Magnetic Interference) which must be minimized in order to meet regulatory agency limitations. To accomplish this, high speed digital devices should be locally bypassed, and the DAA and K-Series device should be located close to each other near the area of the board where the phone line connection is accessed. To avoid problems, power supply and ground traces should be routed separately to the analog and digital functions on the board, and digital signals should not be routed near low level or high impedance analog traces. The analog and digital grounds should only connect at one point near the analog supplies to avoid ground loops. The K–Series modem IC's should have both high frequency and low frequency bypassing as near to the package as possible.

MODEM PERFORMANCE CHARACTERISTICS

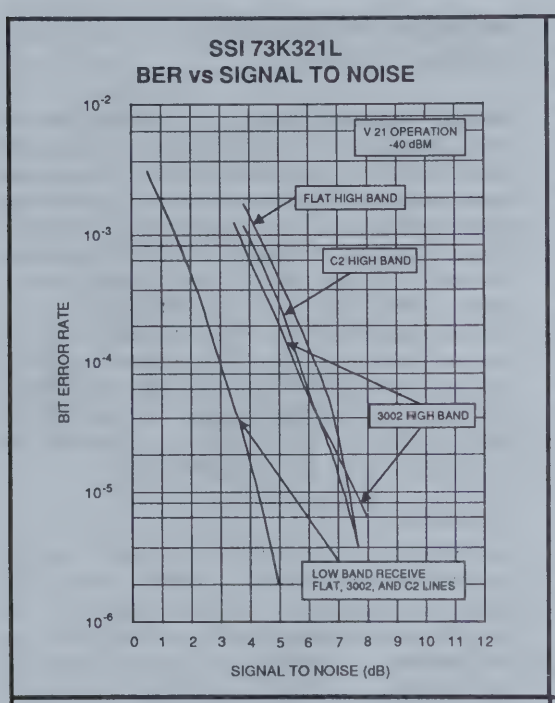
The curves presented here define modem IC performance under a variety of line conditions while inducing disturbances that are typical of those encountered during data transmission on public service telephone lines. Test data was taken using an AEA Electronics' "Autotest I" modem test set and line simulator, operating under computer control. All tests were run full-duplex, using a Concord Data Systems 224 as the reference modem. A 511 pseudo-random-bit pattern was used with $1X10^6$ bits transmitted for each data point. Noise was C-message weighted and all signal-to-noise (S/N) ratios reflect total power measurements similar to the CCITT V.56 measurement specification. The individual tests are defined as follows.

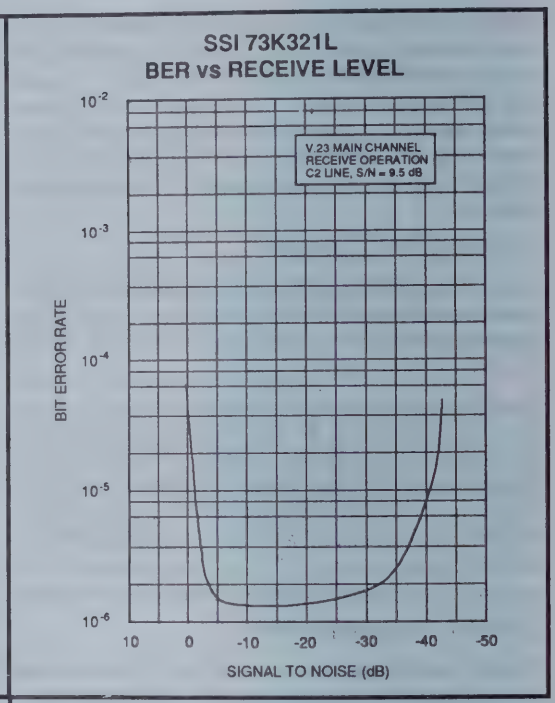
BER vs.S/N

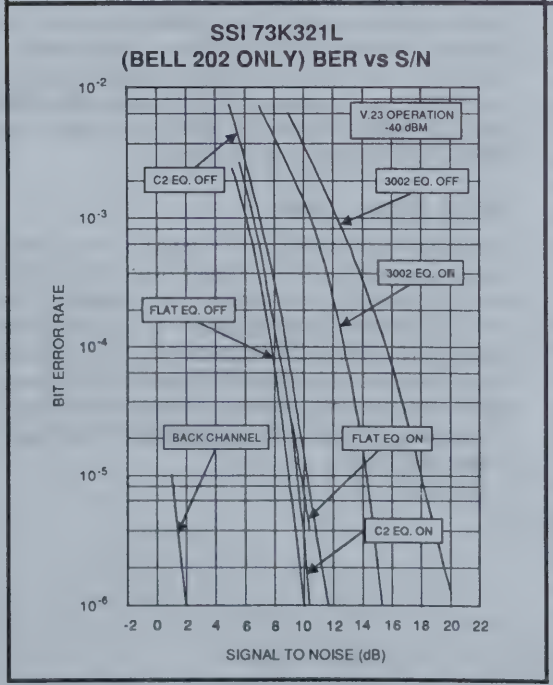
This test measures the ability of the modem to operate over noisy lines with a minimum of data-transfer errors. Since some noise is generated in the best of dial-up lines, the modem must operate with the lowest S/N ratio possible. Optimum modem performance is indicated by test curves that are closest to the zero axis. A narrow spread between curves representing the four line parameters indicates minimal variation in performance while operating over a range of aberrant operating conditions. Typically, a PSK modem will exhibit better BER-performance test curves operating in the highband range than in the lowband.

BER vs. Receive Level

This test measures the dynamic range of the modem. Because signal levels vary widely over dial-up lines, the widest possible dynamic range is desirable. The minimum Bell specification calls for 36 dB of dynamic range. S/N ratios are held constant at the indicated values while the receive level is lowered from a very high to very low signal levels. The width of the "bowl" of these curves, taken at the BER point, is the measure of dynamic range.

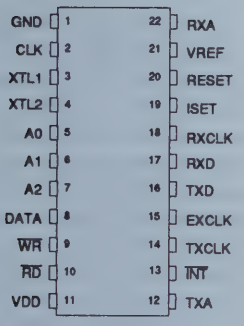

SSI 73K321L
BER vs SIGNAL TO NOISE
BIT ERROR RATE
10^{-2}
10^{-3}
10^{-4}
10^{-5}
10^{-6}
V 21 OPERATION
-40 dBM
FLAT HIGH BAND
C2 HIGH BAND
3002 HIGH BAND
LOW BAND RECEIVE
FLAT, 3002, AND C2 LINES
0 1 2 3 4 5 6 7 8 9 10 11 12
SIGNAL TO NOISE (dB)


SSI 73K321L
BER vs RECEIVE LEVEL
BIT ERROR RATE
10^{-2}
10^{-3}
10^{-4}
10^{-5}
10^{-6}
V.23 MAIN CHANNEL
RECEIVE OPERATION
C2 LINE, S/N = 9.5 dB
10 0 -10 -20 -30 -40 -50
SIGNAL TO NOISE (dB)

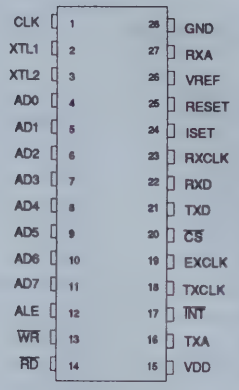

SSI 73K321L
(BELL 202 ONLY) BER vs S/N
BIT ERROR RATE
10^{-2}
10^{-3}
10^{-4}
10^{-5}
10^{-6}
V.23 OPERATION
-40 dBM
C2 EQ. OFF
3002 EQ. OFF
3002 EQ. ON
FLAT EQ. OFF
BACK CHANNEL
FLAT EQ. ON
C2 EQ. ON
-2 0 2 4 6 8 10 12 14 16 18 20 22
SIGNAL TO NOISE (dB)

PACKAGE PIN DESIGNATIONS

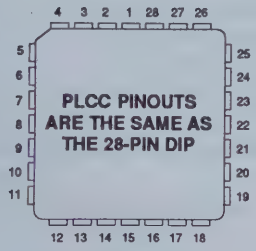
(TOP VIEW)



400-Mil
22-Pin DIP



600-Mil
28-Pin DIP



28-Lead
PLCC

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 73K321L with Parallel Bus Interface		
28-Pin 5 Volt Supply		
Plastic Dual-In-Line	SSI 73K321L - IP	73K321L - IP
Plastic Leaded Chip Carrier	SSI 73K321L - IH	73K321L - IH
SSI 73K321L with Serial Interface		
22-Pin 5 Volt Supply		
Plastic Dual-In-Line	SSI 73K321SL - IP	73K321SL - IP

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NOTES:

SSI 73K322L
CCITT V.23, V.22, V.21 Single-Chip Modem

July, 1989

1

DESCRIPTION

The SSI 73K322L is a highly integrated single-chip modem IC which provides the functions needed to construct a CCITT V.23, V.22 and V.21 compatible modem, capable of 1200 or 0-300 bit/s full-duplex operation or 0-1200 bit/s half-duplex operation with or without the back channel over dial-up lines. The SSI 73K322L is an enhancement of the SSI 73K221L single-chip modem with performance characteristics suitable for European and Asian telephone systems. The SSI 73K322L produces either 550 or 1800 Hz guard tone, recognizes and generates a 2100 Hz answer tone, and allows V.21 fallback for 300 Hz FSK operation. It also operates in V.23, 1200 bit/s FSK mode. The SSI 73K322L integrates analog, digital, and switched-capacitor array functions on a single substrate,offering excellent performance and a high level of functional integration in a single 28- or 22-pin DIP configuration. The SSI 73K322L operates from a single +5 volt supply with very low power consumption.

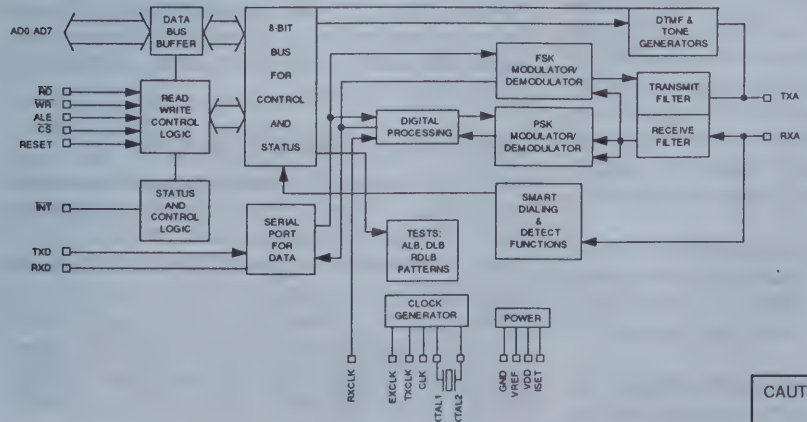
The SSI 73K322L includes the DPSK and FSK modulator/demodulator functions, call progress and handshake tone monitor test modes, and a tone generator capable of producing DTMF, answer, calling and 550 or 1800 Hz guard tone. This device supports V.23, V.22 (except mode v) and V. 21 modes of operation, allowing both synchronous and

(Continued)

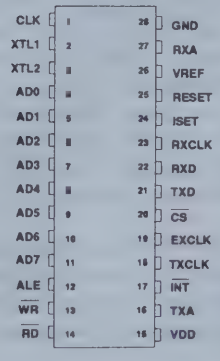
FEATURES

- One-chip CCITT V.23, V.22 and V.21 standard compatible modem
- Full-duplex operation at 0-300 bit/s (FSK) or 600 and 1200 bit/s (DPSK) or 0-1200 bit/s (FSK) forward channel with or without 0-75 bit/s back channel
- Pin and software compatible with other SSI K–Series 1-chip modems
- Interfaces directly with standard microprocessors (8048, 80C51 typical)
- Serial (22-pin DIP) or parallel microprocessor bus (28-pin DIP) for control
- Serial port for data transfer
- Both synchronous and asynchronous modes of operation
- Call progress, carrier, precise answer tone (2100 Hz), calling tone (1300 Hz) and FSK mark detectors
- DTMF and 550 or 1800 Hz guard tone generators
- Test modes available: ALB, DL, RDL, Mark, Space, Alternating bit patterns
- Precise automatic gain control allows 45 dB dynamic range
- Space efficient 22- or 28-pin DIP packages
- CMOS technology for low power consumption using 30 mW @ 5V from a single power supply

BLOCK DIAGRAM



PIN DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

DESCRIPTION (Continued)

asynchronous communications. The SSI 73K322L is designed to appear to the systems designer as a microprocessor peripheral, and will easily interface with popular one-chip microprocessors (80C51 typical) for control of modem functions through its 8-bit multiplexed address/data bus or via an optional serial command bus. An ALE control line simplifies address demultiplexing. Data communications occurs through a separate serial port only.

OPERATION

The SSI 73K322L is ideal for use in either free standing or integral system modem products where multistandard data communications over the 2-wire switched telephone network is desired. Its high functionality, low power consumption and efficient packaging simplify design requirements and increase system reliability. A complete modem requires only the addition of the phone line interface, a control microprocessor, and RS-232 level converter for a typical system. The SSI 73K322L is part of Silicon Systems K-Series family of pin and function compatible single-chip modem products. These devices allow systems to be configured for higher speeds and Bell or CCITT operation with only a single component change.

ASYNCHRONOUS MODE

Data transmission for the DPSK mode requires that data ultimately be transmitted in a synchronous fashion, The SSI 73K322L includes ASYNC/SYNC and SYNC/ASYNC converters which delete or insert stop bits in order to transmit data at a regular rate. In asynchronous mode the serial data comes from the TXD pin into the ASYNC/SYNC rate converter. The ASYNC/SYNC rate converter accepts the data provided on the TXD pin which normally must be 1200 or 600 bit/s +1.0%, -2.5%. The rate converter will then insert or delete stop bits in order to output a signal which is 1200 or 600 bit/s ± .01% (± .01% is the crystal tolerance).

The SYNC/ASYNC converter also has an overspeed mode which allows selection of an output overspeed range of either +1% or +2.3%. In the overspeed mode, some stop bits are output at 7/8 the normal width.

The serial data stream from the transmit buffer or the rate converter is passed through the data scrambler and onto the analog modulator. The data scrambler can be bypassed under processor control when unscrambled data must be transmitted. The ASYNC/SYNC rate converter and the data scrambler are bypassed in all FSK modes. If serial input data contains a break signal through one character (including start and stop bits) the break will be extended to at least 2 • N + 3 bits long (where N is the number of transmitted bits/character).

Serial data from the demodulator is passed normally first through the data descrambler and then through the SYNC/ASYNC rate converter. The ASYNC/ASYNC convertor will reinsert any deleted stop bits and transmit output data at an intra-character rate (bit-to-bit timing) of no greater than 1219 bit/s. An incoming break signal (low through two characters) will be passed through without incorrectly inserting a stop bit.

Similar to the transmit side, both the SYNC/ASYNC rate converter and the data descrambler are bypassed in the FSK modes.

SYNCHRONOUS MODE

The CCITT V.22 standard defines synchronous operation at 600 and 1200 bit/s. Operation is similar to that of the asynchronous mode except that data must be synchronized to a provided clock and no variation in data transfer rate is allowable. Serial input data appearing at TXD must be valid on the rising edge of TXCLK.

TXCLK is an internally derived signal in internal mode and is connected internally to the RXCLK pin in slave mode. Receive data at the RXD pin is clocked out on the falling edge of RXCLK. The ASYNCH/SYNCH converter is bypassed when synchronous mode is selected and data is transmitted out at essentially the same rate as it is input.

DPSK MODULATOR/DEMODULATOR

In DPSK mode the SSI 73K322L modulates a serial bit stream into di-bit pairs that are represented by four possible phase shifts as prescribed by the V.22 standards. The base-band signal is then filtered to reduce intersymbol interference on the bandlimited 2-wire telephone line. Transmission occurs on either a 1200 Hz (originate mode) or 2400 Hz carrier (answer mode). Demodulation is the reverse of the modulation process, with the incoming analog signal eventually

decoded into di-bits and converted back to a serial bit stream. The demodulator also recovers the clock which was encoded into the analog signal during modulation. Demodulation occurs using either a 1200 Hz carrier (answer mode or ALB originate mode) or a 2400 Hz carrier (originate mode or ALB answer mode). The SSI 73K322L uses a phase locked loop coherent demodulation technique that offers inherently better performance than typical DPSK demodulators used by other manufacturers.

FSK MODULATOR/DEMODULATOR

The FSK modulator produces a frequency modulated analog output signal using two discrete frequencies to represent the binary data. V.21 mode uses 980 and 1180 Hz (originate, mark and space) or 1650 and 1850 Hz (answer, mark and space). V.23 mode uses 1300 and 2100 Hz for the main channel and 390 and 450 Hz for the back channel. The modulation rate of the back channel is up to 75 baud. Demodulation involves detecting the received frequencies and decoding them into the appropriate binary value. The rate converter and scrambler/descrambler are automatically bypassed in the V.21 or V.23 modes.

PASSBAND FILTERS AND EQUALIZERS

A high and low band filter is included to shape the amplitude and phase response of the transmit and receive signals and provide compromise delay equalization and rejection of out-of-band signals in the receive channel. Amplitude and phase equalization are necessary to compensate for distortion of the transmission line and to reduce intersymbol interference in the bandlimited receive signal. The transmit signal filtering approximates a 75% square root of raised Cosine frequency response characteristic.

AGC

The automatic gain control maintains a signal level at the input to the demodulators which is constant to within 1 dB. It corrects quickly for increases in signal which would cause clipping and provides a total dynamic range of >45 dB.

PARALLEL BUS INTERFACE

Four 8-bit registers are provided for control, option select and status monitoring. These registers are addressed with the AD0, AD1, and AD2 multiplexed address lines (latched by ALE) and appear to a control microprocessor as four consecutive memory locations. Two control registers and the tone register are read/write memory. The status detect register is read only and cannot be modified except by modem response to monitored parameters.

SERIAL COMMAND INTERFACE

The serial command mode allows access to the SSI 73K322L control and status registers via a serial command port (22-pin version only). In this mode the A0, A1 and A2 lines provide register addresses for data passed through the data pin under control of the $\overline{RD}$ and $\overline{WR}$ lines. A read operation is initiated when the $\overline{RD}$ line is taken low. The next eight cycles of EXCLK will then transfer out eight bits of the selected address location LSB first. A write takes place by shifting in eight bits of data LSB first for eight consecutive cycles of EXCLK. $\overline{WR}$ is then pulsed low and data transferred into the selected register occurs on the rising edge of $\overline{WR}$.

SPECIAL DETECT CIRCUITRY

The special detect circuitry monitors the received analog signal to determine status or presence of carrier, answer tone and weak received signal (long loop condition), special tones such as FSK marking and the 1300 Hz calling tone are also detected. A highly frequency selective call progress detector provides adequate discrimination to accurately detect European call progress signals.

DTMF GENERATOR

The DTMF generator will output one of 16 standard dual-tones determined by a 4-bit binary value and TX DTMF mode bit previously loaded into the tone register. The transmission of DTMF tones is initiated when the DTMF mode is selected and the transmit enable (CR0 bit D1) is changed from 0 to 1.

PIN DESCRIPTION

POWER

NAME	28-PIN	22-PIN	TYPE	DESCRIPTION
GND	28	1	I	System Ground.
VDD	15	11	I	Power supply input, 5V ±10%. Bypass with .1 and 22 µF capacitors to ground.
Vref	26	21	O	An internally generated reference voltage. Bypass with .1 µF capacitor to ground.
Iset	24	19	I	Chip current reference. Sets bias current for op-amps. The chip current is set by connecting this pin to VDD through a 2 MΩ resistor. Iset should be bypassed to GND with a .1 µF capacitor.

PARALLEL MICROPROCESSOR INTERFACE

ALE	12	-	I	Address latch enable. The falling edge of ALE latches the address on AD0-AD2 and the chip select on $\overline{CS}$.
AD0-AD7	4-11	-	I/O	Address/data bus. These bidirectional tri-state multiplexed lines carry information to and from the internal registers.
$\overline{CS}$	20	-	I	Chip select. A low on this pin allows a read cycle or a write cycle to occur. AD0-AD7 will not be driven and no registers will be written if $\overline{CS}$ (latched) is not active. $\overline{CS}$ is latched on the falling edge of ALE.
CLK	1	2	O	Output clock. This pin is selectable under processor control to be either the crystal frequency (for use as a processor clock) or 16 x the data rate for use as a baud rate clock in DPSK modes only. The pin defaults to the crystal frequency on reset.
$\overline{INT}$	17	13	O	Interrupt. This open drain output signal is used to inform the processor that a detect flag has occurred. The processor must then read the detect register to determine which detect triggered the interrupt. $\overline{INT}$ will stay active until the processor reads the detect register or does a full reset.
$\overline{RD}$	14	-	I	Read. A "low" requests a read of the SSI 73K322L internal registers. Data cannot be output unless both $\overline{RD}$ and the latched $\overline{CS}$ are active or "low."
RESET	25	20	I	Reset. An active signal "high" on this pin will put the chip into an inactive state. All control register bits (CR0, CR1, Tone) will be reset. The output of the CLK pin will be set to the crystal frequency. An internal pull down resistor permits power on reset using a capacitor to VDD.

PARALLEL MICROPROCESSOR INTERFACE (Continued)

NAME	28-PIN	22-PIN	TYPE	DESCRIPTION
$\overline{WR}$	13	-	I	Write. A "low" on this informs the SSI 73K322L that data is available on AD0-AD7 for writing into an internal register. Data is latched on the rising edge of $\overline{WR}$. No data is written unless both $\overline{WR}$ and the latched $\overline{CS}$ are active ("low").

SERIAL MICROPROCESSOR INTERFACE

A0-A2	-	5-7	I	Register Address Selection. These lines carry register addresses and should be valid during any read or write operation.
DATA	-	8	I/O	Serial Control Data. Data for a read/write operation is clocked in or out on the falling edge of the EXCLK pin. The direction of data flow is controlled by the $\overline{RD}$ pin. $\overline{RD}$ low outputs data. $\overline{RD}$ high inputs data.
$\overline{RD}$	-	10	I	Read. A "low" on this input informs the SSI 73K322L that data or status information is being read by the processor. The falling edge of the $\overline{RD}$ signal will initiate a read from the addressed register. The $\overline{RD}$ signal must continue for eight falling edges of EXCLK in order to read all eight bits of the referenced register. Read data is provided LSB first. Data will not be output unless the $\overline{RD}$ signal is active.
$\overline{WR}$	-	9	I	Write. A "low" on this input informs the SSI 73K322L that data or status information has been shifted in through the DATA pin and is available for writing to an internal register. The normal procedure for a write is to shift in data LSB first on the DATA pin for eight consecutive falling edges of EXCLK and then to pulse $\overline{WR}$ low. Data is written on the rising edge of $\overline{WR}$.
Note:	In the serial, 22-pin version, the pins AD0-AD7, ALE and $\overline{CS}$ are removed and replaced with the pins; A0, A1, A2, DATA, and an unconnected pin. Also, the $\overline{RD}$ and $\overline{WR}$ controls are used differently. The serial control mode is provided in the 28-pin version by tying ALE high and $\overline{CS}$ low. In this configuration AD7 becomes DATA and AD0, AD1 and AD2 become A0, A1 and A2, respectively.			

RS-232 INTERFACE

NAME	28-PIN	22-PIN	TYPE	DESCRIPTION
EXCLK	19	15	I	External Clock. This signal is used in synchronous DPSK transmission when the external timing option has been selected. In the external timing mode the rising edge of EXCLK is used to strobe synchronous DPSK transmit data available on the TXD pin. Also used for serial control interface.

RS-232 INTERFACE (Continued)

NAME	28-PIN	22-PIN	TYPE	DESCRIPTION
RXCLK	23	18	O	Receive Clock. The falling edge of this clock output is coincident with the transitions in the serial received DPSK data output. The rising edge of RXCLK can be used to latch the valid output data. RXCLK will be valid as long as a carrier is present. In V.23 or V.21 mode a clock which is 16 x1200 or 16 x 300 Hz baud data rate is output, respectively.
RXD	22	17	O	Received Digital Data Output. Serial receive data is available on this pin. The data is always valid on the rising edge of RXCLK when in synchronous mode. RXD will output constant marks if no carrier is detected.
TXCLK	18	14	O	Transmit Clock. This signal is used in synchronous DPSK transmission to latch serial input data on the TXD pin. Data must be provided so that valid data is available on the rising edge of the TXCLK. The transmit clock is derived from different sources depending upon the synchronization mode selection. In Internal Mode the clock is 1200 Hz generated internally. In External Mode TXCLK is phase locked to the EXCLK pin. In Slave Mode TXCLK is phase locked to the RXCLK pin. TXCLK is always active. In V.23 or V.21 mode the output is a 16 x 1200 or 16 x 300 Hz baud clock, respectively.
TXD	21	16	I	Transmit Digital Data Input. Serial data for transmission is input on this pin. In synchronous modes, the data must be valid on the rising edge of the TXCLK clock. In asynchronous modes (1200 or 300 baud) no clocking is necessary. DPSK must be 1200/600 bit/s +1%, -2.5% or +2.3%, -2.5% in overspeed mode.

ANALOG INTERFACE

RXA	27	22	I	Received modulated analog signal input from the phone line.
TXA	16	12	O	Transmit analog output to the phone line.
XTAL1 XTAL2	2 3	3 4	I I	These pins are for the internal crystal oscillator requiring a 11.0592 MHz parallel mode crystal and two load capacitors to Ground. XTAL2 can also be driven from an external clock.

REGISTER DESCRIPTIONS

Four 8-bit internal registers are accessible for control and status monitoring. The registers are accessed in read or write operations by addressing the A0 and A1 address lines in serial mode, or the AD0 and AD1 lines in parallel mode. The AD0 and AD1 lines are latched by ALE. Register CR0 controls the method by which data is transferred over the phone line. CR1 controls the interface between the microprocessor and the SSI 73K322L internal state. DR is a detect register which provides an indication of monitored modem status conditions. TR, the tone control register, controls the DTMF generator, answer and guard tones and RX output gate used in the modem initial connect sequence. All registers are read/write except for DR which is read only. Register control and status bits are identified below:

REGISTER BIT SUMMARY

	ADDRESS	DATA BIT NUMBER							
REGISTER	AD2 - AD0	D7	D6	D5	D4	D3	D2	D1	D0
CONTROL REGISTER 0 CR0	000	MODULATION OPTION		TRANSMIT MODE 3	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ANSWER/ ORIGINATE
CONTROL REGISTER 1 CR1	001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTERRUPT	BYPASS SCRAMBLER/ ADD PH. EQ. (V.23)	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0
DETECT REGISTER DR	010			RECEIVE DATA	UNSCR. MARKS	CARRIER DETECT	SPECIAL TONE	CALL PROGRESS	LONG LOOP
TONE CONTROL REGISTER TR	011	RXD OUTPUT CONTROL	TRANSMIT GUARD/ CALLING TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF3	DTMF2/ V.23 FDX	DTMF1/ OVERSPEED	DTMF0/GUARD/ ANSWER/SPEC. TONE SELECT
CONTROL REGISTER 2 CR2	100				THESE REGISTER LOCATIONS ARE RESERVED FOR				
CONTROL REGISTER 3 CR3	101				USE WITH OTHER K-SERIES FAMILY MEMBERS				
ID REGISTER ID	110	0	0						

NOTE: When a register containing reserved control bits is written into, the reserved bits must be programmed as 0's.

REGISTER ADDRESS TABLE

REGISTER	ADDRESS AD2 - AD0	DATA BIT NUMBER D7	D6	D5	D4	D3	D2	D1	D0
CONTROL REGISTER 0 CR0	000	MODULATION OPTION		TRANSMIT MODE 3	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ORIGINATE/ ANSWER
CONTROL REGISTER 1 CR1	001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTERRUPT	BYPASS SCRAMBLER/ ADD PH. EQ.	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0
DETECT REGISTER DR	010			RECEIVE DATA		CARRIER DETECT	SPECIAL TONE	CALL PROGRESS	LONG LOOP
TONE CONTROL REGISTER TR	011	RXD OUTPUT CONTROL	TRANSMIT GUARD/ CALLING TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF3	DTMF2	DTMF1/ OVERSPEED	DTMF0/GUARD/ ANSWER/ SPECIAL TONE
ID REGISTER ID	110	ID 1	ID 0						

0=1200 BIT/S DPSK
1=600 BIT/S DPSK
0=V.23 FSK
1=V.21 FSK

0000=PWR DOWN
0001=INT SYNCH
0010=EXT SYNCH
0011=SLAVE SYNCH
0100=ASYNCH 8 BITS/CHAR
0101=ASYNCH 9 BITS/CHAR
0110=ASYNCH 10 BITS/CHAR
0111=ASYNCH 11 BITS/CHAR
1100=FSK

0=SQUELCH ANALOG
1=ENABLE ANALOG

0=ANSWER
1=ORIGINATE
IN V.23 MODE :
0=RECEIVE @ 1200 BIT/S, TRANSMIT @ 75 BIT/S
1=RECEIVE @ 75 BIT/S, TRANSMIT @ 1200 BIT/S

00=TX DATA
01=TX ALTERNATE
10=TX MARK
11=TX SPACE

0=OFF
1=ON

0=NORMAL
1=BYPASS SCRAMBLER
1=ADD EXTRA PHASE EQ. IN V.23

0=XTAL
1=16 X DATA RATE OUTPUT AT CLK PIN IN DPSK MODE ONLY

0=NORMAL
1=RESET

00=NORMAL
01=ANALOG LOOPBACK
10=REMOTE DIGITAL LOOPBACK
11=LOCAL DIGITAL LOOPBACK

OUTPUTS RECEIVED DATA STREAM

0=CONDITION NOT DETECTED
1=CONDITION DETECTED

RXD PIN
0=NORMAL
1=TRI STATE

0=OFF
1=ON

0=OFF
1=ON

0=DATA
1=TX DTMF

4 BIT CODE FOR 1 OF 16 DUAL TONE COMBINATIONS. OVERIDES OTHER TRANSMIT MODES

0=NORMAL
1=ALLOWS V.23 FULL DUPLEX OPERATION

0=1800 Hz G.T. (V.22). 2225 Hz ANS TONE GENERATED, FSK MARK DETECT SELECTED
1=550 Hz G.T. (V.22) 2100 Hz ANS TONE GENERATED & DETECTED (V.21, V.22) 1300 Hz DETECTED (V.23)

00=73K212 US 212/103 OR 73K322 V.23/V.22/V.21
01=73K221 EUROPEAN V.22/V.21 or 73K302L
10=73K222 BELL 212/103 AND V.22/V.21
11=73K224 BELL 212/103 AND V.22 bis/V.22/V.21

CONTROL REGISTER 0

	D7	D6	D5	D4	D3	D2	D1	D0
CR0 000	MODUL. OPTION		TRANSMIT MODE 3	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ANSWER/ ORIGINATE

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	Answer/ Originate	0	Selects answer mode (transmit in high band, receive in low band or in V.23 HDX mode, receive at 1200 bit/s and transmit at 75 bit/s).
		1	Selects originate mode (transmit in low band,receive in high band or in V.23 HDX mode, receive at 75 bit/s and transmit at 1200 bit/s).
			Note: This bit works with TR bit D0 to program special tones detected in Tone Register. See detect and tone registers.
D1	Transmit Enable	0	Disables transmit output at TXA.
		1	Enables transmit output at TXA.
			Note: Answer tone and DTMF TX control require TX enable.
D5, D4,D3, D2	Transmit Mode	D5 D4 D3 D2	
		0 0 0 0	Selects power down mode. All functions disabled except digital interface.
		0 0 0 1	Internal synchronous mode. In this mode TXCLK is an internally derived 1200 Hz signal. Serial input data appearing at TXD must be valid on the rising edge of TXCLK. Receive data is clocked out of RXD on the falling edge of RXCLK.
		0 0 1 0	External synchronous mode. Operation is identical to internal synchronous, but TXCLK is connected internally to EXCLK pin, and a 1200 Hz clock must be supplied externally.
		0 0 1 1	Slave synchronous mode. Same operation as other synchronous modes. TXCLK is connected internally to the RXCLK pin in this mode.
		0 1 0 0	Selects PSK asynchronous mode - 8 bits/character (1 start bit, 6 data bits, 1 stop bit).
		0 1 0 1	Selects PSK asynchronous mode - 9 bits/character (1 start bit, 7 data bits, 1 stop bit).
		0 1 1 0	Selects PSK asynchronous mode - 10 bits/character (1 start bit, 8 data bits, 1 stop bit).
		0 1 1 1	Selects PSK asynchronous mode - 11 bits/character (1 start bit, 8 data bits, Parity and/or 1 or 2 stop bits).
		1 1 0 0	Selects FSK operation.

CONTROL REGISTER 0 (Continued)

	D7	D6	D5	D4	D3	D2	D1	D0
CR0 000	MODUL. OPTION		TRANSMIT MODE 3	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ANSWER/ ORIGINATE

BIT NO.	NAME	CONDITION	DESCRIPTION
D6		0	Not used; must be written as a "0."
D7	Modulation Option	D7 D5 D4	Selects:
		0 0 X	PSK asynchronous mode at 1200 bit/s.
		1 0 X	PSK asynchronous mode at 600 bit/s.
		0 1 1	FSK CCITT V.23 mode.
		1 1 1	FSK CCITT V.21 mode.

CONTROL REGISTER 1

	D7	D6	D5	D4	D3	D2	D1	D0
CR1 001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTER.	BYPASS SCRAMB/ ADD PH. EQ.	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0

BIT NO.	NAME	CONDITION	DESCRIPTION
		D1 D0	
D1, D0	Test Mode	0 0	Selects normal operating mode.
		0 1	Analog loopback mode. Loops the transmitted analog signal back to the receiver, and causes the receiver to use the same center frequency as the transmitter. To squelch the TXA pin, transmit enable must be forced low.
		1 0	Selects remote digital loopback. Received data is looped back to transmit data internally, and RXD is forced to a mark. Data on TXD is ignored.
		1 1	Selects local digital loopback. Internally loops TXD back to RXD and continues to transmit data from TXA pin.
D2	Reset	0	Selects normal operation.
		1	Resets modem to power down state. All control register bits (CR0, CR1, Tone) are reset to zero. The output of the clock pin will be set to the crystal frequency.

CONTROL REGISTER 1 (Continued)

	D7	D6	D5	D4	D3	D2	D1	D0
CR1 001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTER.	BYPASS SCRAMB/ ADD PH. EQ.	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0

BIT NO.	NAME	CONDITION	DESCRIPTION
D3	CLK Control (Clock Control)	0	Selects 11.0592 MHz crystal echo output at CLK pin.
		1	Selects 16 X the data rate, output at CLK pin in DPSK modes only.
D4	Bypass Scrambler/ Add Ph. Eq.	0	Selects normal operation. DPSK data is passed through scrambler.
		1	Selects Scrambler Bypass. Bypass DPSK data is routed around scrambler in the transmit path. In V.23 mode, additional phase equalization is added to the main channel filters when D4 is set to 1.
D5	Enable Detect Interrupt	0	Disables interrupt at $\overline{INT}$ pin. All interrupts are normally disabled in power down modes.
		1	Enables $\overline{INT}$ output. An interrupts will be generated with a change in status of DR bits D1-D4. The special tone and call progress detect interrupts are masked when the TX enable bit is set. Carrier detect is masked when TX DTMF is activated. All interrupts will be disabled if the device is in power down mode.
D7, D6	Transmit Pattern	D7 D6	
		0 0	Selects normal data transmission as controlled by the state of the TXD pin.
		0 1	Selects an alternating mark/space transmit pattern for modem testing.
		1 0	Selects a constant mark transmit pattern.
		1 1	Selects a constant space transmit pattern.

DETECT REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
DR 010			RECEIVE DATA	UNSCR. MARK	CARR. DETECT	SPECIAL TONE	CALL PROG.	LONG LOOP

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	Long Loop	0	Indicates normal received signal.
		1	Indicates low received signal level.
D1	Call Progress Detect	0	No call progress tone detected.
		1	Indicates presence of call progress tones. The call progress detection circuitry is activated by energy in the normal 350 to 620 Hz call progress bandwidth.
D2	Special Tone Detect	0	No special tone detected as programmed by CR0 bit D0 and Tone Register bit D0.
		1	Special tone detected. The detected tone is:
			(1) 2100 Hz answer tone if D0 of TR=1 and the device is in V.21 or V.22 originate mode.
			(2) 1300 Hz calling tone if D0 of TR=1 and the device is in V.21, or V.22 answer mode.
			(3) an FSK mark in the mode the device is set to receive.
			Tolerance on special tones is ±3%.
D3	Carrier Detect	0	No carrier detected in the receive channel.
		1	Indicated carrier has been detected in the received channel.
D4	Unscr. Mark (Unscrambled Mark)	0	No unscrambled mark.
		1	Indicates detection of unscrambled marks in the received data. A valid indication requires that unscrambled marks be received for > 165.5 ± 6.5 ms.
D5	Receive Data		Continuously outputs the received data stream. This data is the same as that output on the RXD pin, but it is not disabled when RXD is tri-stated.
D6, D7			Not used.

TONE REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
TR 011	RXD OUTPUT CONTR.	TRANSMIT GUARD/ CALLING TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF 3	DTMF 2	DTMF 1/ OVER-SPEED	DTMF 0/ G.T./ANSW./ SP. TONE/ SELECT

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	DTMF 0	D6 D5 D4 D0	D0 interacts with bits D6, D4, and CR0 as shown.
		X X 1 X	Transmit DTMF tones.
	Guard Tone/ Answer Tone	1 X 0 0	Select 1800 Hz guard tone if in V.22 and answer mode in CR0.
	Special Tone/ Detect/Select	1 X 0 1	Select 550 Hz guard tone if in V.22 and answer mode in CR0.
		X X 0 0	Mark of an FSK mode selected in CR0 is to be detected in D2 of DR.
		X X 0 1	2100 Hz answer tone will be detected in D2 of DR if V.21 or V.22 originate mode is selected in CR0.
			1300 Hz calling tone will be detected in D2 of DR if V.21, or V.22 answer mode is selected in CR0.
		X 0 0 0	Transmit 2225 Hz Answer Tone
		X 1 0 0	Transmit 2100 Hz Answer Tone
D1	DTMF 1/ Overspeed	D4 D1	D1 interacts with D4 as shown.
		0 0	Asynchronous PSK 1200 or 600 bit/s +1.0% -2.5%.
		0 1	Asynchronous PSK 1200 or 600 bit/s +2.3% -2.5%.
D3, D2, D1, D0	DTMF 3, 2, 1, 0	D3 D2 D1 D0	
		0 0 0 0 - 1 1 1 1	Programs 1 of 16 DTMF tone pairs that will be transmitted when TX DTMF and TX enable bit (CR0, bit D1) is set. Tone encoding is shown below:

KEYBOARD EQUIVALENT	DTMF CODE D3 D2 D1 D0	TONES LOW HIGH
1	0 0 0 1	697 1209
2	0 0 1 0	697 1336
3	0 0 1 1	697 1477
4	0 1 0 0	770 1209
5	0 1 0 1	770 1336
6	0 1 1 0	770 1477
7	0 1 1 1	852 1209

TONE REGISTER (Continued)

	D7	D6	D5	D4	D3	D2	D1	D0
TR 011	RXD OUTPUT CONTR.	TRANSMIT GUARD/ CALLING TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF 3	DTMF 2	DTMF 1/ OVER-SPEED	DTMF 0/ GUARD/ SPECIAL TONE SEL

BIT NO.	NAME	CONDITION	DESCRIPTION
D3, D2, D1, D0 (Cont.)			KEYBOARD EQUIVALENT / DTMF CODE D3 D2 D1 D0 / TONES LOW HIGH
			8 — 1 0 0 0 — 852 1336
			9 — 1 0 0 1 — 852 1477
			0 — 1 0 1 0 — 941 1336
			* — 1 0 1 1 — 941 1209
			# — 1 1 0 0 — 941 1477
			A — 1 1 0 1 — 697 1633
			B — 1 1 1 0 — 770 1633
			C — 1 1 1 1 — 852 1633
			D — 0 0 0 0 — 941 1633
D4	TX DTMF (Transmit DTMF)	0	Disabled DTMF.
		1	Activates DTMF. The selected DTMF tones are transmitted continuously when this bit is high. TX DTMF overrides all other transmit functions.
D5	TX ANS (Transmit Answer tone)	0	Disables answer tone generator.
		1	Enables answer tone generator. A 2100 Hz answer tone will be transmitted continuously when the transmit enable bit is set. The device must be in answer mode. To transmit answer tone, the device must be in DPSK answer mode.
D6	TX Guard or Calling Tone (Transmit Guard or Calling Tone)	0	Disables guard/calling tone generator.
		1	Transmit guard tone if in V.22 and answering; otherwise transmit calling tone, in any other mode including V.23 mode.
D7	RXD Output Control	0	Enables RXD pin. Receive data will be output on RXD.
		1	Disables RXD pin. The RXD pin reverts to a high impedance with internal weak pull-up resistor.

ID REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
ID 110	ID 1	ID 0						

BIT NO.	NAME	CONDITION	DESCRIPTION
D7, D6	Device Identification Signature	D7 D6	Indicates Device:
		0 0	SSI 73K212(L) or 73K322L
		0 1	SSI 73K221(L) or 73K302L
		1 0	SSI 73K222(L)
		1 1	SSI 73K224L

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
VDD Supply Voltage	14	V
Storage Temperature	-65 to 150	°C
Soldering Temperature (10 sec.)	260	°C
Applied Voltage	-0.3 to VDD+0.3	V

Note: All inputs and outputs are protected from static charge using built-in, industry standard protection devices and all outputs are short-circuit protected.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
VDD Supply Voltage		4.5	5	5.5	V
Digital Pins					
VIH, Input High Voltage					
Reset, XTAL1, XTAL2		3.0		VDD	V
All other inputs		2.0		VDD	V
VIL, Input Low Voltage		0		0.8	V
IOH, Output High Current		-0.4			mA
IOL, Output Low Current				1.6	mA
TA, Operating Free-Air Temperature		-40		+85	°C

RECOMMENDED OPERATING CONDITIONS (Continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
External Component (Refer to Application section for placement.)					
VREF Bypass capacitor	(External to GND)	0.1			µF
Bias setting resistor	(Placed between VDD and ISET pins)	1.8	2	2.2	MΩ
ISET Bypass capacitor	(ISET pin to GND)	0.1			µF
VDD Bypass capacitor 1	(External to GND)	0.1			µF
VDD Bypass capacitor 2	(External to GND)	22			µF
Clock Variation	(11.0592 MHz) Crystal or external clock	-0.01		+0.01	%

DC ELECTRICAL CHARACTERISTICS
(TA = -40°C to 85°C, VDD = recommended range unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
IDD, Supply Current	ISET Resistor = 2 MΩ				
IDDA, Active	CLK = 11.0592 MHz		7	10	mA
IDD1, Power-down	CLK = 11.0592 MHz			4	mA
IDD2, Power-down	CLK = 19.200 KHz			3	mA
Digital Inputs					
IIH, Input High Current	VI = VIH Max			100	µA
IIL, Input Low Current	VI = VIL Min	-200			µA
Reset Pull-down Current	Reset = VDD	1		50	µA
Digital Outputs					
VOH, Output High Voltage	IO = IOH MIN	2.4		VDD	V
VOL, Output Low Voltage	IO = IO MAX			0.4	V
VOL, CLK Output	IO = 3.6 mA			0.6	V
RXDTri-State Pull-up Curr.	RXD = GND	-1		-50	µA

DC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNITS
Capacitance					
Inputs	Capacitance, all Digital Input pins			10	pF
XTAL1, 2 Load Capacitors	Depends on crystal characteristics	15		60	pF
CLK	Maximum Capacitive Load			15	pF

DYNAMIC CHARACTERISTICS AND TIMING
(TA = -40°C to +85°C, VDD = Recommended range unless otherwise noted.)

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNITS
PSK Modulator					
Carrier Suppression	Measured at TXA	55			dB
Output Amplitude	TX scrambled marks	-11	-10	-9	dBm0
FSK Modulator					
Output Freq. Error	CLK = 11.0592 MHz	-0.35		+.35	%
Transmit Level	Transmit Dotting Pattern	-11	-10	-9	dBm0
Harmonic Distortion in 700-2900 Hz band	THD in the alternate band DPSK or FSK		-60	-50	dB
Output Bias Distortion	Transmit Dotting Pattern In ALB @ RXD		±8		%
Total Output Jitter	Random Input in ALB @ RXD	-10		+10	%
DTMF Generator					
Freq. Accuracy		-.25		+.25	%
Output Amplitude	Low Band	-10	-9	-8	dBm0
Output Amplitude	High Band	-8	-7	-6	dBm0
Twist	High-Band to Low-Band	1.0	2.0	3.0	dB
Long Loop Detect	DPSK only	-38		-28	dBm0
Dynamic Range	Refer to Performance Curves		45		dB

DYNAMIC CHARACTERISTICS AND TIMING (Continued)

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNITS
Call Progress Detector					
Detect Level	-3 dB points in 285 and 675 Hz	-38			dBm0
Reject Level	Test signal is a 460 Hz sinusoid			-45	dBm0
Delay Time	-70 dBm0 to -30 dBm0 STEP	20		40	ms
Hold Time	-30 dBm0 to -70 dBm0 STEP	20		40	ms
Hysteresis		2			dB
Carrier Detect					
Threshold	DPSK or FSK receive data	-49		-42	dBm0
Delay Time					
V.21		13		20	ms
V.22		15		32	ms
V.23 Forward Channel		7		12	ms
V.23 Back Channel		25		40	ms
Hold Time					
V.21		12		30	ms
V.22		10		24	ms
V.23 Forward Channel		7		15	ms
V.23 Back Channel		22		40	ms
Hysteresis		2			dB
Special Tone Detectors					
Detect Level	See definitions for TR bit D0 mode	-49		-42	dBm0
Delay Time					
2100 Hz answer tone		15		35	ms
1300Hz calling tone		13		20	ms
390 Hz V.23 back channel mark		25		60	ms

Note: Parameters expressed in dBm0 refer to the following definition:

0 dB loss in the Transmit path to the line.
2 dB gain in the Receive path from the line.

Refer to the Basic Box Modem diagram in the Applications section for the DAA design.

DYNAMIC CHARACTERISTICS AND TIMING (Continued)

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNITS
Special Tone Detectors (Continued)					
980 or 1650 Hz V.21 marks		15		30	ms
Hold Time					
2100 Hz answer tone		4		24	ms
1300 Hz calling tone		4		24	ms
390 Hz V.23 back channel mark		20		30	ms
980 or 1650 Hz V.21 marks		7		20	ms
Hysteresis		2			dB
Detect Freq. Range	Any Special Tone	-3		+3	%
Output Smoothing Filter					
Output load	TXA pin; FSK Single Tone out for THD = -50 dB in .3 to 3.4 KHz	10		 50	KΩ pF
Out of Band Energy	Frequency >12KHz in all modes			-70	dBm0
Output Impedance	TXA pin		200	300	Ω
Clock Noise	TXA pin; 76.8 KHz or 122.88 KHz inV.23 main channel			0.4	mVrms
Carrier VCO					
Capture Range	Originate or Answer	-10		+10	Hz
Capture Time	-10 Hz to +10 Hz Carrier Freq. Change Assum.		40	100	ms
Recovered Clock					
Capture Range	% of frequency center frequency (center at 1200 Hz)	-625		+625	ppm
Data Delay Time	Analog data in at RXA pin to receive data valid at RXD pin		30	50	ms

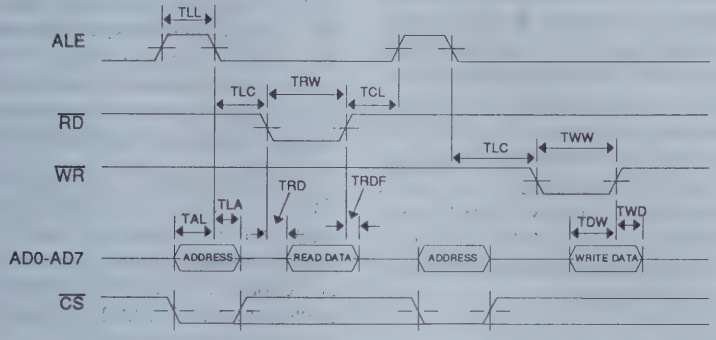
DYNAMIC CHARACTERISTICS AND TIMING (Continued)

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNITS
Guard Tone Generator					
Tone Accuracy	550 or 1800 Hz	-20		+20	Hz
Tone Level	550 Hz	-4.0	-3.0	-2.0	dB
(Below DPSK Output)	1800 Hz	-7.0	-6.0	-5.0	dB
Harmonic Distortion	550 Hz			-50	dB
700 to 2900 Hz	1800 Hz			-60	dB
Timing (Refer to Timing Diagrams)					
TAL	$\overline{CS}$/Addr. setup before ALE	30			ns
TLA	$\overline{CS}$/Addr. Hold after latch	20			ns
TLC	Latch to $\overline{RD}/\overline{WR}$ control	40			ns
TCL	$\overline{RD}/\overline{WR}$ Control to Latch	10			ns
TRD	Data out from $\overline{RD}$	0		160	ns
TLL	ALE width	60			ns
TRDF	Data float after READ	0		80	ns
TRW	READ width	200		25000	ns
TWW	WRITE width	140		25000	ns
TDW	Data setup before WRITE	150			ns
TWD	Data hold after WRITE	20			ns
TCKD	Data out after CLK			200	ns
TCKW	WRITE after CLK	150			ns
TDCK	Data setup before CLK	150			ns
TAC	Address setup before control [1]	50			ns
TCA	Address hold after control [1]	50			ns

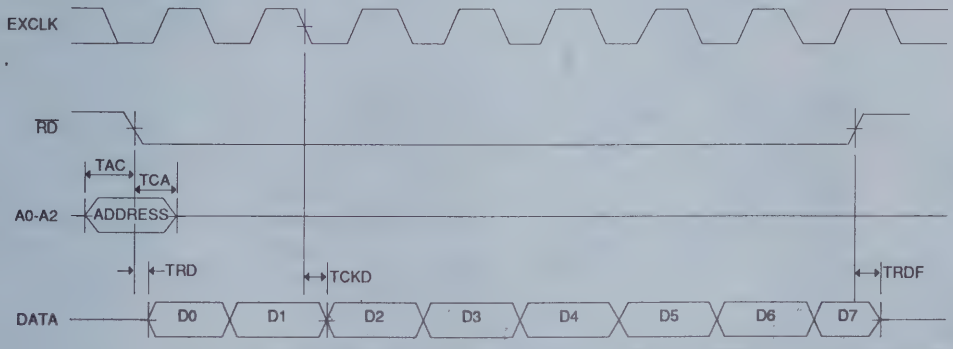
1: Control for setup is the falling edge of $\overline{RD}$ or $\overline{WR}$.
Control for hold is the falling edge of $\overline{RD}$ or the rising edge of $\overline{WR}$.

TIMING DIAGRAMS

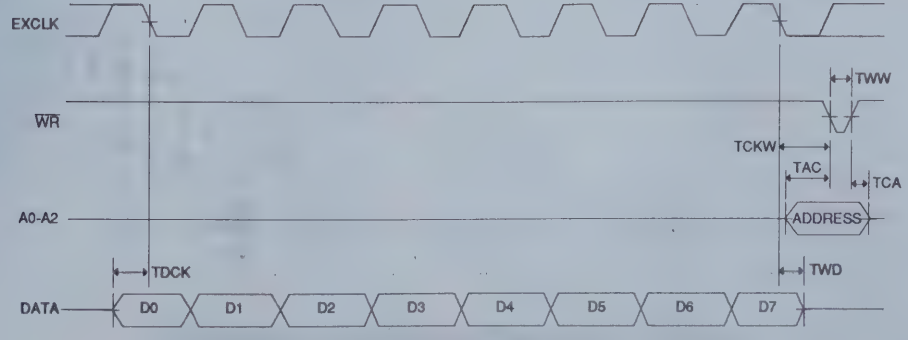
BUS TIMING DIAGRAM (PARALLEL VERSION)



READ TIMING DIAGRAM (SERIAL VERSION)



WRITE TIMING DIAGRAM (SERIAL VERSION)



APPLICATIONS INFORMATION

GENERAL CONSIDERATIONS

Figures 1 and 2 show the basic circuit diagram for K–Series modem integrated circuits. K-Series products are designed to be used in conjunction with a control processor, a UART or RS-232 serial data interface, and a DAA phone line interface to function as a typical intelligent modem. The K-Series ICs interface directly with Intel 8048 and 80C51 microprocessors for control and status monitoring purposes. Two typical DAA arrangements are shown: one for a split ±5 or ±12 volt design and one for a single 5 volt design. These diagrams are for reference only and do not represent production-ready modem designs.

K-Series devices are available in two control interface versions: one for a parallel multiplexed address/data interface, and one for a serial interface. The parallel version is intended for use with 8039/48 or 8031/51 microcontrollers from Intel or many other manufacturers. The serial interface 22-pin version can be used with other microcontrollers or in applications where only a limited number of port lines are available. The parallel versions may also be used in the serial mode, as explained in the data sheet pin description.

In most applications the controller will monitor the serial data for commands from the DTE and the received data for break signals from the far end modem. In this way, command data to the modem is sent over the same data line as the transmitted data. In other applications the RS-232 interface handshake lines are used for modem control.

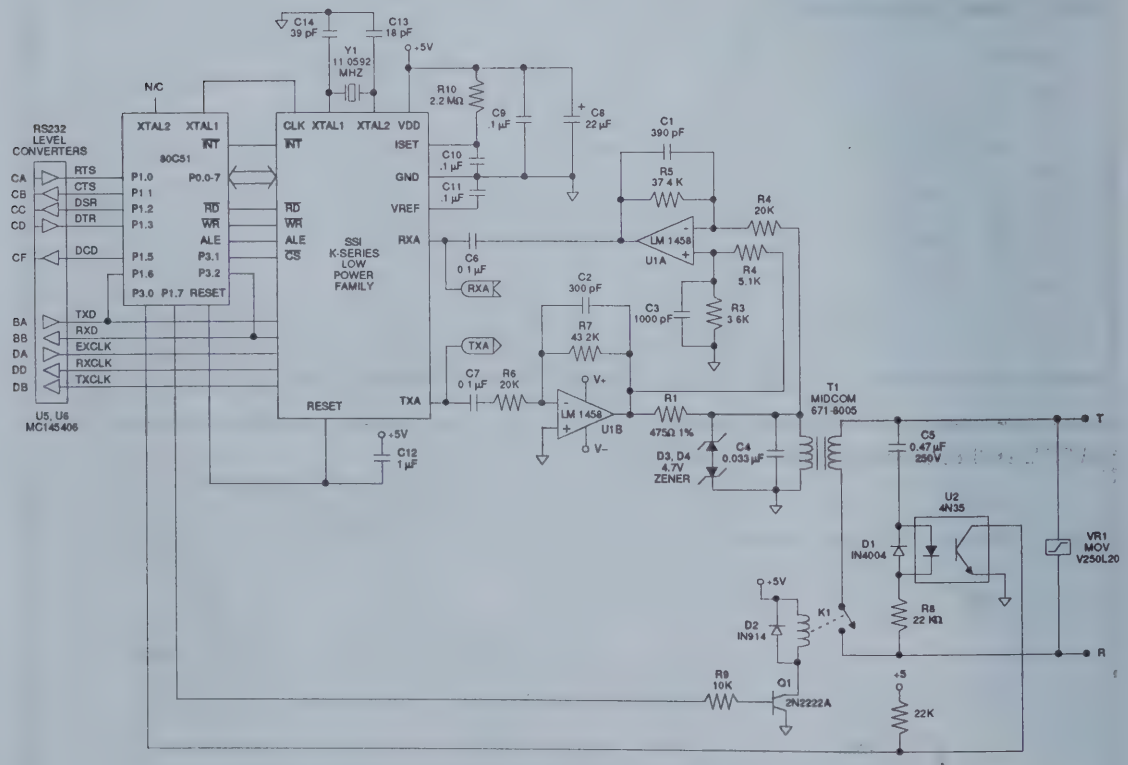


FIGURE 1: Basic Box Modem with Dual-Supply DAA

DIRECT ACCESS ARRANGEMENT (DAA)

The DAAs shown are two examples of how the "hybrid" may be implemented. The split supply design (Figure 1) is a typical two op-amp hybrid. The receive op-amp serves two purposes. It supplies gain to amplify the receive signal to the proper level for the modem's detectors and demodulator, and it removes the transmitted signal from the receive signal present at the transformer. This is done by supplying a portion of the transmitted signal to the non-inverting input of the receive op-amp at the same amplitude as the signal appearing at the transformer, making the transmit signal common mode.

The single-supply DAA is more complex than the dual-supply version described above, but its use eliminates the need for a second power supply. This DAA (Figure 2) uses a bridged drive to allow undistorted signals to be sent with a single 5 volt supply. Because DTMF tones utilize a higher amplitude than data, these signals will clip if a single-ended drive approach is used. The bridged driver uses an extra op-amp (U1A) to invert the signal coming from the gain setting op-amp (U1B) before sending it to the other leg of the transformer. Each op-amp then supplies half the drive signal to the transformer. The receive amplifier (op-amp C) picks off its signal at the junction of the impedance matching resistor and the transformer. Because the bottom leg of the transformer is being driven in one direction by U1A and the resistor is driven in the opposite direction at the same time by U1B, the summing point of the transformer and resistor remains relatively constant and the receive signal is unaffected.

DESIGN CONSIDERATIONS

Silicon Systems 1-chip modem products include all basic modem functions on a single IC, accessible from a standard bus interface. This makes these devices adaptable for use in a variety of applications, and as easy to control as conventional digital bus peripherals.

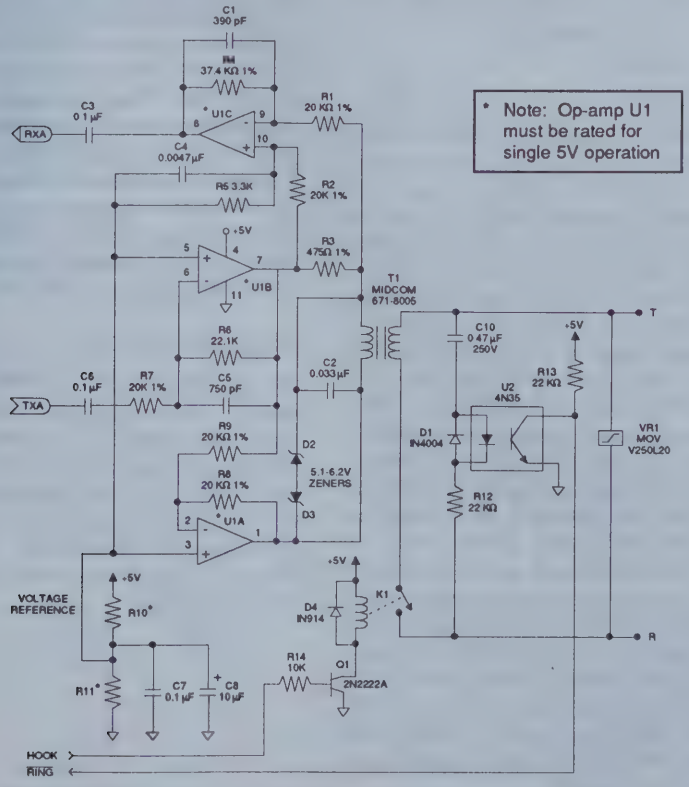


FIGURE 2: Single 5V DAA Version

Unlike digital logic circuitry, however, modem designs must properly contend with precise frequency tolerances, and very low level analog signals, to insure acceptable performance. Using good analog circuit design practices will generally result in a sound design. Folllowing are additional recommendations which should be taken into consideration when starting new designs.

CRYSTAL OSCILLATOR

The K-Series crystal oscillator requires a parallel mode (antiresonant) crystal which operates at 11.0592 MHz. It is important that this precise frequency be maintained to within ±.01% accuracy.

In order for a parallel mode crystal to operate correctly and to specification, it must have a load capacitor connected to the junction of each of the crystal and internal inverter connections, terminated to ground. The values of these capacitors depend primarily on the crystal's characteristics, and to a lesser degree on the internal inverter circuit. The values used affect the accuracy and start up characteristics of the oscillator.

LAYOUT CONSIDERATIONS

Good analog/digital design rules must be used to control system noise in order to obtain highest performance in modem designs. The more digital circuitry present on the PC board, the more this attention to noise control is needed. The modem should be treated as a high impedance analog device. A 22 µF electrolytic capacitor in parallel with a 0.1 µF ceramic capacitor between VDD and ground is recommended. Liberal use of ground planes and larger traces on power and ground are also highly favored. High speed digital circuits tend to generate a significant amount of EMI (Electro-Magnetic Interference) which must be minimized in order to meet regulatory agency limitations. To accomplish this, high speed digital devices should be locally bypassed, and the DAA and K-Series device should be located close to each other near the area of the board where the phone line connection is accessed. To avoid problems, power supply and ground traces should be routed separately to the analog and digital functions on the board, and digital signals should not be routed near low level or high impedance analog traces. The analog and digital grounds should only connect at one point near the analog supplies to avoid ground loops. The K–Series modem IC's should have both high frequency and low frequency bypassing as near to the package as possible.

MODEM PERFORMANCE CHARACTERISTICS

The curves presented here define modem IC performance under a variety of line conditions while inducing disturbances that are typical of those encountered during data transmission on public service telephone lines. Test data was taken using an AEA Electronics' "Autotest I" modem test set and line simulator, operating under computer control. All tests were run full-duplex, using a Concord Data Systems 224 as the reference modem. A 511 pseudo-random-bit pattern was used with $1X10^6$ bits transmitted for each data point. Noise was C-message weighted and all signal-to-noise (S/N) ratios reflect total power measurements similar to the CCITT V.56 measurement specification. The individual tests are defined as follows.

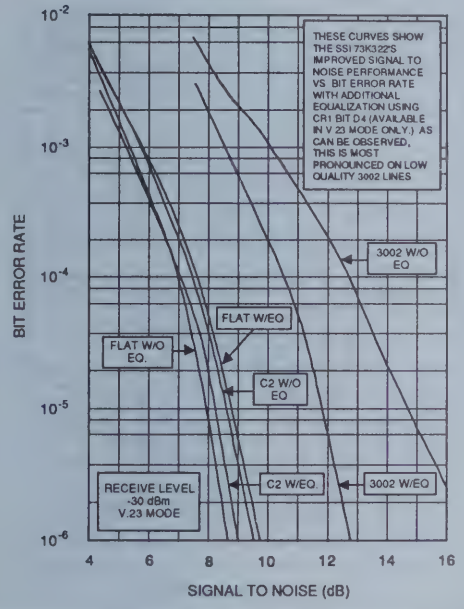
BER vs.S/N

This test measures the ability of the modem to operate over noisy lines with a minimum of data-transfer errors. Since some noise is generated in the best of dial-up lines, the modem must operate with the lowest S/N ratio possible. Optimum modem performance is indicated by test curves that are closest to the zero axis. A narrow spread between curves representing the four line parameters indicates minimal variation in performance while operating over a range of aberrant operating conditions. Typically, a PSK modem will exhibit better BER-performance test curves operating in the highband range than in the lowband.

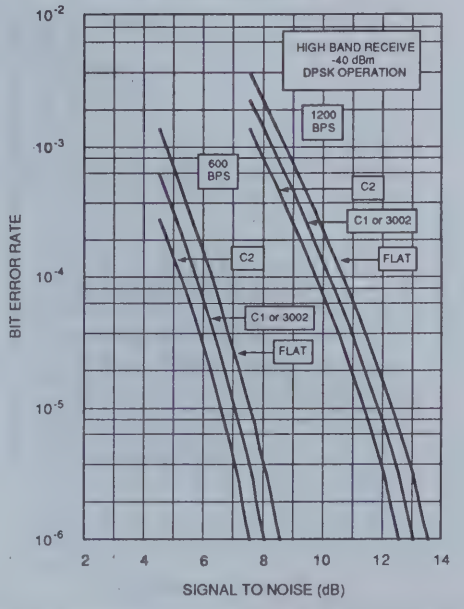
BER vs. Receive Level

This test measures the dynamic range of the modem. Because signal levels vary widely over dial-up lines, the widest possible dynamic range is desirable. The minimum Bell specification calls for 36 dB of dynamic range. S/N ratios are held constant at the indicated values while the receive level is lowered from a very high to very low signal levels. The width of the "bowl" of these curves, taken at the BER point, is the measure of dynamic range.

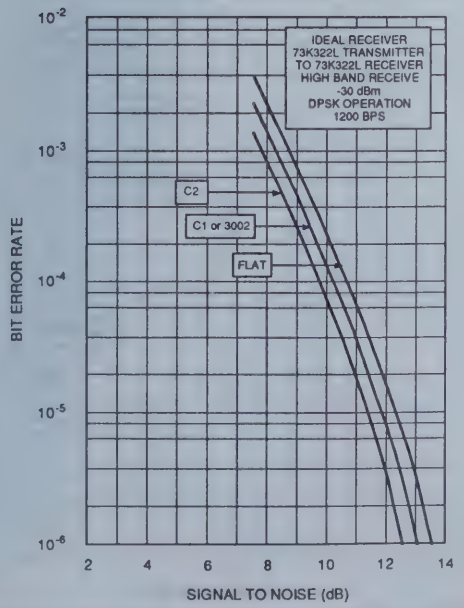
SSI 73K322L (V.23 ONLY) BER vs S/N


THESE CURVES SHOW THE SSI 73K322'S IMPROVED SIGNAL TO NOISE PERFORMANCE VS. BIT ERROR RATE WITH ADDITIONAL EQUALIZATION USING CR1 BIT D4 (AVAILABLE IN V.23 MODE ONLY.) AS CAN BE OBSERVED, THIS IS MOST PRONOUNCED ON LOW QUALITY 3002 LINES
3002 W/O EQ
FLAT W/EQ
FLAT W/O EQ.
C2 W/O EQ
RECEIVE LEVEL -30 dBm V.23 MODE
C2 W/EQ
3002 W/EQ
BIT ERROR RATE
SIGNAL TO NOISE (dB)

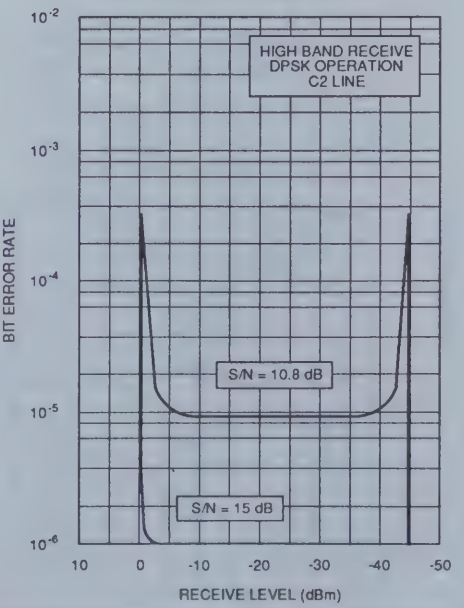
SSI 73K322L BER vs S/N

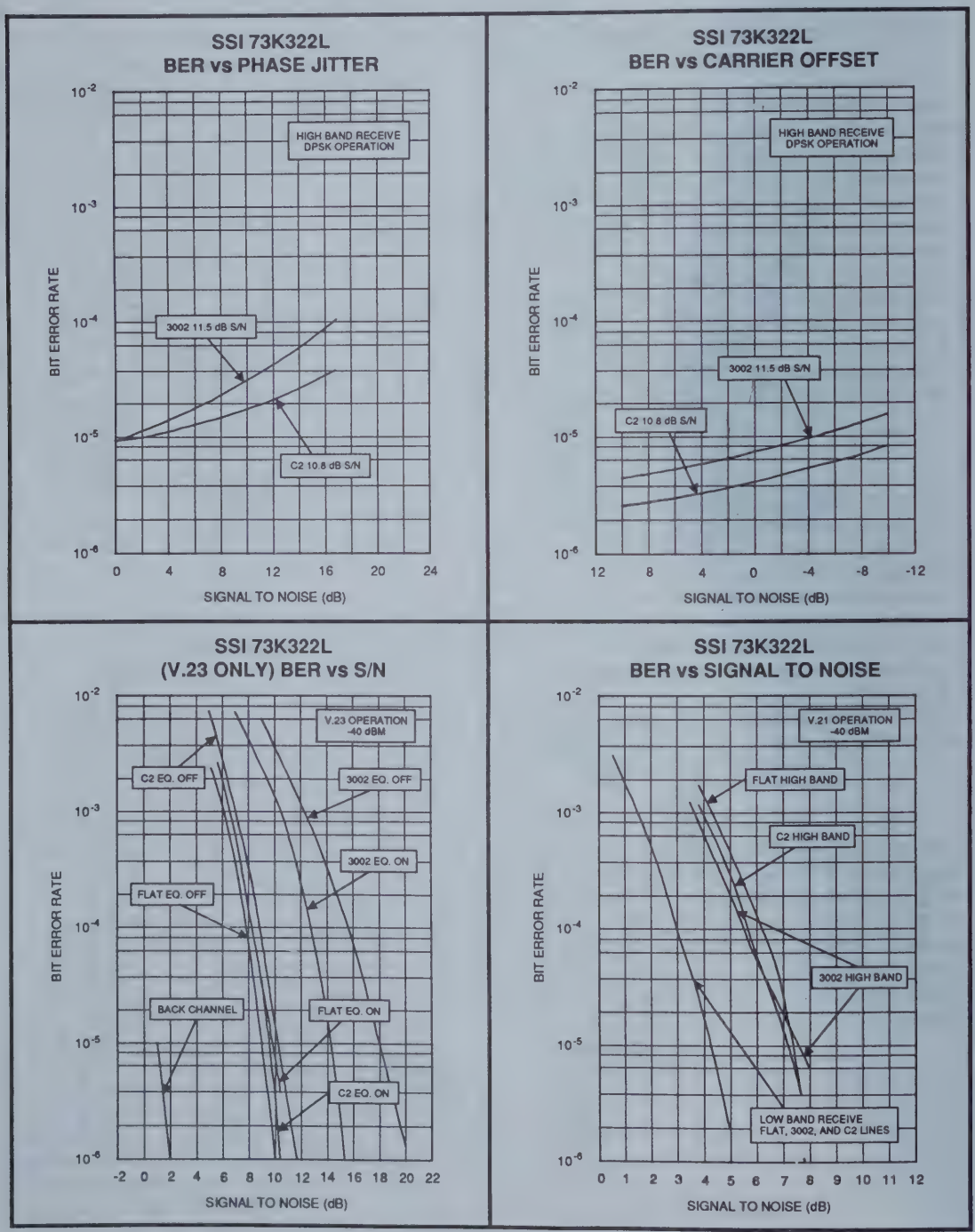


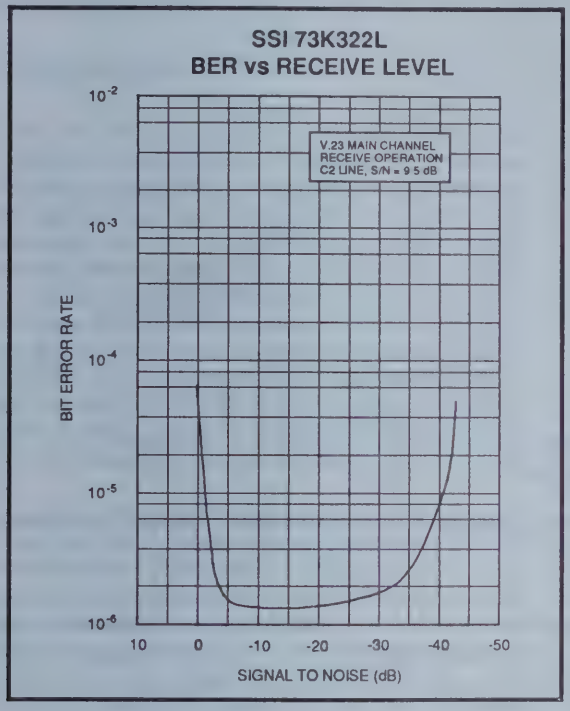
SSI 73K322L BER vs IDEAL RECEIVER


IDEAL RECEIVER 73K322L TRANSMITTER TO 73K322L RECEIVER HIGH BAND RECEIVE -30 dBm DPSK OPERATION 1200 BPS
C2
C1 or 3002
FLAT
BIT ERROR RATE
SIGNAL TO NOISE (dB)

SSI 73K322L BER vs RECEIVE LEVEL

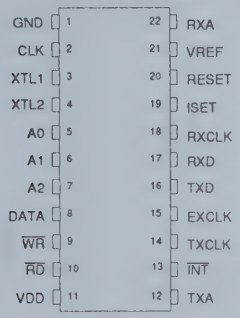



SSI 73K322L
BER vs PHASE JITTER
BIT ERROR RATE
HIGH BAND RECEIVE
DPSK OPERATION
3002 11.5 dB S/N
C2 10.8 dB S/N
SIGNAL TO NOISE (dB)
SSI 73K322L
BER vs CARRIER OFFSET
BIT ERROR RATE
HIGH BAND RECEIVE
DPSK OPERATION
3002 11.5 dB S/N
C2 10.8 dB S/N
SIGNAL TO NOISE (dB)
SSI 73K322L
(V.23 ONLY) BER vs S/N
BIT ERROR RATE
V.23 OPERATION
-40 dBM
C2 EQ. OFF
3002 EQ. OFF
3002 EQ. ON
FLAT EQ. OFF
BACK CHANNEL
FLAT EQ. ON
C2 EQ. ON
SIGNAL TO NOISE (dB)
SSI 73K322L
BER vs SIGNAL TO NOISE
BIT ERROR RATE
V.21 OPERATION
-40 dBM
FLAT HIGH BAND
C2 HIGH BAND
3002 HIGH BAND
LOW BAND RECEIVE
FLAT, 3002, AND C2 LINES
SIGNAL TO NOISE (dB)

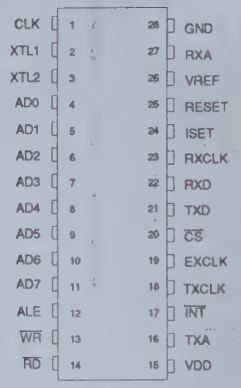

SSI 73K322L
BER vs RECEIVE LEVEL
V.23 MAIN CHANNEL
RECEIVE OPERATION
C2 LINE, S/N = 9.5 dB
BIT ERROR RATE
10-2
10-3
10-4
10-5
10-6
10
0
-10
-20
-30
-40
-50
SIGNAL TO NOISE (dB)

SSI 73K322L
CCITT V.23, V.22, V.21
Single-Chip Modem

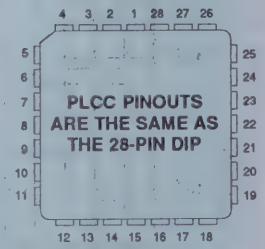
PACKAGE PIN DESIGNATIONS
(TOP VIEW)



400-Mil
22-Pin DIP



600-Mil
28-Pin DIP



28-Lead
PLCC

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 73K322L with Parallel Bus Interface		
28-Pin 5 Volt Supply		
Plastic Dual-In-Line	SSI 73K322L - IP	73K322L - IP
Plastic Leaded Chip Carrier	SSI 73K322L - IH	73K322L - IH
SSI 73K322L with Serial Interface		
22-Pin 5 Volt Supply		
Plastic Dual-In-Line	SSI 73K322SL - IP	73K322SL - IP

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SSI 73K324/K324L
CCITT V.22 bis, V.22, V.21, V.23 Single-Chip Modem

Advance Information

July, 1989

1

DESCRIPTION

The SSI 73K324 is a highly integrated single-chip modem IC which provides the functions needed to design a quad-mode CCITT compatible modem capable of operation over dial-up lines. The SSI 73K324 adds V.23 capability to the CCITT modes of SSI's 73K224 one-chip modem, allowing a one-chip implementation in designs intended for European markets which require this added fallback mode. The SSI 73K324 offers excellent performance and a high level of functional integration in a single 28-pin DIP. The device supports all V.22 bis, V.22, V.21, and V.23 operating modes, allowing both synchronous and asynchronous operation as defined by the appropriate standard.

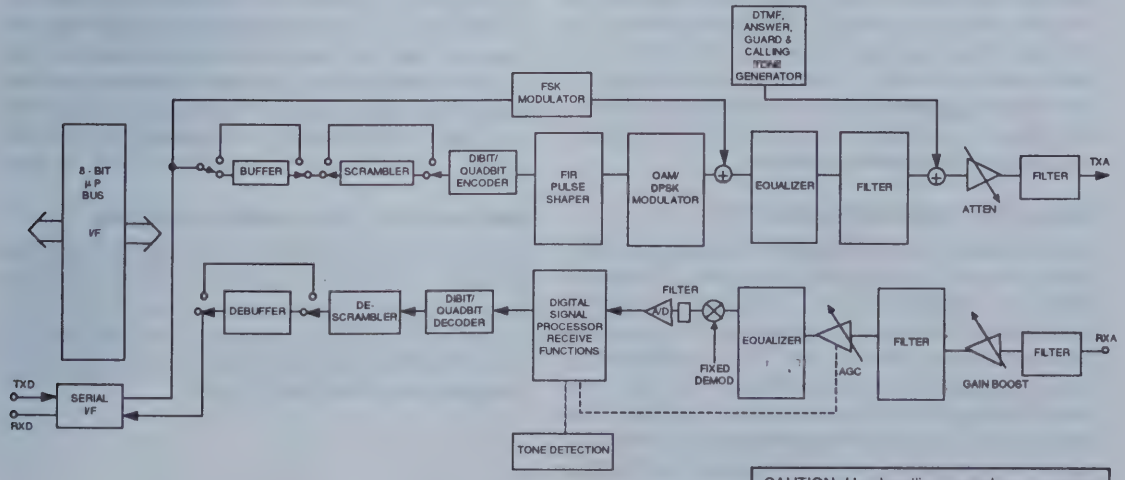
The SSI 73K324 is designed to appear to the Systems Engineer as a microprocessor peripheral, and will easily interface with popular one-chip microcontrollers (80C51 typical) for control of modem functions through its 8-bit multiplexed address/data bus. An optional serial command bus is also available for specialized applications not requiring a parallel interface. Data communications occurs through a separate serial port.

(Continued)

FEATURES

- **One-chip multi-mode CCITT V.22 bis, V.22, V.21, V.23 compatible modem**
- **FSK (75, 300, 1200 bit/s), DPSK (600, 1200 bit/s), or QAM (2400 bit/s) encoding**
- **Pin and software compatible with other SSI K–Series family one-chip modems**
- **Interfaces directly with standard microprocessors (8048, 80C51 typical)**
- **Serial or parallel microprocessor bus for control**
- **Selectable asynch/synch with internal buffer/de-buffer and scrambler/descrambler functions**
- **All synchronous (internal, external, slave) and asynchronous operating modes**
- **Adaptive equalization for optimum performance over all lines**
- **Programmable transmit attenuation (15 dB, 1 dB steps), and selectable receive boost (+12 dB)**
- **Call progress, carrier, answer tone, unscrambled mark, S1, calling tone (1300 Hz) and signal quality monitors**
- **DTMF, answer and guard tone generators**
- **Test modes available: ALB, DL, RDL, Mark, Space and Alternating bit patterns**
- **CMOS technology for low power consumption**

BLOCK DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

DESCRIPTION (Continued)

The SSI 73K324 offers full hardware and software compatibility with other products in Silicon Systems' K–Series family of single-chip modems, allowing system upgrades with a single component change. The SSI 73K324 is ideal for use in free-standing or integral system modem products where full-duplex 2400 bit/s operation with alternate mode capability is required. Its high functionality, low power consumption, and efficient packaging simplify design requirements and increase system reliability. A complete modem requires only the addition of the phone line interface, a control microprocessor, and RS-232 level converters for a typical system.

FUNCTIONAL DESCRIPTION

The SSI 73K324 is designed to provide a complete V.22 bis, V.22, V.21, and V.23 compatible modem on a chip. Many functions were included to simplify implementation in typical modem designs. In addition to the basic 2400 bit/s QAM, 1200/600 bit/s DPSK and 1200/300/75 bit/s FSK modulator/demodulator sections, the device also includes synch/asynch buffering, DTMF, guard, and calling tone generator capabilities. Handshake pattern detectors simplify control of connect sequences, and precise tone detectors allow accurate detection of call progress, answer back, and calling tones. All operating modes defined by the incorporated standards are included, and test modes are provided for simplified diagnostics. Most functions are selectable as options, and logical defaults are provided when override modes are activated. The device can be directly interfaced to a microprocessor via its 8-bit multiplexed address/data bus for control and status monitoring. Data communications takes place through a separate serial port.

QAM MODULATOR/DEMODULATOR

The SSI 73K324 encodes incoming data into quad-bits represented by 16 possible signal points with specific phase and amplitude levels. The baseband signal is then filtered to reduce intersymbol interference on the bandlimited telephone network. The modulator transmits this encoded data using either a 1200 Hz (originate mode) or 2400 Hz (answer mode) carrier. The demodulator, although more complex, essentially reverses this procedure while also recovering the data clock from the incoming signal. Adaptive equalization corrects for varying line conditions by automatically changing filter parameters to compensate for line characteristics.

DPSK MODULATOR/DEMODULATOR

The SSI 73K324 modulates a serial bit stream into di-bit pairs that are represented by four possible phase shifts as prescribed by the Bell 212A/V.22 standards. The baseband signal is then filtered to reduce intersymbol interference on the bandlimited 2-wire PSTN line. Transmission occurs on either a 1200 Hz (originate mode) or 2400 Hz carrier (answer mode). Demodulation is the reverse of the modulation process, with the incoming analog signal eventually decoded into di-bits and converted back to a serial bit stream. The demodulator also recovers the clock which was encoded into the analog signal during modulation. Demodulation occurs using either a 1200 Hz carrier (answer mode or ALB originate mode) or a 2400 Hz carrier (originate mode or ALB answer mode). The SSI 73K324 use a phase locked loop coherent demodulation technique that offers excellent performance. Adaptive equalization is also used in DPSK modes for optimium operation with varying line conditons.

FSK MODULATOR/DEMODULATOR

The FSK modulator/demodulator produces a frequency modulated analog output signal using two discrete frequencies to represent the binary data. V.21 frequencies of 980 and 1180 Hz (originate mark and space), or 1650 and 1850 Hz (answer mark and space) are used in V.21 mode. V. 23 mode uses 1300 and 2100 Hz for the main channel or 390 and 450 Hz for the back channel. Demodulatoion involves detecting the received frequencies and decoding them into the appropriate binary value. The rate converter and scrambler/descrambler are bypassed in the FSK modes.

PASSBAND FILTERS AND EQUALIZERS

High and low band filters are included to shape the amplitude and phase response of the transmit and receive signals and to provide compromise delay equalization as well as rejection of out-of-band signals. The transmit signal filtering corresponds to a Sin X/X frequency response characteristic.

ASYNCHRONOUS MODE

The asynchronous mode is used for communciation with asynchronous terminals which may transfer data at 600, 1200, or 2400 bit/s +1%, -2.5% even though the modem's output is limited to the nominal bit rate ±.01%. When transmitting in this mode the serial data on the TxD input is passed through a rate converter which inserts or deletes stop bits in the serial bit stream in order to output a signal that is the nominal bit rate ±.01%. This signal is then routed to a data scrambler and into the analog modulator where di-bit or quad-bit encoding results in the output signal. Both the rate converter and scrambler can be bypassed for handshaking, FSK, and synchronous operation as selected. Received data is processed in a similar fashion except that the rate converter now acts to reinsert any deleted stop bits and output data to the terminal at no greater than the bit rate plus 1%. An incoming break signal (low through two characters) will be recognized in accordance with the appropriate standard and passed through without incorrectly inserting a stop bit.

The SYNC/ASYNC converter has an overspeed mode which allows selection of an output speed range of either +1% or +2.3%. In the overspeed mode, some stop bits are output at 7/8 the normal width.

Similar to the transmit side, both the SYNC/ASYNC rate converter and the data descrambler are bypassed in the FSK modes.

SYNCHRONOUS MODE

Synchronous operation is possible only in the QAM or DPSK modes. Operation is similar to that of the asynchronous mode except that data must be synchronized to a clock and no variation in data transfer rate is allowable. Serial input data appearing at TXD must be valid on the rising edge of TXCLK.

TXCLK is an internally derived 1200 or 2400 Hz signal in internal mode and is connected internally to the RXCLK pin in slave mode. Receive data at the RXD pin is clocked out on the falling edge of RXCLK. The asynch/synch converter is bypassed when synchronous mode is selected and data is transmitted out at essentially the same rate as it is input.

PARALLEL BUS INTERFACE

Seven 8-bit registers are provided for control, option select, and status monitoring. These registers are addressed with the AD0, AD1, and AD2 multiplexed address lines (latched by ALE) and appear to a control microprocessor as seven consecutive memory locations. Five contol registers are read/write. The status detect and ID register are read only and cannot be modified except by modem response to monitored parameters.

SERIAL COMMAND INTERFACE

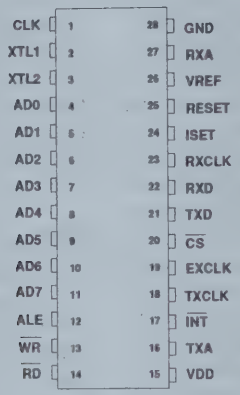
The serial command mode allows access to the SSI 73K324 control and status registers via a serial command port. In this mode the A0, A1, and A2 lines provide register addresses for data passed through the data pin under control of the $\overline{RD}$ and $\overline{WR}$ lines. A read operation is initiated when the $\overline{RD}$ line is taken low. The next eight cycles of EXCLK will then transfer ou eight bits of the selected addresss location LSB first. A write takes place by shifting in eight bits of data LSB first for eight consectuive cycles of EXCLK. $\overline{WR}$ is then pulsed low and data transfer into the selected register occurs on the rising edge of $\overline{WR}$.

TONE GENERATOR

The tone generator will output one of 16 standard dual tones determined by a 4-bit binary value and TX DTMF mode bit previously loaded into the tone register. Guard, answer, and calling tones are also provided by this section.

SSI 73K324/K324L
CCITT V.22 bis, V.22, V.21, V.23
Single-Chip Modem

PACKAGE PIN DESIGNATIONS
(TOP VIEW)



600-Mil
28-Pin DIP

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Performance Testing
SSi K-Series
Single-Chip Modem Family

WHY MODEM PERFORMANCE IS IMPORTANT

In today's world of expanding communications, the modem has become an essential element in providing data communications capability for such applications as personal computers, lap-top PCs, and hand-held portable terminals. To fit the requirements of these systems, the modem must become more compact even as it becomes more complex. As more modem functions are integrated onto a single chip, it is the modem IC that becomes the key to designing small footprint modems that integrate well into today's computer applications.

Trying to compare competitive modem ICs by analyzing published technical specifications can be misleading. No meaningful comparisons can be made, because data sheets provide little useful performance information. Products that appear functionally competitive can vary widely in datacom performance.

Hidden differences in modem architecture can have a profound effect on overall modem operation. Where one modem IC might perform well within a real-world operating environment, another seemingly comparable IC might perform just marginally. So ultimately what the designer needs is a way to realistically compare modem ICs by their ability to perform, error-free, under real-world operating conditions.

THE REAL WORLD OF TELECOMMUNICATIONS

Telephone lines vary. In different geographical areas, factors such as age, technology, and upkeep of equipment all contribute to variations in the physical operating environment. The physical mechanics of call-routing introduce other uncertainties, since call-routing can be completely random in a typical dial-up connection due to the automatic routing techniques being used.

Also, differences in the switching and multiplexing methods used in different locations, as well as differences in the conductive medium (copper-wire or fiber-optics), all add to the mix, making it difficult to design a modem that will perform well in a manner that is transparent to all of these factors.

These equipment and routing factors that adversely affect data communications create performance aberrations that are known collectively as line impairments. These line impairments cause the real-world side-effects that define the actual environment in which the modem, and the modem IC, must survive and perform.

Line Impairments

Generally, line impairments can be classified into four categories: line noise, signal-level variations, phase distortion, and carrier offset.

Line Noise

Line noise is the most common impairment to efficient datacommunications and can manifest itself in many ways. Ambient noise, for example, can be caused by copper line conductors. Wideband noise can be generated by hybrid repeater amplifiers in the network. Crosstalk from adjacent lines can sometimes couple into the connection and add to noise on the line.

Generally, noise impairments occur within the 300 to 3000 Hz voiceband, since other frequencies are attenuated by repeaters or filters on the line. The specific quality that enables a modem IC to operate error-free in a noisy line environment can be found in its design architecture, which reflects the functional efficiency of both its components and its circuit layout.

Signal-Level Variations

High signal-level is one impairment in this category. This stronger-than-normal signal can occur when an unusually efficient connection is made, as when routed through a PBX or when the transmitter and receiver are within close proximity to one another. A maximum level for normal operation on a dial-up line might be -10 dBm. An abnormally high level might approach 0 dBm.

Low signal-levels result from high line-resistance or from long, circuitous call-routing paths. The lowest signal level expected on a dial-up line is -45 dBm. The ability of the modem to handle abnormally high or low signal-levels is defined by its dynamic range.

Gain hits are short, quick changes in the receive signal's amplitude. The phenomenon can be caused by trunk-line switching activity or by sudden changes in line impedance, both of which can cause a breakdown in data-transfer integrity. Gain hits can be offset by fast-tracking capability within the AGC circuitry of the modem IC.

Phase Distortion

These impairments include phase jitter, phase hits, and group/envelope delay. Phase jitter is a periodic shift in the phase of the received carrier, which can be caused by variations in the line characteristics or by imperfections in the transmitting modem. Phase hits are more instantaneous in nature. They are characterized by significant changes in phase in the received carrier and are caused by ongoing switching action in the dial-up network. Group delay (envelope delay) results from reactive line-impedance characteristics that induce phase shifts in the frequencies present in the received signal. The modem must correct for group-delay distortion. Failure to do so can result in a phenomenon known as intersymbol interference. This occurs when frequency elements from one signal-modulation period overlap those of another, making it difficult to detect the original phase-encoded information in the signal, thus introducing data errors.

Carrier Offset

This impairment refers to a shift in frequency between the transmitted signal and the received signal. The condition is often introduced during long-distance call routing, where frequency-division multiplexing combines lower-frequency voiceband signals into a higher frequency signal. This phenomenon can be offset by the modem's phase-lock-loop tracking capabilities.

HOW MODEMS CAN BE COMPARED FOR PERFORMANCE

In order to compare modem ICs realistically, the design engineer needs to test each device under conditions that reflect real-life telephone line conditions. To achieve this, a test environment must be set up to simulate a set of actual line characteristics that conform to specifications defined by Bell System published standards. The engineer can then subject each test modem to artificially induced impairments under each of these line-standard conditions and compare the specific performance of competitive modems. A range of line conditions must be used to show how the modem will operate over the random variety of lines that might be encountered in typical operation.

Line Standards

Characteristics for dial-up telephone lines are not commonly specified, but leased lines are conditioned lines for which linear-distortion characteristics, including frequency-response and envelope-distortion parameters, are guaranteed by the telephone company. The Bell System line standards define four premium line conditions that operate with characteristics similar to those found in dial-up lines. These lines, which allow for modem performance testing over a wide range of representative conditions, include the following:

The 3002 Line is the lowest quality leased line and represents the poorest environment for accurate data communications. Allowable amplitude variation is 15 dB over the voiceband range. Envelope delay can vary as much as 1750 microseconds over the 800 to 2600 Hz range.

The C1 Line is conditioned to a greater extent than the 3002 line and can be considered to represent the average in dial-up line characteristics. Amplitude variation over the frequency band of interest is limited to 8 dB. Allowable envelope delay is the same as for the 3002 line.

The C2 Line represents an intermediate-quality line for modem testing. Frequency response is limited to 8 dB amplitude variation. Envelope delay is improved to not more than 500 microseconds over a 1000 to 2600 Hz range.

The C4 Line represents the best line conditions to be expected in a dial-up telephone environment. Optimum modem performance would be expected using this standard. Group delay or attenuation is negligible. Frequency response is limited to 8 dB. Envelope delay distortion is held to less than 300 microseconds over a 1000 to 2600 Hz range.

The Testing Method

To qualify modem ICs for performance, the test method must be uniformly applied. A test unit is used to simulate each of the Bell System line standards and to generate the environmentally representative line impairments. A typical test set-up includes a line simulator, a personal computer, an RMS voltmeter, and a reference modem to test against. Control of the test parameters is handled by the PC connected to the test fixture through a GPIB data bus. The PC sets up and controls the line simulator, monitors the results, and accumulates the error count for each iteration.

Two modem ICs are compared in a typical test sequence. The modem IC to be tested is connected to the modem testing equipment via a breadboard evaluation fixture and is fed a continuous data stream for testing. The tester monitors the data received from the test modem and the data bit-errors are counted and plotted to signify the ratio between the number of bits transmitted compared to the number of transmission error-bits. This results in a statistical bit-error rate (BER).

The test method calls for a large sample of data errors to be simulated for each device, under each line condition. Multiple data points are taken for each test for each device. Test message data is transmitted in a random, broad-range pattern. Each data point results from the transmission of a million data bits and a complete test sequence on a single modem IC could represent 100 hours of test time before a realistic error sampling might be realized.

The SSI K-Series Modem ICs

Silicon Systems' K-Series family of modem ICs use an integrated analog/digital design philosophy for enhanced high-performance operation, which virtually eliminates data-error-related modem failures. These pin and function-compatible family products comply with the full range of relevant worldwide operating standards for data transfer speeds ranging from 300 to 2400 bit/s. The SSI 73K224, the industry's first 2400 bit/s single-chip modem for both U.S. and European standards, features adaptive equalization, which further enhances performance by giving the modem the ability to adapt automatically to varying line conditions.

The K-Series modem ICs are used in the sample test curves presented with this document as a base against which competitive performance information can be compared.

MODEM PERFORMANCE CHARACTERISTICS

The curves presented here define modem IC performance under a variety of line conditions while inducing disturbances that are typical of those encountered during data transmission on public service telephone lines. Test data was taken using an AEA Electronics' "Autotest I" modem test set and line simulator, operating under computer control. All tests were run full-duplex, using a Concord Data Systems 224 as the reference modem. A 511 pseudo-random-bit pattern was used with $1X10^6$ bits transmitted for each data point. Noise was C-message weighted and all signal-to-noise (S/N) ratios reflect total power measurements similar to the CCITT V.56 measurement specification. The individual tests are defined as follows.

BER vs.S/N

This test measures the ability of the modem to operate over noisy lines with a minimum of data-transfer errors. Since some noise is generated in the best of dial-up lines, the modem must operate with the lowest S/N ratio possible. Optimum modem performance is indicated by test curves that are closest to the zero axis. A narrow spread between curves representing the four line parameters indicates minimal variation in performance while operating over a range of aberrant operating conditions. Typically, a PSK modem will exhibit better BER-performance test curves operating in the highband range than in the lowband.

Ideal Receivers

The modem transmit function is easier to implement than the receive function. Because of this, it is generally assumed that only the receiver needs to be analyzed, but in practice this is not the case. Transmitter variations from unit to unit can affect overall modem performance. In this graph, the curve indicates the effect of the transmitter on the highband receive performance of an ideal receiver.

BER vs. Receive Level

This test measures the dynamic range of the modem. Because signal levels vary widely over dial-up lines, the widest possible dynamic range is desirable. The minimum Bell specification calls for 36 dB of dynamic range. S/N ratios are held constant at the indicated values while the receive level is lowered from a very high to very low signal levels. The width of the "bowl" of these curves, taken at the BER point, is the measure of dynamic range.

BER vs. Phase Jitter

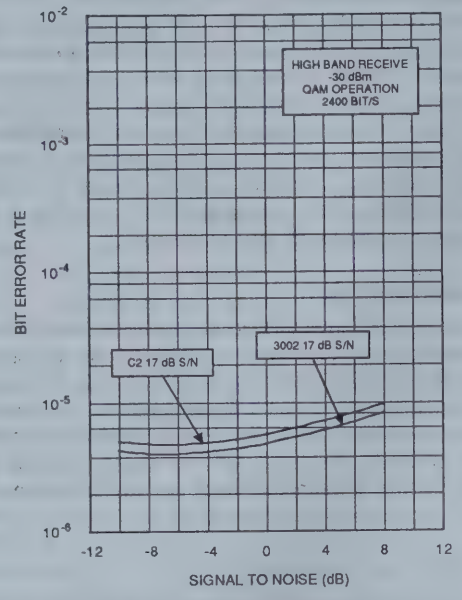
PSK and QAM modulation is sensitive to phase jitter. Modems using these techniques need to be as tolerant as possible of phase jitter on the line. In this test, relatively flat curves indicate minimal degradation of performance when phase jitter is encountered on the line.

BER vs. Carrier Offset

This parameter indicates how the modem's performance is affected by the shifts in frequency encountered in normal public telephone network operation. Flat curves are an indication that there is no performance degradation from frequency offsets. The SSI K-Series modem ICs use a second-order, carrier-tracking phase-lock-loop that is insensitive to carrier offsets in excess of 10 Hz. Both the Bell and European/Japanese CCITT specifications allow as much as 7-Hz offset.

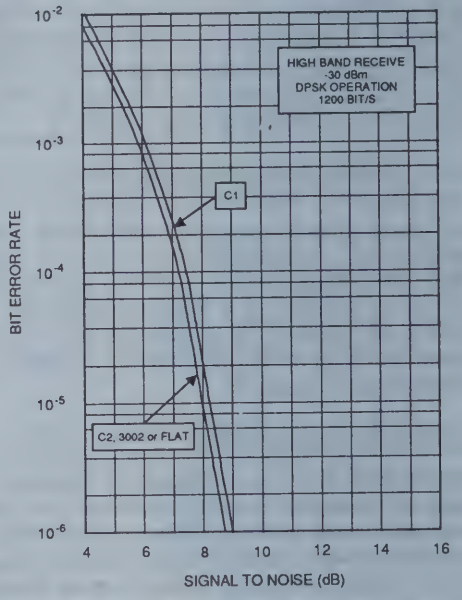
SSI 73K224L BER vs CARRIER OFFSET

PRELIMINARY



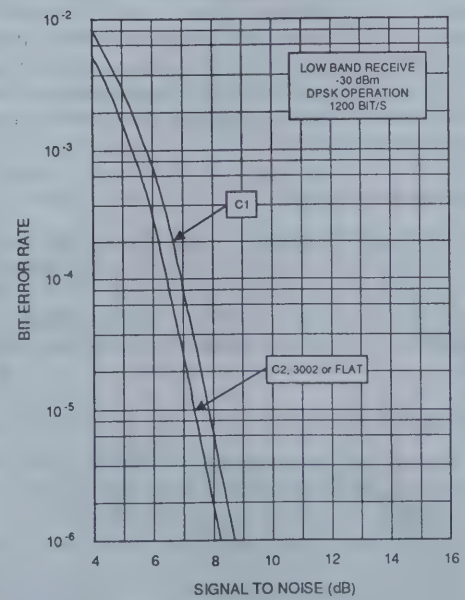
SSI 73K224L BER vs S/N

PRELIMINARY

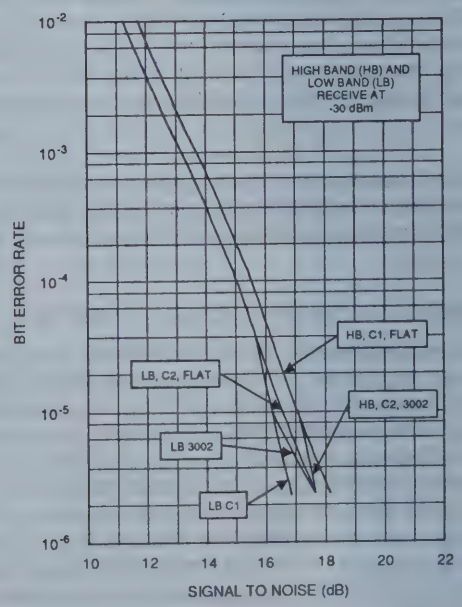


SSI 73K224L BER vsS/N

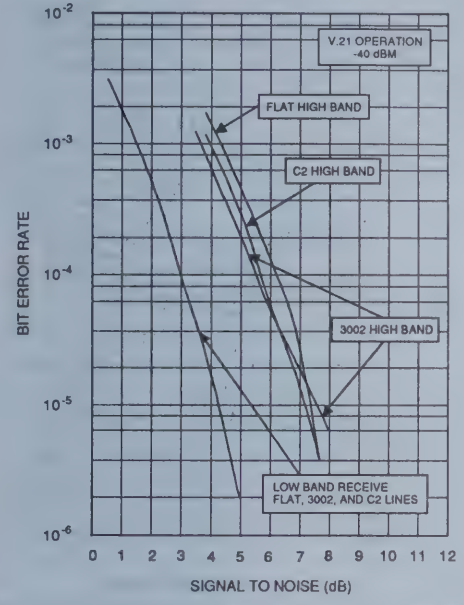
PRELIMINARY



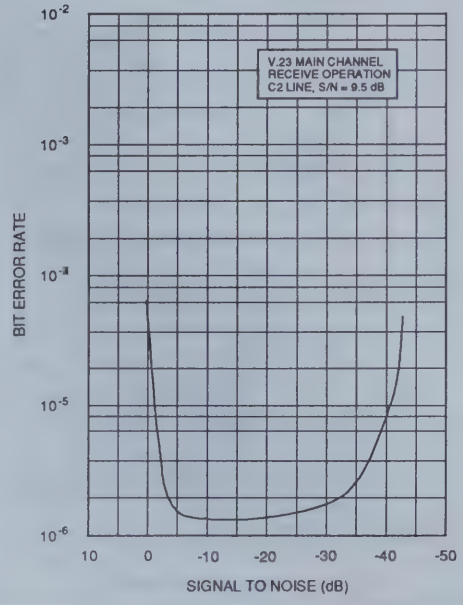
SSI 73K224L BER vs QAM



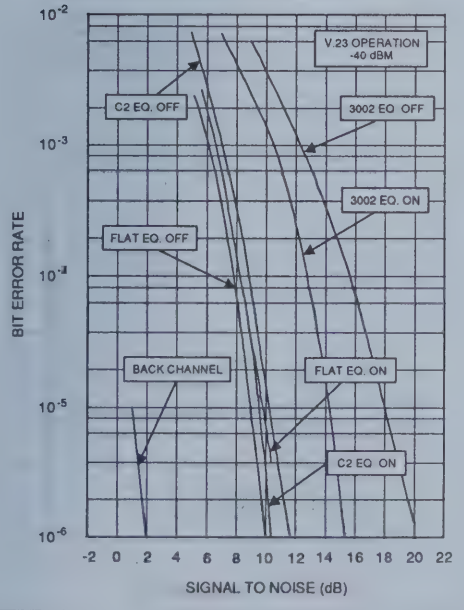
SSI 73K321L, 73K322L
BER vs SIGNAL TO NOISE



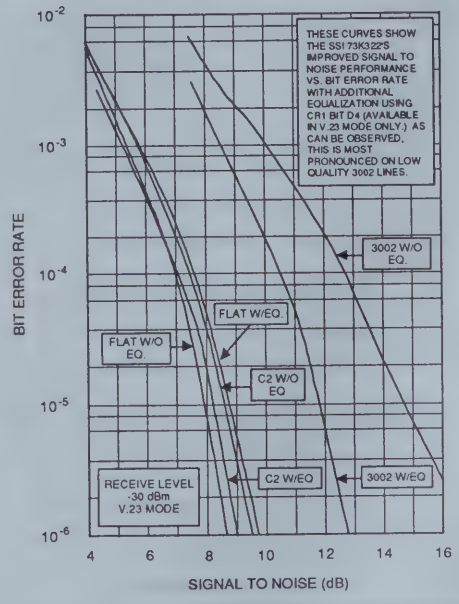
SSI 73K321L, 73K322L
BER vs RECEIVE LEVEL



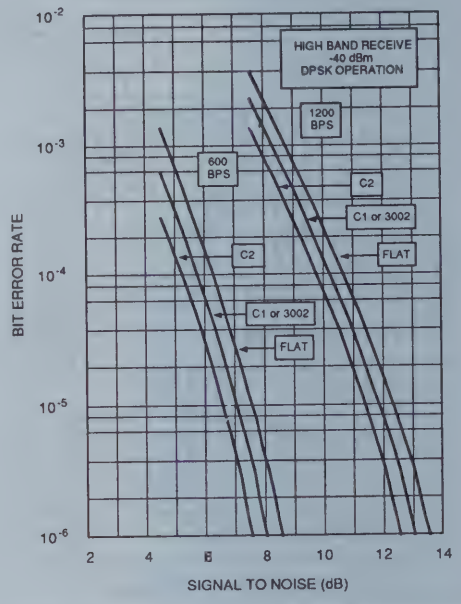
SSI 73K321L, 73K322L
(BELL 202 ONLY) BER vs S/N



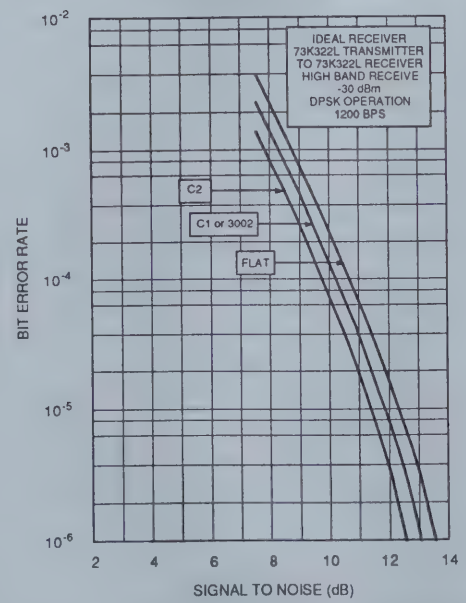
SSI 73K321L, 73K322L (V.23 ONLY)
BER vs S/N


THESE CURVES SHOW THE SSI 73K322'S IMPROVED SIGNAL TO NOISE PERFORMANCE VS. BIT ERROR RATE WITH ADDITIONAL EQUALIZATION USING CR1 BIT D4 (AVAILABLE IN V.23 MODE ONLY.) AS CAN BE OBSERVED, THIS IS MOST PRONOUNCED ON LOW QUALITY 3002 LINES.
3002 W/O EQ.
FLAT W/EQ.
FLAT W/O EQ.
C2 W/O EQ.
C2 W/EQ
3002 W/EQ
RECEIVE LEVEL -30 dBm V.23 MODE
BIT ERROR RATE
SIGNAL TO NOISE (dB)

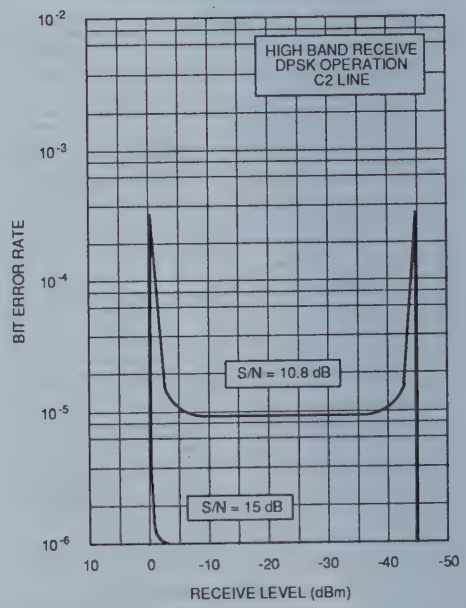
SSI 73K322L
BER vs S/N

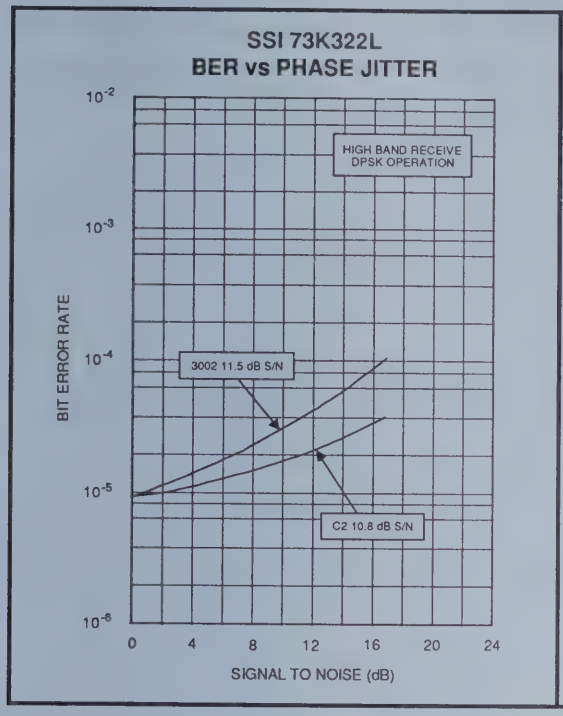


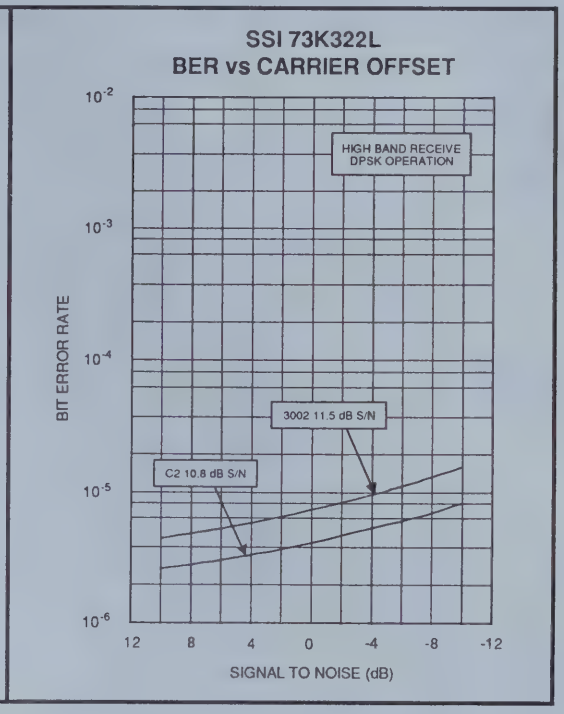
SSI 73K322L
BER vs IDEAL RECEIVER


IDEAL RECEIVER 73K322L TRANSMITTER TO 73K322L RECEIVER HIGH BAND RECEIVE -30 dBm DPSK OPERATION 1200 BPS
C2
C1 or 3002
FLAT
BIT ERROR RATE
SIGNAL TO NOISE (dB)

SSI 73K322L
BER vs RECEIVE LEVEL




SSI 73K322L
BER vs PHASE JITTER
HIGH BAND RECEIVE
DPSK OPERATION
3002 11.5 dB S/N
C2 10.8 dB S/N
BIT ERROR RATE
10^{-2}
10^{-3}
10^{-4}
10^{-5}
10^{-6}
0
4
8
12
16
20
24
SIGNAL TO NOISE (dB)


SSI 73K322L
BER vs CARRIER OFFSET
HIGH BAND RECEIVE
DPSK OPERATION
3002 11.5 dB S/N
C2 10.8 dB S/N
BIT ERROR RATE
10^{-2}
10^{-3}
10^{-4}
10^{-5}
10^{-6}
12
8
4
0
-4
-8
-12
SIGNAL TO NOISE (dB)

NOTES:

Section 2

MODEM PROTOCOL AND CONTROLLERS

SSI 73D2180
Bell 212A/103, CCITT V.22, V.21 Modem Device Set

July, 1989

2

DESCRIPTION

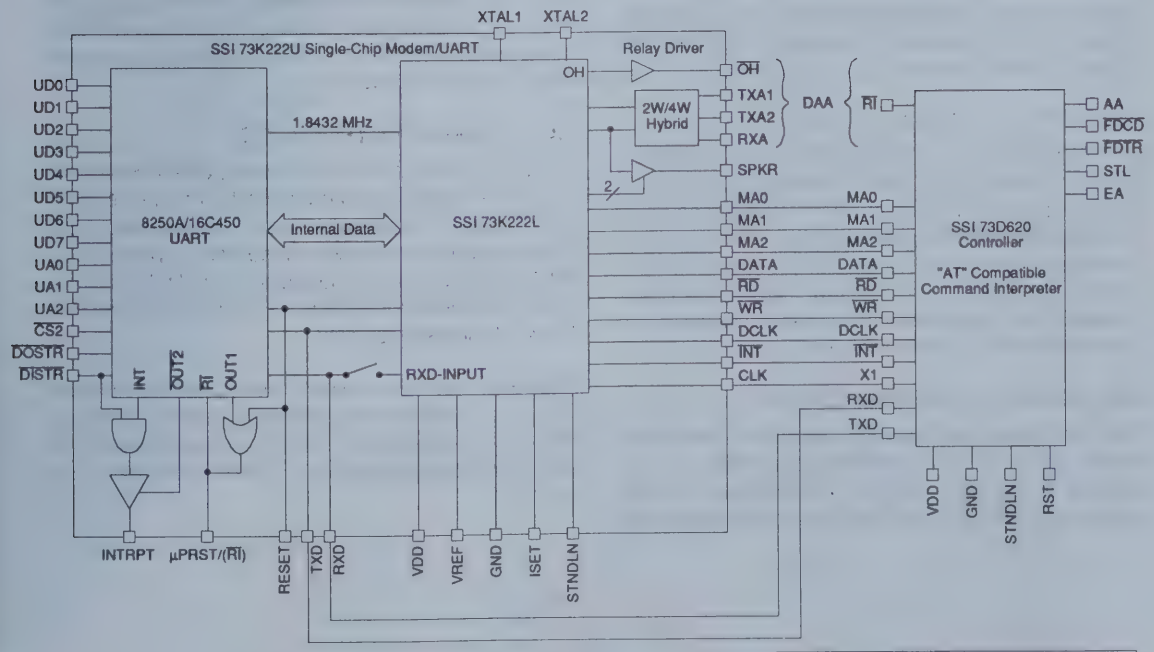
The SSI 73D2180 consists of two CMOS integrated circuits which provide the data pump functions and command interpretation required to construct a high performance 1200 bit/s full-duplex intelligent modem. The 73D2180 includes operating modes compatible with CCITT V.22, V.21, Bell 212A, and 103 data-communications standards. Using advanced processes that include analog and switched capacitor filter techniques, the SSI 73D2180 offers excellent performance and a high level of functional integration in a compact two-chip set. The 73D2180 provides a Hayes "AT" compatible command interpreter, a 16C450 compatible UART and an enhanced version of Silicon Systems' 73K222L single-chip modem.

The 73D2180 is ideal for use in integral system modem products where full-duplex 1200 bit/s data-communications over the 2-wire public service telephone network is desired.

FEATURES

- Multi-mode CCITT V.22/V.21 & Bell 212A/103 compatible device set for intelligent modem designs
- Full duplex operation at 0-300 and 1200 bit/s
- Includes high-level "AT" command interpreter compatible with 1200 bit/s industry standard products
- Complete complement of "AT" modem features
- Selectable automatic speed detect, handshake and autobaud functions
- Dynamic range from 0 to -45dBm
- Call progress, carrier and answer tone detectors provide intelligent dialing functions
- DTMF and CCITT guard tone generators
- Test modes available - ALB, DL, RDL for complete test capability
- Space efficient 40-pin DIPs or 44-pin PLCCs
- Low power consumption (115 mW using +5V)

BLOCK DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

OPERATION

The SSI 73D2180 is a complete Bell 212A/103 and V.22/V.21 intelligent modem contained in two IC's. The device set forms the basis for a high performance integral modem product with self-contained command interpreter and a 16C450 compatible UART.

The 73D2180 chip set is composed of the SSI 73K222U single-chip modem/UART and the SSI 73D620 controller chip. The 73K222U is a single-chip modem integrated on the same die with a 16C450 compatible UART. The 73K222U interfaces with the main CPU via a parallel demultiplexed bus. Commands and data are passed to the chip set over this port and are serialized by the on-board UART. The 73D620 controller chip hosts an "AT" compatible command interpreter. This controller monitors the internal serial bus of the 73K222U (UART output) for user commands which it interprets and executes. The 73D620 controller communicates with the 73K222U modem/UART via a serial port. Refer to the block diagram on Page 1 and to the 73K222U Modem/UART Data Sheet for further details.

The SSI 73K222U provides the DPSK and FSK modulator/demodulator functions, call progress and handshake tone monitors, test modes and a tone generator capable of producing DTMF, answer and CCITT guard tones. This device supports the V.22, V.21 and Bell 212A/103 operating modes.

DPSK MODULATOR/DEMODULATOR

In DPSK mode the 73D2180 modulates the 1200 bit/s incoming data into dibits represented by four possible signal points as specified by CCITT recommendation V.22 and Bell 212A. The modulator transmits this encoded data using either a 1200 Hz (originate mode) or 2400 Hz (answer mode) carrier. The demodulator reverses this procedure and recovers the data and data clock from the incoming signal.

FSK MODULATOR/DEMODULATOR

The FSK transmitter frequency modulates the analog output signal using two discrete frequencies to represent the binary data. The Bell 103 standard frequencies of 1270 and 1070 Hz (originate mark and space) and 2225 and 2025 Hz (answer mark and space) or the V.21 standard frequencies of 980 and 1180 Hz (originate mark and space) and 1650 and 1850 Hz (answer mark and space) are used when this mode is selected. Demodulation involves detecting the received frequencies and decoding them into the appropriate binary value.

PASSBAND FILTERS AND EQUALIZERS

A bandsplit filter is included to shape the amplitude and phase response of the transmit signal to a square root 75% raised cosine and provide rejection of out-of-band signals in the receive channel.

AUTOMATIC HANDSHAKE

The SSI 73D2180 will automatically perform a complete handshake as defined by the CCITT V.22, V.21 and Bell 212A/103 standards to connect with a remote modem. The 73D2180 automatically determines the speed and operating mode and adjusts its operation to correspond to that of an originating modem when answering a call.

TEST MODES

The SSI 73D2180 allows use of Analog Loopback, Digital Loopback and Remote Digital Loopback test modes. Full test mode capability allows testing of the modem and interface functions from the local terminal using the appropriate control commands, or remotely using the RDL function.

"AT" COMMAND INTERPRETER

The SSI 73D620 controller includes an AT command interpreter which is compatible with the Hayes 1200 Smartmodem™ command set. Functions and features included with intelligent modems are provided by the 73D620 controller including auto-dial/auto-answer, handshake with auto-fallback, and selectable pulse or DTMF dialing sequences.

The 73D620 is also compatible with other SSI modem/UART family members and can be used interchangably with these products. Modes not available will be automatically disabled by the 73D620 controller in this case.

PIN DESCRIPTION - SSI 73D620 CONTROLLER

GENERAL

NAME	DIP	PLCC	TYPE	DESCRIPTION
VDD	40	44	I	+5V supply ±10%. Bypass with a 0.1 µF capacitor to ground.
GND	20	22	I	Digital ground
X1	19	21	I	11.0592 MHz clock input from the 73K222U.
RST	9	10	I	Reset Input. A high on this pin for two machine cycles while the oscillator is running resets the device. An internal pull-down resistor permits power-on reset using a 0.1 µF capacitor to the 5V supply.
STNDLN	13	15	I	Stand alone. Tie low for proper operation as a command interpreter. Tie high to disable device.
EA	31	35	I	Tie to VDD.
AA	28	31	I	Auto Answer at power-up. Tie high to enable auto answer on power-up feature. Controller will automatically answer a ring as specified in the S11 register. Tie low to disable auto answer on power-up.
$\overline{\text{FDCD}}$	14	16	I	Force on data carrier detect. Tie low to permanently force on data carrier detect indication to controller. Tie high or leave floating to allow carrier detection from telephone line.
$\overline{\text{FDTR}}$	15	17	I	Force on data terminal ready. Tie low to permanently force on the data terminal ready indication to the controller. Tie high or leave floating to allow data terminal ready indication to be obtained from the 73K222U register.
STL	16	18	I	Switched telephone lines. Tie high or leave floating if operating with the public switched telephone network lines. Tie low if operating with leased lines.
$\overline{\text{RI}}$	17	19	I	Ring indication. Input to the controller from the telephone ring isolation circuit.

PIN DESCRIPTION - SSI 73D620 CONTROLLER (Continued)

MODEM INTERFACE

NAME	DIP	PLCC	TYPE	DESCRIPTION
MA0-MA2	6-8	7-9	O	See SSI 73K222U pin description
DATA	1	2	I/O	See SSI 73K222U pin description
$\overline{RD}$	4	5	O	See SSI 73K222U pin description
$\overline{WR}$	5	6	O	See SSI 73K222U pin description
DCLK	2	3	O	See SSI 73K222U pin description
INT	12	14	O	See SSI 73K222U pin description
RXD	10	11	I	See SSI 73K222U pin description
TXD	11	13	I	See SSI 73K222U pin description

Note: Unused 73D620 controller pins are active, but not used for this application. These pins should be left floating.

PIN DESCRIPTION - SSI 73K222U

GENERAL

NAME	DIP	PLCC	TYPE	DESCRIPTION
VDD	40	44	I	+5V Supply ±10%, bypass with a 0.1 and a 22 µF capacitor to GND.
GND	20	22	I	Ground. Connect to analog ground.
VREF	19	21	O	VREF is an internally generated reference voltage which is externally bypassed by a 0.1 µF capacitor to the system ground.
ISET	9	11	I	The analog current is set by connecting this pin to VDD through a 2MΩ resistor. ISET should be bypassed to GND. Alternatively, an internal bias can be selected by connecting ISET to GND, which will result in a larger worst-case supply current due to the low tolerance of on-chip resistors. Bypass with .1µF capacitor if resistor is used.
XTAL1, XTAL2	25 24	27 26	I I	These pins are inputs for the internal crystal oscillator requiring an 11.0592 MHz crystal. XTAL2 can also be driven from an external clock.
CLK	21	23	O	Output Clock. This pin provides an 11.0592 MHz clock to drive the 73D620 controller.

GENERAL (Continued)

NAME	DIP	PLCC	TYPE	DESCRIPTION
RESET	10	12	I	Reset. An active signal (high) on this pin will put the chip into an inactive state. The control register bits (except the Receiver Buffer, Transmitter Holding, and Divisor latches) will be reset. The output of the CLK pin will be set to the crystal frequency. An internal pull-down resistor permits power-on reset using a 0.1μF capacitor connected to the 5V supply.
STNDLN	15	17	I	Tie low to enable the dual-port mode of the chip. This is required in order to operate properly with the 73D620.

UART INTERFACE

NAME	DIP	PLCC	TYPE	DESCRIPTION
UA0-UA2	37-39	41-43	I	UART Address. These pins determine which of the UART registers is being selected during a read or write on the UART data bus. The contents of the DLAB bit in the UART's Line Control Register also control which register is referenced. See the SSI 73K222U data sheet.
UDO-UD7	27-34	30-37	I/O	UART Data. Data or control information to the UART registers is carried over these lines.
$\overline{\text{DISTR}}$	35	38	I	Data Input Strobe. A low on this pin requests a read of the internal UART registers. Data is output on the D0-D7 lines if $\overline{\text{DISTR}}$ and $\overline{\text{CS2}}$ are active.
$\overline{\text{DOSTR}}$	36	39	I	Data Output Strobe. A low on this pin requests a write of the internal UART registers. Data on the D0-D7 lines are latched on the rising edge of $\overline{\text{DOSTR}}$. Data is only written if both $\overline{\text{DOSTR}}$ and $\overline{\text{CS2}}$ are active.
$\overline{\text{CS2}}$	1	2	I	Chip Select. A low on this pin allows a read or write to the UART registers to occur.
INTRPT	5	7	O	UART Interrupt. This signal indicates that an interrupt condition from the UART has occurred. If the Enable 8250A interrupt bit in the interrupt Enable Register is 0 the interrupt is gated by the $\overline{\text{DISTR}}$ signal to provide compatibility with the 8250B. The output can be put in a high impedance state with the OUT2 register bit in the Modem Control Register. See the SSI 73K222U data sheet.

PIN DESCRIPTION - SSI 73K222U (Continued)

ANALOG / LINE INTERFACE

NAME	DIP	PLCC	TYPE	DESCRIPTION
TXA1, TXA2	3 4	4 5	O O	Transmitted Analog (differential). These pins provide the analog output signals to be transmitted to the phone line. The drivers will differentially drive the impedance of the line transformer and the impedance matching resistor. An external hybrid can also be built using TXA1 as a single ended transmit signal; in such a case, TXA2 should be left floating.
RXA	16	18	I	Received Analog. This pin inputs analog signals from the line transformer to the two-to-four wire hybrid. This input can also be taken directly from an external hybrid.
SPKR	17	19	O	Speaker Output. This pin outputs the received signal through a programmable attenuator stage, which controls volume or disables the speaker.
$\overline{OH}$	18	20	O	Off-hook relay driver. This signal is an open drain output capable of sinking 20mA and is used for controlling a hook relay.

MICROPROCESSOR INTERFACE (STNDLN = 0)

NAME	DIP	PLCC	TYPE	DESCRIPTION
MA0-MA2	12-14	14-16	I	Modem Address Control. These lines carry register addresses for the modem registers and are valid throughout any read or write operation.
DATA	22	24	I/O	Serial Control Data. Serial control data to be read/written is clocked in/out on the falling edge of the DCLK pin. The direction of data transfer is controlled by the state of the $\overline{RD}$ pin. If the $\overline{RD}$ pin is active (low) the DATA line is an output. Conversely, if the $\overline{RD}$ pin is inactive (high) the DATA line is an input.
$\overline{RD}$	23	25	I	Read. A low on this input informs the SSI 73K222U that control data or status information is being read by the processor from a modem register.
$\overline{WR}$	26	28	I	Write. A low on this input informs the SSI 73K222U that control data or status information is available for writing into a modem register. The procedure for writing is to shift in data LSB first on the DATA pin for eight consecutive cycles of DCLK and then to pulse $\overline{WR}$ low. Data is written on the rising edge of $\overline{WR}$.

MICROPROCESSOR INTERFACE (STNDLN = 0)

NAME	DIP	PLCC	TYPE	DESCRIPTION
DCLK	11	13	I	Data Clock. The falling edge of this clock is used to strobe control data for the modem registers in or out on the DATA pin. The procedure for a WRITE is to shift in data LSB first on the DATA pin for eight consecutive cycles of DCLK and then to pulse $\overline{WR}$ low. Data is written on the rising edge of $\overline{WR}$. The falling edge of the $\overline{RD}$ signal must continue for eight cycles of DCLK in order to read all eight bits of the reference register. Read data is provided LSB first. Data will not be output unless the $\overline{RD}$ signal is active.
$\overline{INT}$	2	3	O	Modem Interrupt (with weak pull-up). This output signal is used to inform the 73D620 controller that a change in a modem detect flag has occurred. The controller then reads the Modem Detect Register to determine which detect triggered the interrupt. $\overline{INT}$ stays active until the controller reads the Modem Detect Register or does a full reset.
µPRST	8	10	O	Microprocessor Reset. This output signal is used to provide a hardware reset to the controller. This signal is high if the RESET pin is high or the MCR bit D3 (OUT1) bit is set. See the SSI 73K222U data sheet.
RXD	6	8	O	RXD outputs data received by modem from telephone line. This data is monitored by the 73D620 controller.
TXD	7	9	O	TXD is serial output of UART. This data is monitored by the 73D620 controller which checks for and executes the "AT" commands downloaded from the computer's CPU.

"AT" COMMANDS SUPPORTED
(Note: s=string; n=decimal, 0-255; x=Boolean, 0/1=false/true)

COMMAND	OPTIONS	DEFAULT
A/	Repeats last command line	N/A
A	Answer	N/A
Bx	BELL/CCITT = 1/0*	1
Ds	Dial string specified by s	No string
Ex	Command echo, 0/1 = off/on	1
Hn	Hook status, 0/1 = on/off	N/A
In	ID code, 0/1/2/3/4 (see Table 5)	N/A
Ln	Speaker volume, (0)1/2/3 = lo/med/hi	2
Mn	Speaker, 0/1/2/ = control (see Table 3)	1
On	Online, 0/1/2/ = on-line/on-line with remote digital loopback (see Table 4)	N/A
P	Pulse dial	Pulse
Qx	Quiet result, 0/1 = 1-quiet	0
R	Reverse originate	N/A
Sn=n	Set S register (see Table 2)	N/A
Sn?	Return value in register n (see Table 2)	N/A
T	Touch tone dial	Pulse
Vx	Verbose result, 0/1 = off/on	1
Xn	Result code, 0/1/2/3/4 (see Table 1)	4
Yx	Enable long space disconnect, 1 = enable	0
Z	Restore all default settings	N/A

*B0 command (CCITT mode) is operational only when using K-series modem/UARTs that include CCITT modes.

Dial string arguments:

, = delay	@ = silent answer	! = flash
; = return to command	W = wait for tone	R=reverse mode

TABLE 1: Result Codes

Xn	VOCAL/NUMERIC RESULT CODE
X0	OK/0, CONNECT/1, RING/2, NO CARRIER/3, ERROR/4
X1	All functions of X0 + CONNECT (RATE)/1 = 300, 5 = 1200
X2	All functions of X1 + NO DIAL TONE/6
X3	All functions of X1 + BUSY/7
X4	All functions of X3 + NO DIAL TONE/6

TABLE 2: S Registers Supported

NUMBER	FUNCTION	UNITS	DEFAULT
S0	Answer on ring	No. of rings	000[1]
S1	Ring counter	No. of rings up to 8	000
S2	Escape code	ASCII CHR$( )	043
S3	Carriage return	ASCII CHR$( )	013
S4	Line feed	ASCII CHR$( )	010
S5	Back space	ASCII CHR$( )	008
S6	Wait for dial tone	Seconds	002
S7	Wait for carrier	Seconds	030
S8	Pause time	Seconds	002
S9	Carrier valid	100 milliseconds	006
S10	Carrier drop out	100 milliseconds	007
S11	DTMF tone duration	1 millisecond	070
S12	Escape guard time	20 milliseconds	050
S13	Bit mapped register		N/A
S14	Bit mapped register	Decimal 0-255	Hex 6A
S15	Bit mapped register		N/A
S16	Test register	Decimal #	000

[1]Valid for AA pin tied low.

DIP SWITCH FUNCTIONS SUPPORTED
(DIP switches are only read on power-up.)

PIN	FUNCTION	SETTINGS (Suggested default underlined)
$\overline{\text{FDTR}}$	Force DTR on	Tie high or float: DTR signal controls modem
		Tie low: DTR always on
STL	Operate with switched telephone lines	Tie high or float: Switched telephone lines
		Tie low: Leased lines
$\overline{\text{FDCD}}$	Force DCD on	Tie high or float: RS-232 DCD line toggles
		Tie low: DCD line always on

TABLE 3: Speaker Modes

Mn	SPEAKER MODE
M0	Speaker off
M1	Speaker on during connect only
M2	Speaker on always

TABLE 4: O Modes

On	ONLINE/RETRAIN MODE
O0	Return online
O1	Return online
O2	Return online with remote digital loopback enabled

TABLE 5: ID Codes

In	CODE
I 0	Product code (139)
I 1	ROM checksum
I 2	Checksum test
I 3	Product revision
I 4	Software copyright

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

TA = 0°C to 70°C, VDD = 5V ± 10%, unless otherwise noted.

PARAMETER	RATING	UNIT
VDD Supply Voltage	7	V
Storage Temperature	-65 to 150	°C
Soldering Temperature (10 sec.)	260	°C
Applied Voltage	-0.3 to VDD +0.3	V

NOTE: All inputs and outputs are protected from static charge using built-in, industry standard protection devices and all outputs are short-circuit protected.

RECOMMENDED OPERATING CONDITIONS

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNIT
VDD, Supply Voltage		4.5	5	5.5	V
TA, Operating Free-Air Temperature		0		70	°C
External Component [3]					
VREF Bypass Capacitor [2]	(External to GND)	0.1			µF
Bias Setting Resistor [1]	(Placed between VDD and ISET pins)	1.8	2	2.2	MΩ
ISET Bypass Capacitor [2]	ISET pin to GND	0.1			µF
VDD Bypass Capacitor [2]	(External to GND)	0.1			µF
Input Clock Variation	(11.0592 MHz)	-0.01		+0.01	%

Note 1: Optional for minimum worst case current consumption.

Note 2: Minimum for optimized system layout; may require higher values for noisy environments.

Note 3: Refer to application drawing for placement.

DC CHARACTERISTICS
TA = 0°C to +70°C, VDD = 5V ± 10%, unless otherwise noted.

PARAMETERS		CONDITIONS	MIN	NOM	MAX	UNIT
IDD, Supply Current						
73K222U IDDA, Active		ISET Resistor = 2 MΩ		8	12	mA
73K222U IDDA, Active		ISET = GND		8	15	mA
73K222U IDD1, Power-Down		CLK = 11.0592 MHz		3	4	mA
73K222U IDD2, Power-Down		CLK = 19.200 KHz		2	3	mA
73D620L IDDA, Active			11	15	19	mA
Digital Inputs						
Input High Current	IIH	VI = VDD			100	µA
Input Low Current	IIL	VI = 0	-200			µA
Input Low Voltage	VIL				0.8	V
Input High Voltage	VIH	Except RESET & XTAL 1	2.0			V
Input High Voltage	VIH	RESET & XTAL 1	3.0			V
Pull Down Current		RESET pin	5		30	µA
Input Capacitance					10	pF
Digital Outputs						
Output High Voltage	VOH	IOUT = - 1 mA	2.4		VDD	V
VOL UD0-UD7 and INTRPT		IOUT = 3.2 mA			.4	V
VOL other outputs		IOUT = 1.6 mA			.4	V
CLK Output	VOL	IOUT = 3.2 mA			0.6	V
OH Output	VOL	IOUT = 20 mA			1.0	V
OH Output	VOL	IOUT = 10 mA			0.5	V
Offstate Current INTRPT pin		VO = 0V	-20		20	µA
Analog Pins						
RXA Input Resistance				200		KΩ
RXA Input Capacitance					25	pF

DYNAMIC CHARACTERISTICS AND TIMING
TA = 0°C to +70°C, VDD = 5V ± 10%, unless otherwise noted.

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNIT
DPSK Modulator					
Carrier Suppression	Measured at TXA	55			dB
Output Amplitude	ANS TONE 2225 or 2100 Hz	-11	-10.0	-9	dBm0[1]
	DPSK TX Scrambled Marks	-11	-10.0	-9	dBm0
	FSK Dotting Pattern	-11	-10.0	-9	dBm0
FSK Tone Error	Bell 103 or V.21			±5	Hz
DTMF Generator					
Freq. Accuracy		-.25		.25	%
Output Amplitude	Low Band	-10	-9	-8	dBm0
Output Amplitude	High Band	-8	-7	-6	dBm0
Long Loop Detect	DPSK or FSK	-40		-32	dBm0
Demodulator Dynamic Range	DPSK or FSK		45		dB
Call Progress Detector					
Detect Level	2-Tones in 350-600Hz Band	-39		0	dBm0
Reject Level	2-Tones in 350-600Hz Band			-46	dBm0
Delay Time	-70dBm0 to -30dBm0 Step	27		80	ms
Hold Time	-30dBm0 to -70dBm0 Step	27		80	ms
Hysteresis		2			dB
Carrier Detect	DPSK or FSK Receive				
Threshold	Data	-49		-42	dBm0
Delay Time	-70 dBm0 to -30 dBm0 Step	15		45	ms
Hysteresis		2	3.0		dB
Hold Time	-30 dBm0 to -70 dBm0 Step	10		24	ms

Note 1: All units in dBm0 are measured at the line input to the transformer. The interface circuit inserts an 8dB loss in the transmit path (TXA1 - TXA2 to line), and a 3dB loss in the receive path (line to RXA).

DYNAMIC CHARACTERISTICS AND TIMING (Continued)

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNIT
Answer Tone Detector					
Detect Level Threshold	In FSK mode	-49.5		-42	dBm0
Delay Time	-70dBm0 to -30dBm0 STEP	20		45	ms
Hold Time	-30dBm0 to -70dBm0 STEP	10		30	ms
Detect Frequency Range		-2.5		+2.5	%
Hybrid Loading					
R1	See Figure 1		600		Ω
R2	Nominal telephone line load		600		Ω
C	TXA Hybrid Loading	.02		.033	µF
Speaker Output					
Gain Error		-1		+1	dB
Output Swing SPKR	10K||50pF LOAD 5% THD	2.75			VPP
Carrier VCO					
Capture Range	Originate or Answer	-10		10	Hz
Capture Time	-10Hz to +10Hz Carrier Frequency change assumed		40	100	ms
Recovered Clock					
Capture Range	% of Center Frequency	-625		+625	ppm
Data Delay Time	Analog data in at RXA pin to receive data valid at RXD pin.		30	50	ms
Guard Tone Generator					
Tone Accuracy	550 or 1800Hz	-20		+20	Hz
Tone Level	550 Hz	-4.0	-3.0	-2.0	dB
(Below DPSK Output)	1800 Hz	-7.0	-6.0	-5.0	dB
Harmonic Distortion	700 to 2900 Hz			-60	dB
Capacitance					
Inputs	All digital inputs			10	pF
XTAL1, XTAL2 load capacitors	Per crystal manufacturer's recommendations		30		pF
CLK	Maximum capacitive load			15	pF

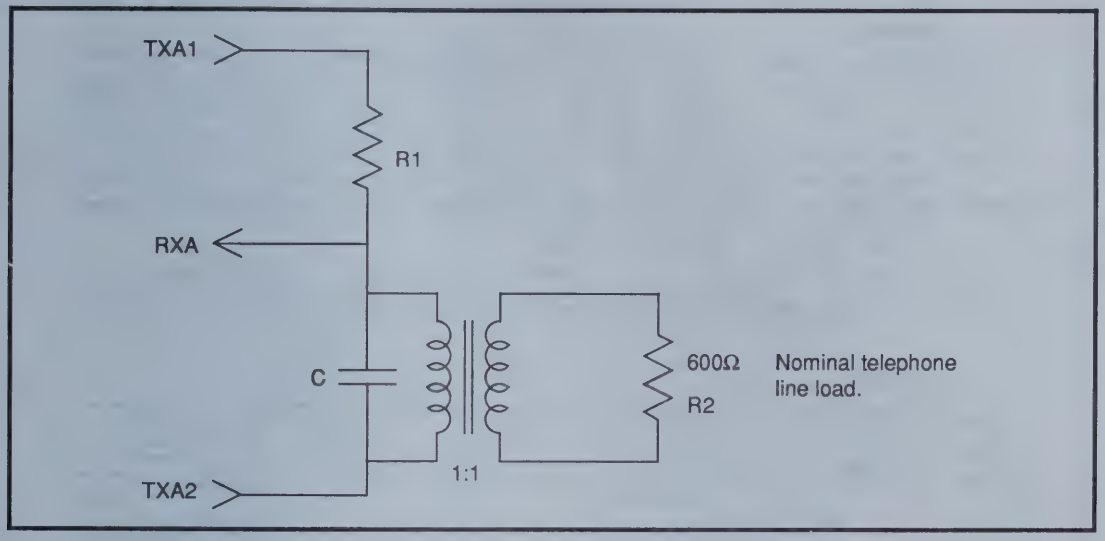


FIGURE 1: TXA Hybrid Loading Analog Interface Hybrid Loading

SERIAL BUS INTERFACE (See Figure 2)
The following times are for CL = 100pF.

PARAMETER		MIN	NOM	MAX	UNIT
TRD	Data out from Read	0		140	ns
TCKD	Data out after Clock			200	ns
TRDF	Data Float after Read	0		200	ns
TRCK	Clock High after Read	200			ns
TWW	Write Width	140		25000	ns
TDCK	Data Setup Before Clock	150			ns
TCKD	Data Hold after Clock	20			ns
TCKW	Write after Clock	150			ns
TACR	Address setup before Control[1]	50			ns
TCAR	Address Hold after Control [1]	50			ns
TACW	Address setup before Write	50			ns
TCAW	Address Hold after Write	50			ns

Note 1: Control is later of falling edge of RD or DCLK.

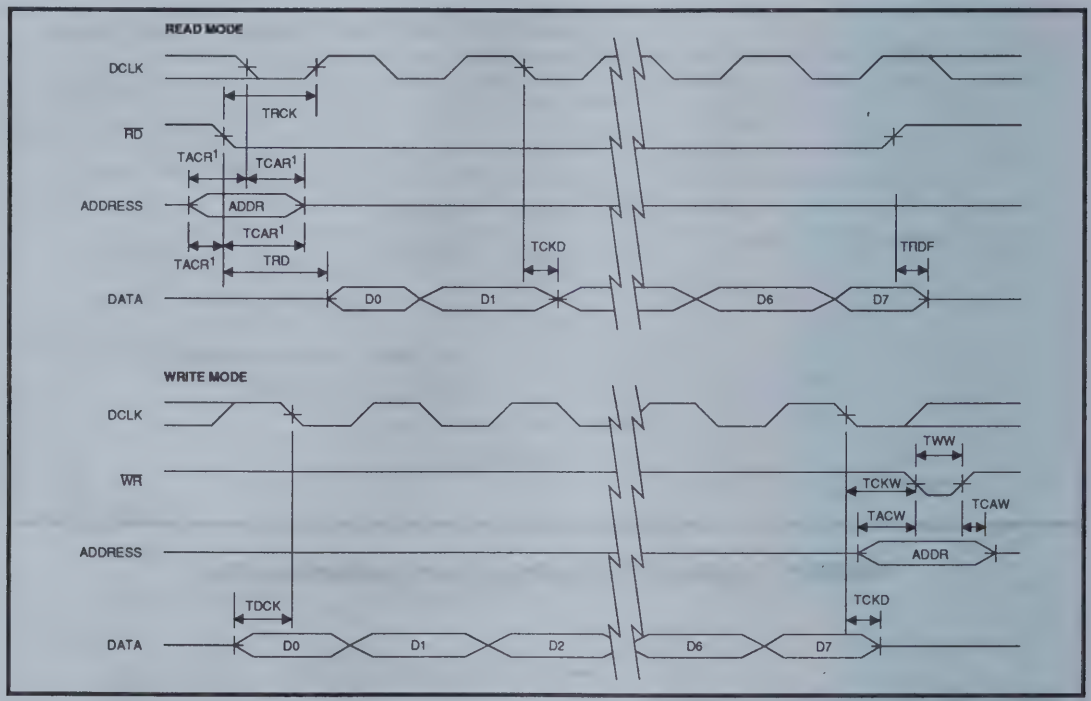


FIGURE 2: Modem Serial Bus Timing

PARALLEL BUS INTERFACE (See Figure 3) The following times are for Cl = 100pF.

PARAMETER		MIN	MAX	UNIT
RC	Read Cycle = TAD + TRC	240		ns
TDIW	DISTR Width	80		ns
TDDD	Delay DISTR to Data (read time)		80	ns
THZ	DISTR to Floating Data Delay	0	50	ns
TRA	Address Hold after DISTR	20		ns
TRCS	Chip select hold after DISTR	20		ns
TAR	DISTR Delay after Address	20		ns
TCSR	DISTR Delay after Chip Select	20		ns
WC	Write Cycle = TAW + TDOW + TWC	140		ns
TDOW	DOSTR Width	80		ns
TDS	Data Setup	30		ns
TDH	Data Hold	20		ns

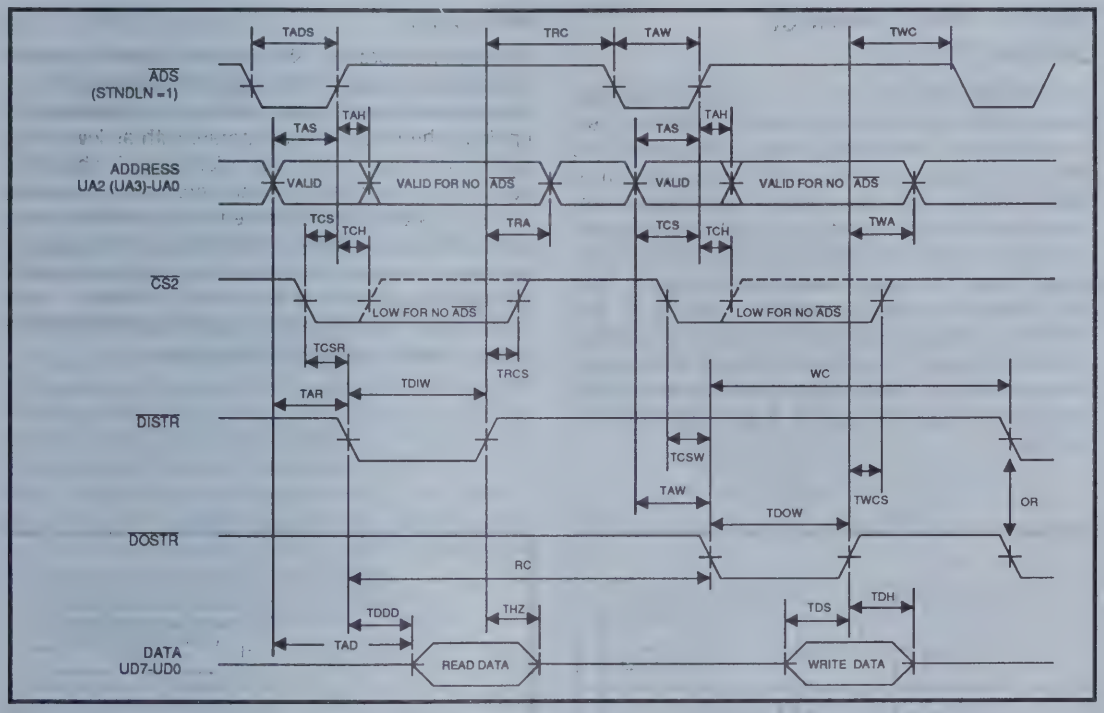


FIGURE 3: UART Bus Timing

PARALLEL BUS INTERFACE (Continued)

PARAMETER		MIN	MAX	UNIT
TWA	Address Hold after DOSTR	20		ns
TWCS	Chip select hold after DOSTR	20		ns
TAW	DOSTR delay after Address	20		ns
TCSW	DOSTR delay after Chip Select	20		ns
TADS	Address Strobe Width			ns
TAS	Address Setup Time			ns
TAH	Address Hold Time			ns
TCS	Chip Select Setup Time			ns
TCH	Chip Select Hold Time			ns
TRC	Read Cycle Delay	40		ns
TWC	Write Cycle Delay	40		ns
TAD	Address to Read Data	200		ns

TYPICAL PERFORMANCE CHARACTERISTICS

The SSI 73K222U was designed using an integrated analog/digital architecture that offers optimum performance over a wide range of line conditions. The SSI 73K222U utilizes the circuit design proven in SSI's 73K222L one-chip modem, with added enhancements which extend low signal level performance and increase immunity to spurious noise typically encountered in integral bus applications. The SSI 73K222U provides excellent immunity to the types of disturbances present with usage of the dial-up telephone network. The following curves show representative Bit Error Rate performance under various line conditions. (See Figures 4, 5 and 6 Performance Curves)

BER vs S/N

This test measures the ability of the modem to function with minimum errors when operating over noisy lines. Since some noise is generated by even the best dial-up lines, the modem must operate with as low a S/N ratio as possible. Optimum performance is shown by curves that are closest to the zero axis. A narrow spread between curves for the four line conditions indicates minimal variation in performance when operating over a range of line qualities and is typical of high performance adaptive equalization receivers. High band receive data is typically better than low band due to the inherent design of PSK modems.

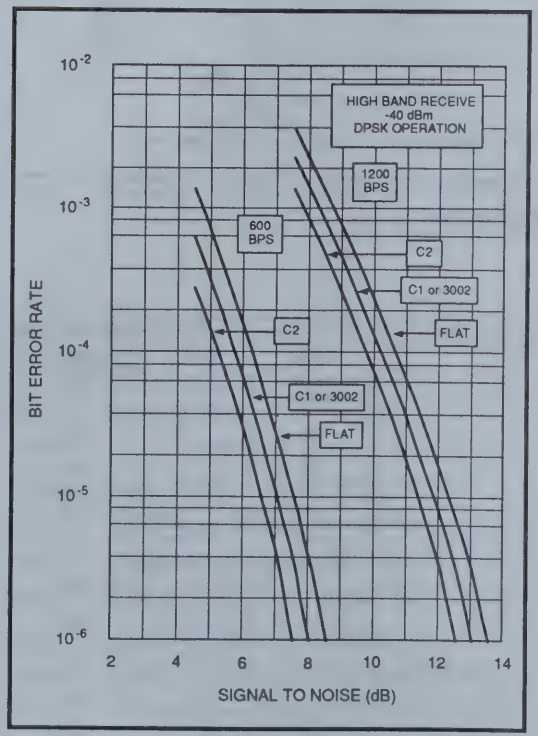


FIGURE 4: SSI 73K222U Typical BER vs. S/N

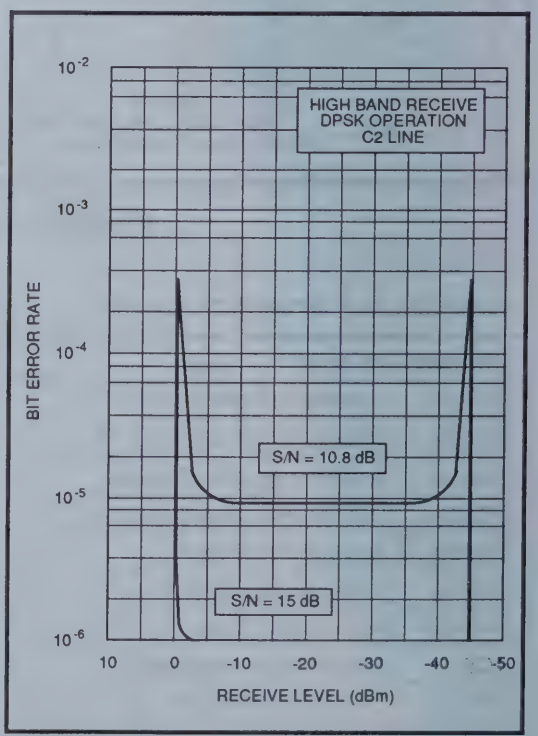


FIGURE 5: SSI 73K222U Typical BER vs. Receive Level

BER vs Receive Level

This measures the dynamic range of the modem. As signal levels vary widely over dial-up lines, the widest dynamic range possible is desirable. The minimum Bell specification calls for 36dB of dynamic range. S/N ratios were held constant at the indicated values while receive level was lowered from very high to very low signal levels. The "width of the bowl" of these curves taken at the 10^{-3} BER point is a measure of the dynamic range.

BER vs Carrier Offset

This parameter indicates how the modem performance is impacted by frequency shifts encountered in normal PSTN operation. Flat curves show no performance degradation from frequency offsets. The SSI K-Series devices use a 2nd order carrier tracking phase-locked-loop, which is insensitive to carrier offsets in excess of 10Hz. The Bell network specifications allow as much as 7Hz offset, and the CCITT specifications require modems to operate with 7Hz of offset.

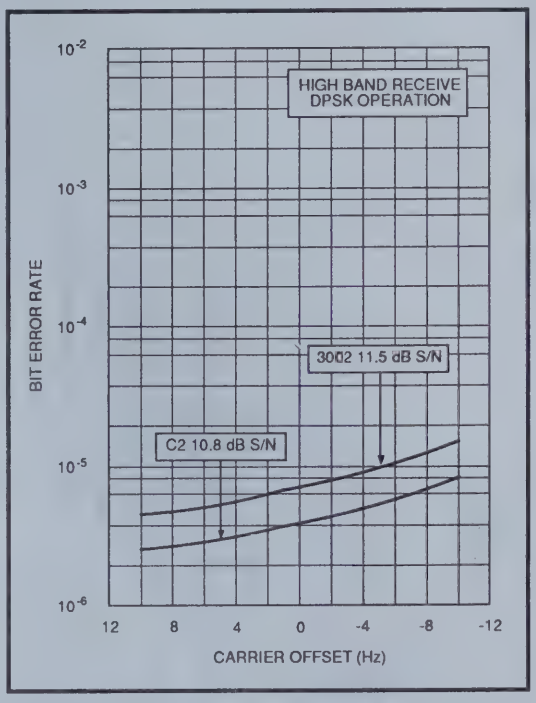


FIGURE 6: SSI 73K222U Typical BER vs. Carrier Offset

APPLICATIONS INFORMATION

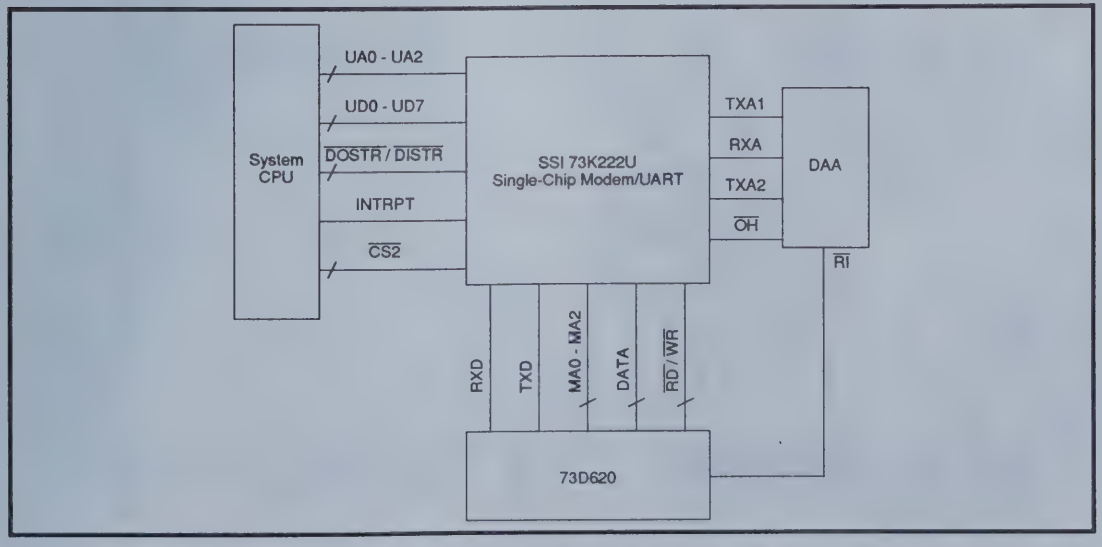


FIGURE 7: Typical Block Diagram for an Internal Modem Utilizing the SSI 73D2180 Chip-Set

APPLICATIONS INFORMATION (Continued)

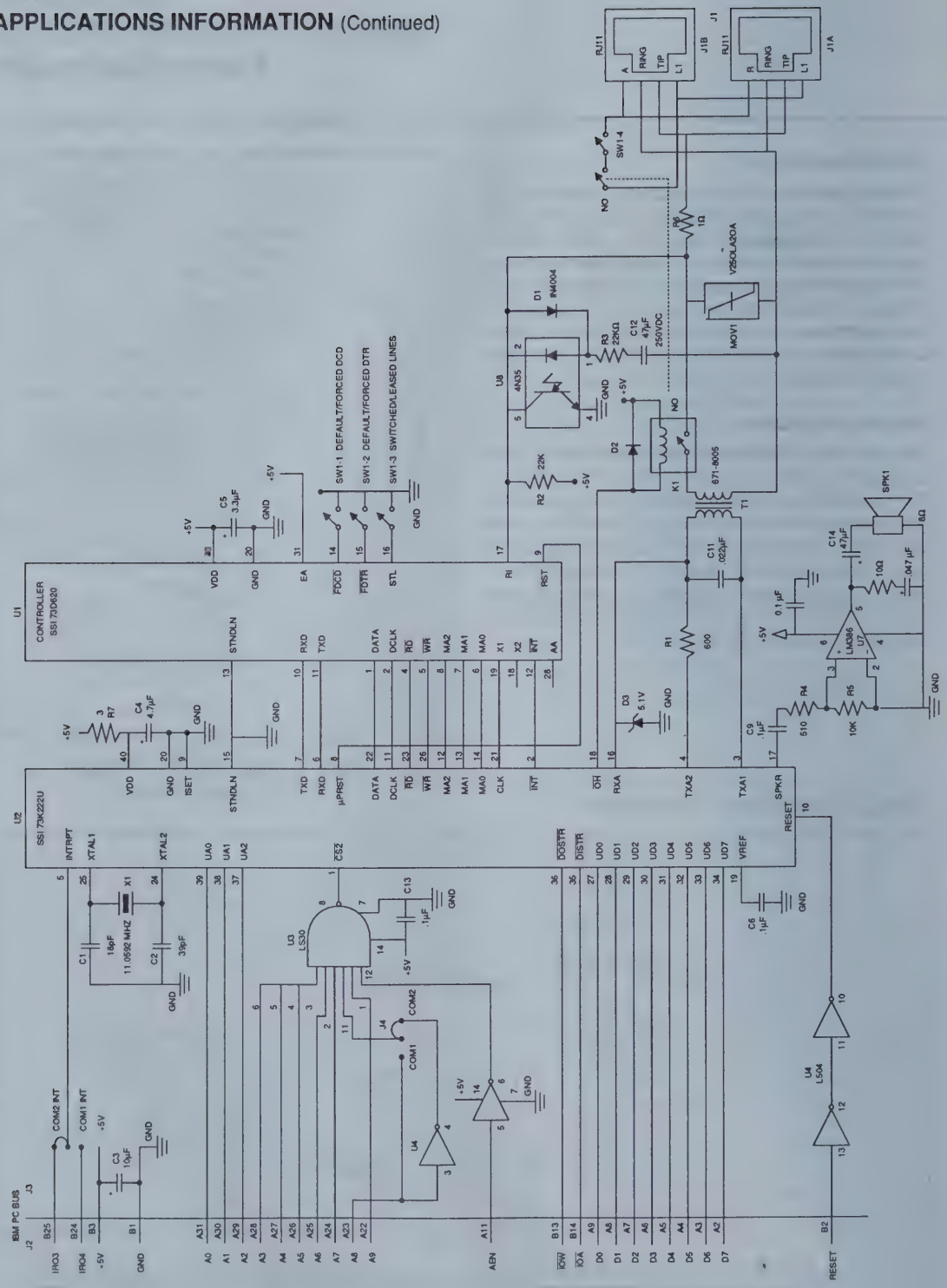
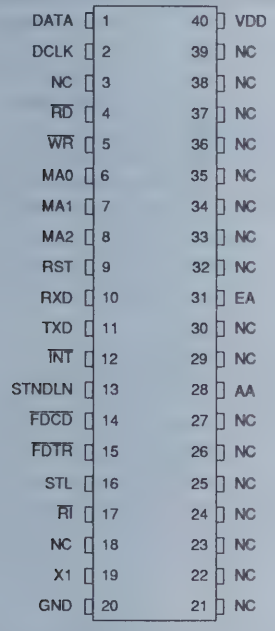
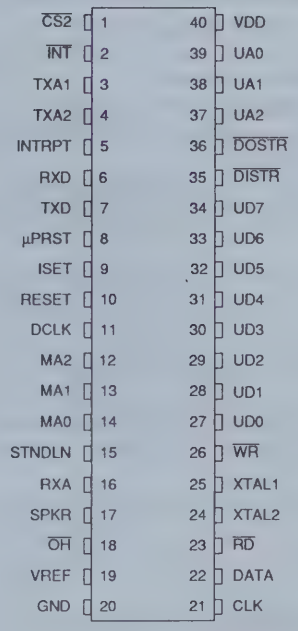


FIGURE 8: Typical Internal Modem Schematic Utilizing the SSI 73D2180 Chip-Set

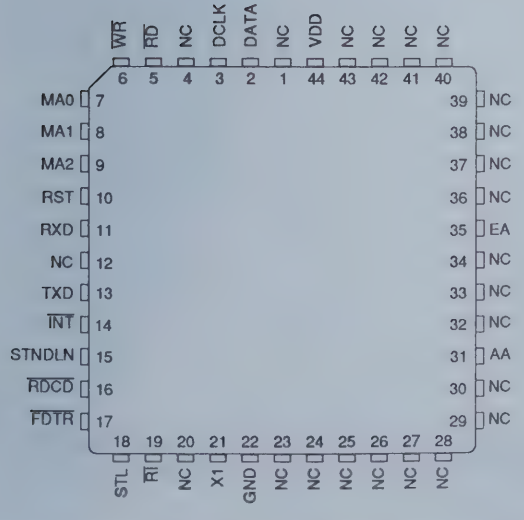
PACKAGE PIN DESIGNATIONS


DATA 1 40 VDD
DCLK 2 39 NC
NC 3 38 NC
RD 4 37 NC
WR 5 36 NC
MA0 6 35 NC
MA1 7 34 NC
MA2 8 33 NC
RST 9 32 NC
RXD 10 31 EA
TXD 11 30 NC
INT 12 29 NC
STNDLN 13 28 AA
FDCD 14 27 NC
FDTR 15 26 NC
STL 16 25 NC
RI 17 24 NC
NC 18 23 NC
X1 19 22 NC
GND 20 21 NC

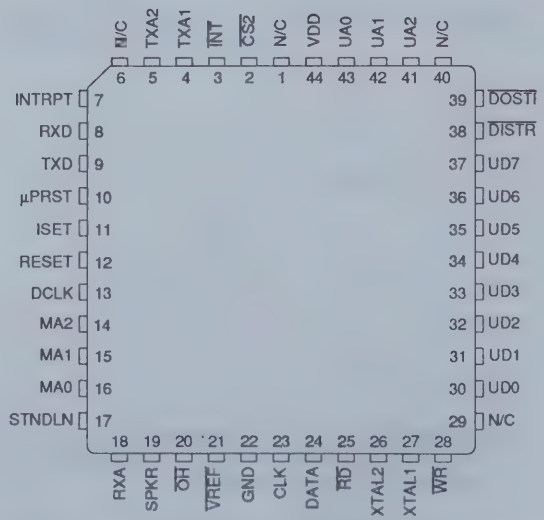
SSI 73D620 40-pin DIP


CS2 1 40 VDD
INT 2 39 UA0
TXA1 3 38 UA1
TXA2 4 37 UA2
INTRPT 5 36 DOSTR
RXD 6 35 DISTR
TXD 7 34 UD7
µPRST 8 33 UD6
ISET 9 32 UD5
RESET 10 31 UD4
DCLK 11 30 UD3
MA2 12 29 UD2
MA1 13 28 UD1
MA0 14 27 UD0
STNDLN 15 26 WR
RXA 16 25 XTAL1
SPKR 17 24 XTAL2
OH 18 23 RD
VREF 19 22 DATA
GND 20 21 CLK

SSI 73K222U 40-pin DIP



SSI 73D620 44-pin PLCC



SSI 73K222U 44-pin PLCC

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 73D2180 Chip-set Two 40-pin DIP packages	SSI 73D2180L-CP	73K222U-IP 73D620L-CP
SSI 73D2180 Chip-set Two 44-pin PLCC packages	SSI 73D2180L-CH	73K222U-IH 73D620L-CH

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silicon systems®

SSI 73D2240
V.22bis 2400 Bit/s Intelligent Modem Device Set

Advance Information

July, 1989

2

DESCRIPTION

The SSI 73D2240 is a set of two IC's that provide the data pump functions needed to design a high-performance, low-power 2400 bit/s intelligent modem for use in dial-up telephone network applications. The 73D2240 consists of the SSI 73K224L 1-chip multi-mode modem along with the SSI 73D600, a companion supervisory controller that provides a complete "AT" command and feature set compatible with industry standard products.

The 73D2240 includes operating modes compatible with CCITT V.22bis, V.22, and V.21, as well as Bell 212A and 103 data communications standards. Using advanced CMOS processes that integrate analog, digital signal processing and switched capacitor filter functions on the same chip, the SSI 73D2240 offers excellent performance, full modem features and the lowest power consumption available in a compact 2-chip set.

The 73D2240 can be used in free standing and integral modem designs where full-duplex 2400 bit/s operation is required. Single 5V supply operation with extremely low power draw make it ideal for battery powered terminals, lap-top P.C.'s and other power sensitive applications.

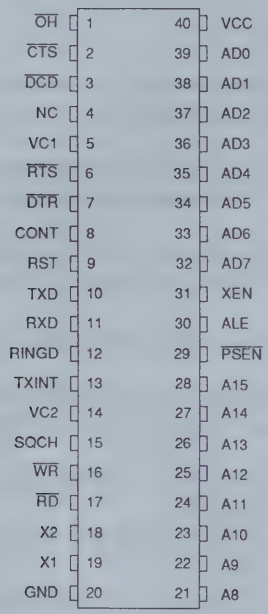
FEATURES

- **Multi-mode V.22bis/V.22/V.21 and Bell 212A/103 compatible device set for intelligent modem designs**
- **Full duplex operation at 0-300, 600, 1200 and 2400 bit/s with both synchronous and asychronous modes**
- **Includes industry standard "AT" commands and features compatible with existing 2400 bit/s modem products**
- **Automatic speed detect and terminal autobaud functions**
- **Supports external non-volatile RAM for storage of 2 separate set-up configurations and "N" number dialing**
- **Intelligent dialing functions including adaptive pulse or DTMF dialing**
- **Low power operation (<200 mW @ 5V) from single +5V supply**
- **Power down capability for very low quiesent power**
- **Adaptive equalization for optimum performance over all lines**
- **Full test modes, including self-test capability**
- **Compact 40/28-pin DIP or 44/32-pin PLCC packages for surface mount designs**

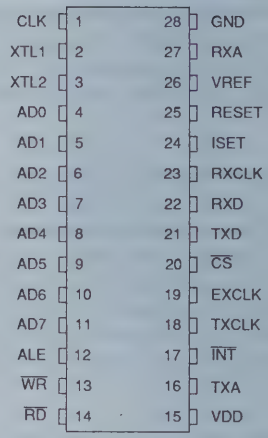
SSI 73D2240
V.22bis 2400 Bit/s
Intelligent Modem Device Set

PACKAGE PIN DESIGNATIONS
(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.



SSI 73D600 40-pin DIP



SSI 73K224L 28-pin DIP

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SSI 73K224L Protected by the following Patents (4,777,453) (4,789,995)

SSI 73D2404
V.22 bis 2400 Bit/s Modem Device Set

July, 1989

DESCRIPTION

The SSI 73D2404 consists of three CMOS integrated circuits which together provide the data pump functions required to construct a high performance 2400 bit/s full-duplex intelligent modem for use over the dial-up telephone network. The 73D2404 includes operating modes compatible with CCITT V.22 bis, V.22, V.21, as well as Bell 212A and 103 data-communications standards. Using advanced CMOS processes that include analog, digital signal processing and switched capacitor filter techniques, the SSI 73D2404 offers excellent performance and a high level of functional integration in a compact three-chip set which includes one 40-pin and two 28-pin dual-in-line packages.

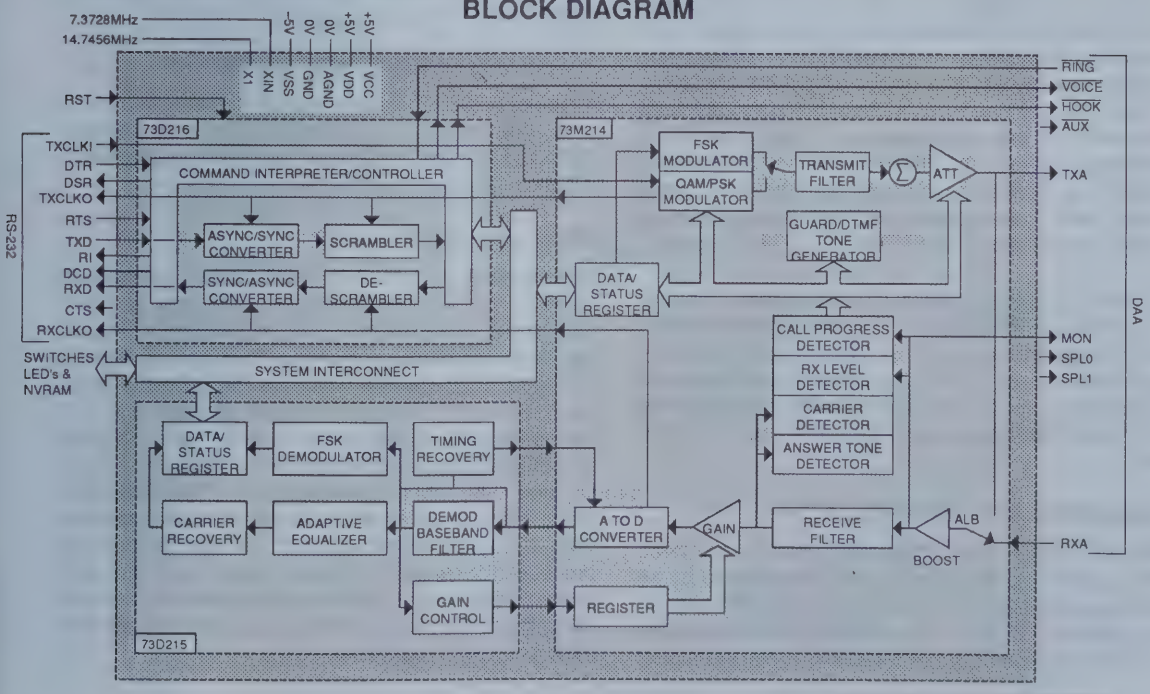
The 73D2404 is ideal for use in both free-standing or integral system modem products where full-duplex 2400 bit/s data-communications over the 2-wire public service telephone network is desired.

FEATURES

- **Multi-mode V.22 bis/V.22/V.21 & Bell 212A/103 compatible device set for intelligent modem designs**
- **Full duplex operation at 0-300, 1200 and 2400bps with all operating modes both synch & asynch**
- **Includes high-level "AT" command interpreter compatible with 2400 bit/s industry standard products**
- **Complete complement of "AT" modem features**
- **Selectable automatic speed detect, handshake and autobaud functions**
- **Supports external non-volatile memory to store user configurations**
- **Adaptive equalization for optimum performance over all lines**
- **Dynamic range from 0 to -45dBm**
- **Call progress, carrier and answer tone detectors provide intelligent dialing functions**

(Continued)

BLOCK DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

FEATURES (Continued)

- **DTMF and CCITT guard tone generators**
- **Test modes available - ALB, DL, RDL for complete test capability**
- **Space efficient 28 and 40-pin DIPs**
- **All CMOS technology for low power consumption (< 600mW using +/-5V)**

OPERATION

The SSI 73D2404 is a complete V.22 bis intelligent modem contained in three CMOS IC's. The device set forms the basis for a high performance stand-alone modem product with self-contained command interpreter, indicator LED's, default switches and interface lines for an RS-232 serial port. Both data and commands are passed over the serial port as in conventional intelligent modem designs.

The SSI 73D2404 provides the QAM, PSK and FSK modulator/demodulator functions, call progress and handshake tone monitors, test modes and a tone generator capable of producing DTMF, answer and CCITT guard tones. This device supports the V.22 bis, V.22, V.21 and Bell 212A/103 operating modes, both synchronous and asynchronous. The 73D2404 is designed to provide functions needed for an intelligent modem and includes auto-dial/auto-answer, handshake with auto-fallback, and selectable pulse or DTMF dialing sequences to simplify these designs.

The SSI 73D2404 consists of three devices. The SSI 73M214 is an analog processor that performs the filtering, timing adjustment, level detection and modulation functions. The 73D215 is the receiver digital signal processor. The 73D216 is a command processor that provides supervisory control and command interpretation.

QAM MODULATOR/DEMODULATOR

The SSI 73D2404 scrambles and encodes the 2400 bit/s incoming data into quad bits represented by 16 possible signal points as specified by CCITT recommendation V.22 bis. The modulator transmits this encoded data using either a 1200 Hz (originate mode) or 2400 Hz (answer mode) carrier. The demodulator reverses this procedure and recovers a data clock from the incoming signal. Adaptive equalization corrects for different line conditions by automatically changing filter parameters to compensate for line characteristics.

PSK MODULATOR/DEMODULATOR

In PSK mode the 73D2404 modulates the 1200 bit/s incoming data using a subset of the QAM signal points as specified by CCITT recommendation V.22 bis, V.22 and Bell 212A. The PSK demodulator is similar to the QAM demodulator.

FSK MODULATOR/DEMODULATOR

The FSK transmitter frequency modulates the analog output signal using two discrete frequencies to represent the binary data. The Bell 103 standard frequencies of 1270 and 1070 Hz (originate mark and space) and 2225 and 2025 Hz (answer mark and space) or the V.21 standard frequencies of 980 and 1180 Hz (originate mark and space) and 1650 and 1850 Hz (answer mark and space) are used when this mode is selected. Demodulation involves detecting the received frequencies and decoding them into the appropriate binary value.

PASSBAND FILTERS AND EQUALIZERS

A bandsplit filter is included to shape the amplitude and phase response of the transmit signal to a square root 75% raised cosine and provide rejection of out-of-band signals in the receive channel.

ASYNCHRONOUS MODES

The asynchronous mode is used for communication between asynchronous terminals which may vary the data rate from +1.5% to -1.5%. When transmitting in this mode the serial data on the TXD input is passed through a rate converter which inserts or deletes stop bits in the serial bit stream in order to output a signal whose data rate is accurate to 0.01%. The signal is routed to a data scrambler (following the CCITT V.22 bis algorithm) and into the modulator. The 73D2404 recognizes a break signal and handles it in accordance with BELL 212A specifications. Received data is processed in a similar fashion except that the rate converter now acts to reinsert any deleted stop bits. An incoming break signal will be passed through without incorrectly inserting a stop bit.

SYNCHRONOUS MODES

Synchronous operation is possible only with the QAM or PSK mode. Operation is similar to that of the asynchronous mode except that data must be synchronized to a provided clock and no variation in data transfer rate is allowable. Serial input data appearing at TXD must be valid on the falling edge of TXCLK. Receive data at the RXD output is clocked out on the rising edge of RXCLK. The async/synch converter is bypassed when synchronous mode is selected and data is transmitted out at the same rate as is input.

AUTOMATIC HANDSHAKE

The SSI 73D2404 will automatically perform a complete handshake as defined by the V.22 bis, V.22 and Bell 212A/103 standards to connect with a remote modem. The 73D2404 automatically determines the speed and operating mode and adjusts its operation to correspond to that of an answering modem when originating a call.

TEST MODES

The SSI 73D2404 allows use of Analog Loopback, Digital Loopback and Remote Digital Loopback test modes. Full test mode capability allows testing of the modem and interface functions from the local terminal using the appropriate control commands, or remotely using the RDL function.

ADAPTIVE EQUALIZATION WITH AUTO-RETRAIN

The SSI 73D2404 uses adaptive equalization which automatically compensates for varying line characteristics by adjusting taps on a multi-tap FIR filter. Optimum performance is obtained with this technique over a wide range of line conditions. When the line quality deteriorates to a specified level the 73D2404 can automatically initiate a retrain of the equalizer to re-establish data communications without the need to go through a complete handshake sequence.

"AT" COMMAND INTERPRETER

The SSI 73D2404 includes an AT command interpreter which is compatible with the Hayes 2400 Smartmodem™ command set. Functions and features included with intelligent modems are provided by the 73D2404 command interpreter.

NON-VOLATILE MEMORY

The SSI 73D2404 supports connection to an external non-volatile memory (ie. Xicor X2444) to store a dial string and the current AT command configuration.

SPEED/PROTOCOL COMPATIBILITY GUIDE

Calling a:			73D2404 originating as:				
			Bell		CCITT		
			300	1200	300	1200	2400
Bell	300	(103)	300	300	-	-	300
	1200	(212)	300	1200	-	1200	1200
	2400[1]	(224)	300	1200	-	1200	2400
CCITT	300	(V.21)	-	-	300	-	-
	1200	(V.22)	300	1200	-	1200	1200
	2400	(V.22 bis)	300	1200	-	1200	2400

Called from a:			73D2404 answering as:				
			Bell		CCITT		
			300	1200	300	1200	2400
Bell	300	(103)	300	300	-	-	300
	1200	(212)	300	1200	-	1200	1200
	2400	(224)	300	1200	-	1200	2400
CCITT	300	(V.21)	-	-	300	-	-
	1200	(V.22)	300	1200	-	1200	1200
	2400	(V.22 bis)	300	1200	-	1200	2400

[1] A Bell 2400 is a V.22 bis using a 2225 Hz answer tone without unscrambled marks.

HARDWARE INTERFACE

POWER SUPPLIES AND CLOCKS

I/O	LABEL	PIN CONNECTION			DESCRIPTION
		73M214	73D215	73D216	
I	VDD			40	Positive supply (analog +5V)
I	VCC	28	28		Positive supply (digital +5V)
I	VSS	14			Negative supply (analog -5V)
I	AGND	26			Analog ground
I	GND	15	14	20	Digital ground
I	X1			19	Clock input 14.7456 MHz
I	XIN	18			Clock input 7.3728 MHz
I	RST			9	Reset (10 µF & 8.2k)

DAA INTERFACE

I	RxA	27			Receive analog from DAA
O	TxA	20			Transmit analog to DAA
O	MON	25			Audio monitor
O	SPL0			B.4*	Audio volume control
O	SPL1			B.5*	Audio volume control
I	RINGB			5	From ring indicator
O	HOOKB			6	Off hook relay control
O	AUXR			B.7*	Auxiliary relay control

RS-232/V.24 INTERFACE

O	RI			3	Ring indicator output
O	RATE			B.3*	Indicates high speed
I	TXD			10	Digital data from terminal
O	RXD			11	Digital receive data
O	DCD			2	Data carrier detect
O	DSR			4	Data set ready
I	EXCLK	22			External Tx sync clock input
O	RXCLK	24		8	Receive clock ouptut
O	TXCLK	23		15	Transmit clock output
O	CTS			B.6*	Clear to send
I	RTS			B.6*	Request to send
I	DTR			B.7*	Indicates DTE available

* Available with expanded I/O

HARDWARE INTERFACE (Continued)

LED DISPLAY

I/O	LABEL	PIN CONNECTION 73M214	73D215	73D216	DESCRIPTION
O	WRB	4	24	16	Write strobe (active low)
LED	TR	Performed externally			Data terminal ready
LED	SD			10	Transmit data
LED	RD			11	Receive data
LED	CD			2	Data carrier detect
LED	HS			B.3*	High speed indicator
LED	MR			B.2*	Modem ready/test in progress
LED	AA			B.1*	Auto answer indicator
LED	OH			B.0*	Off hook indicator

DEFAULT SWITCHES

O	IOENB			26	LED/switch enable (active low)
O	RDB	3	25	17	Read strobe (active low)
SW	SW2-1	Performed externally			Force DTR
SW	SW2-2			B.5*	Disable "AT" recognition ("Dumb" mode)
SW	SW2-3	Performed externally			Force DCD

NVRAM INTERFACE

O	NVRCE			14	NVRAM CE (active high)
I/O	TXD			10	NVRAM DI/DO
I	RXD			11	NVRAM SK

* Available with expanded I/O

HARDWARE INTERFACE (Continued)

I/O	LABEL	PIN CONNECTION 73M214	73D215	73D216	DESCRIPTION
DEVICE SET INTERCONNECT (Refer to Figure 7 & 8.)					
S	VPP		1		+5V
S	INT		17		+5V
S	EA			31	+5V
S	EXADCC	19			0V
S	DACKB		2		+5V
S	CLK	16	15		7.3728 MHz
S	RXINT		5	13	System interconnect
S	TXINTB	21		12	
S	RSTDPX		16	1	
S	FSK		4	7	
S	RDB	3	25	17	
S	WRB	4	24	16	
S	A15	2		28	
S	A8		27	21	
S	D0	5	6	39	
S	D1	6	7	38	
S	D2	7	8	37	
S	D3	8	9	36	
S	D4		10	35	
S	D5		11	34	
S	D6		12	33	
S	D7		13	32	
S	SIN	10	22		
S	SOUT	11	21		
S	SIRQ	9	23		
S	SCK	13	18		
S	SENB	12	19,20		

"AT" COMMANDS SUPPORTED
(Note: s=string; n=decimal, 0-255; x=boolean, 0/1=false/true)

COMMAND	OPTIONS	DEFAULT
A/	Repeats last command line	N/A
A	Answer	N/A
Bx	BELL/CCITT = 1/0 answer tone @1200 (N/A @2400)	1
Ds	Dial string specified by s	No string
Ex	Command echo, 0/1 = off/on	1
Hn	Hook status, 0/1 = on/off	N/A
In	ID code, 0/1/2/3/4 (see Table 8)	N/A
Kn	SSi test	N/A
Ln	Speaker volume, (0)1/2/3 = lo/med/hi	2
Mn	Speaker, 0/1/2/3 = control (see Table 3)	1
On	Online, 0/1/2/3 = on-line/retrain/no retrain (see Table 4)	N/A
P	Pulse dial	Pulse
Qx	Quiet result, 0/1 = 1-quiet	0
R	Reverse originate	N/A
Sn=n	Set S register (see Table 2)	N/A
Sn?	Return value in register n (see Table 2)	N/A
T	Touch tone dial	Pulse
Ux	User help screen, Sreg, dial string, data format	N/A
Vx	Verbose result, 0/1 = off/on	1
Xn	Result code, 0/1/2/3/4 (see Table 1)	4
Yx	Enable long space disconnect, 1 = enable	0
Z	Restore from Non-Volatile Memory	N/A
&Cx	Carrier detect override, 0/1 = on/normal	0
&Dn	DTR mode, 0/1/2/3 (see Table 5)	0
&F	Restore to factory configuration	N/A
&Gn	CCITT guard tone, 0/1/2 = off/1800/550	0
&Jx	Auxiliary relay control	0
&Mn	Async/Sync mode, 0/1/2/3 (see Table 6)	0

"AT" COMMANDS SUPPORTED (Continued)

COMMAND	OPTIONS	DEFAULT
&Rx	Enable RTS/CTS	0
&Sx	DSR override, 0/1=on/normal	0
&Tn	Test mode (see Table 7)	N/A
&Px	Pulse dial mode, 0/1=U.S./U.K.	0
&W	Write current configuration to NVRAM	N/A
&Xn	Sync Tx clock mode, 0/1/2=int/ext/slave	0
&Zs	Store a telephone number=string	N/A

Factory configuration[1]:
B1 E1 F1 L2 M1 P Q0 V1 X4 Y0 &C0 &D0 &G0 &J0 &M0 &P0 &R0 &S0 &T4 &X0

Dial string arguments:

, = delay	@ = silent answer	! = flash	
; = return to command	s = dial stored number	W = wait for tone	R=reverse mode

[1]If the NovRAM has not been initialized it may be necessary to Power down/Power up and type AT&F&W<cr> to properly initialize modem state.

TABLE 1: Result Codes

Xn	VOCAL/NUMERIC RESULT CODE
X0	OK/0, CONNECT/1, RING/2, NO CARRIER/3, ERROR/4
X1	All functions of X0 + CONNCET (RATE)/1 = 300, 5 = 1200, 10 = 2400
X2	All functions of X1 + NO DIAL TONE/6
X3	All functions of X1 + BUSY/7
X4	All functions of X3 + NO DIAL TONE/6

TABLE 2: S Registers Supported

NUMBER	FUNCTION	UNITS	DEFAULT
S0[1]	Answer on ring	No. of rings	000
S1	Ring counter	No. of rings up to 8	000
S2	Escape code	ASCII CHR$( )	043
S3	Carriage return	ASCII CHR$( )	013

[1]Stored in NVRAM with &W command

TABLE 2: S Registers Supported (Continued)

NUMBER	FUNCTION	UNITS	DEFAULT
S4	Line feed	ASCII CHR$( )	010
S5	Back space	ASCII CHR$( )	008
S6	Wait for dial tone	Seconds	002
S7	Wait for carrier	Seconds	030
S8	Pause time	Seconds	002
S9	Carrier valid	100 milliseconds	006
S10	Carrier drop out	100 milliseconds	014
S11	DTMF tone duration	1 millisecond	070
S12	Escape guard time	20 milliseconds	050
S13	Unused		N/A
*S14[1]	Bit mapped register	Decimal 0-255	170
S15	Unused		N/A
S16	Test register	Decimal #	000
S17	SSI Special test register	Decimal 0-255	096
S18	Test timer	Decimal 0-255	000
S19	Unused		N/A
S20	Unused		N/A
*S21[1]	Bit mapped register	Decimal 0-255	000
*S22[1]	Bit mapped register	Decimal 0-255	118
*S23[1]	Bit mapped register	Decimal 0-255	007
S24	Unused		N/A
S25[1]	DTR delay	10 milliseconds	005
S26[1]	CTS delay	10 milliseconds	001
*S27[1]	Bit mapped register	Decimal 0-255	064

*The bit mapped register functions are equivalent to normal "AT" command modem registers. They are not needed for evaluation of the 73D2404 capabilities.

Asynchronous character formats supported:
[Number of data bits, parity (even/odd/none), number of stop bits]

1200/2400 bit/s: 7N2, 7E1, 7O1, 8N1

300 bit/s: 7N2, 7E1, 7O1, 8N1, 8E1, 8O1

[1]Stored in NVRAM with &W command

TABLE 3: Speaker Modes

Mn	SPEAKER MODE
M0	Speaker off
M1	Speaker on during connect only
M2	Speaker on always
M3	Speaker on during call progress

TABLE 4: O Modes

On	ONLINE/RETRAIN MODE
O0	Return online
O1	Return online with retrain
O2	Enable automatic retrain (default)
O3	Disable automatic retrain

TABLE 5: DTR Modes

&Dn	DTR MODE
&D0	Ignore DTR
&D1	Go to command state if ON to OFF detected
&D2	Go to command state and disable auto-answer if ON to OFF detected
&D3	Initialize modem with NVRAM if ON to OFF detected

TABLE 6: Synchronous Modes

&Mn	SYNCHRONOUS MODE
&M0	Asynchronous
&M1	Sync mode entered upon completion of connect sequence
&M2	Dial stored number on OFF to ON transition of DTR and go online
&M3	Manual dial using DTR as talk data switch

TABLE 7: Test Modes

&Tn	TEST MODE
&T0	End/Abort test
&T1	Initiate local analog loopback (L3)
&T3	Initiate local digital loopback
&T4	Permit remote digital loopback (L2)
&T5	Prohibit remote digital loopback
&T6	Initiate remote digital loopback (L2)
&T7	Initiate RDL with self-test and error detector
&T8	Initiate ALB with self-test and error detector

TABLE 8: ID Codes

In	CODE
I 0	Product code (249)
I 1	ROM checksum
I 2	Checksum test
I 3	Product revision
I 4	Software copyright

DIP SWITCH FUNCTIONS SUPPORTED
(DIP switches are only read on power-up if NovRAM is not present.)

SWITCH	FUNCTION	SETTINGS (Suggested default underlined)
SW2-1	DTR override	off = DTR signal controls modem
		on = DTR always on
SW2-2	"AT" command set recognition	off = Normal operation
		on = "AT" command recognition disabled ("dumb" mode)
SW2-3	Carrier detect override	off = RS-232 CD line toggles (&C1)
		on = CD line always on (&C0)

RECOMMENDED OPERATING CONDITIONS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Ta, Ambient Temperature		0		70	°C
VCC & VDD, Supply Voltage	73M214, 73D215, 73D216	4.25		5.25	V
VSS, Supply Voltage	73M214	-5.25		-4.25	V
VDD, VSS Bypass Capacitors		10+0.1			µF
Input Low Voltage (VIL)		0		0.8	V
Input High Voltage (VIH)		2.0		VDD	V
Output Low Current				1.6	mA
Output High Current		0.4			mA
CLK Load Capacitance				25	pF
Digital Load Capacitance				50	pF
TxA, MON Loading				See Note	
Input Clock Rrequency (X1)			14.7456		MHz
Input Clock Variation (X1, XIN)	XIN must be X1 div. by 2	-0.01		0.01	%

Note: 10 KΩ in parallel with 50 pF

INPUT CLOCK TIMING (See Figure 1.)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
TCLCX		20			ns
TCLCX2		54		82	ns
TCHCX		20			ns
TCHCX2		54		82	ns
TR, TF				15	ns
TCHCH		0		20	ns

INTERFACE TIMING (This information is provided to assist in the connection of external circuitry to the data bus. Refer to application circuit in Figure 9.)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
LED Write Timing (See Figure 2.)						
TWLWH	WRB pulse width		307			ns
TAVWL	Address valid to WRB low		141			ns
TQVWH	Data valid to WRB high		370			ns
TQVWX	Data valid to WRB transition		27			ns
TWHDX	Data hold after WRB		86			ns
Switch Read Timing (See Figure 3.)						
TRLRH	RDB pulse width		307			ns
TAVRL	Address valid to RDB low		141			ns
TRLDV	RDB low to data valid				174	ns
TRHDX	Data hold after RDB		0			ns

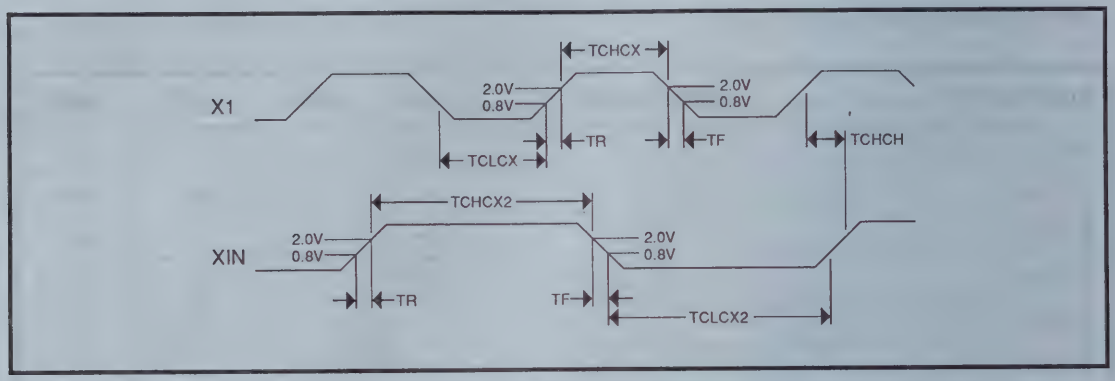


FIGURE 1: Input Clock Timing

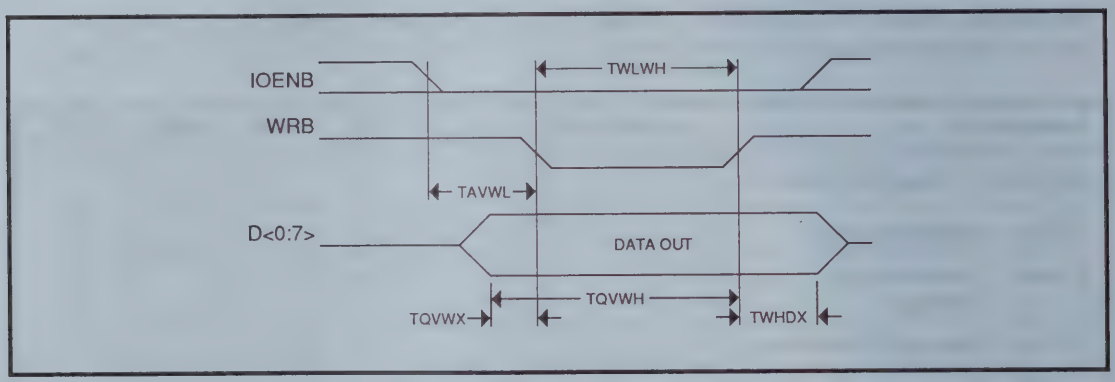


FIGURE 2: LED Write Timing

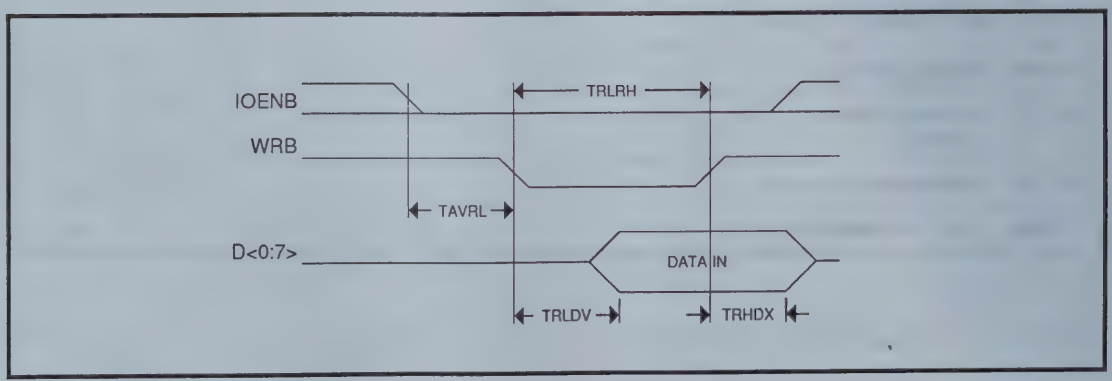


FIGURE 3: Switch Read Timing

DC ELECTRICAL CHARACTERISTICS

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
IDD	Supply Current				100	mA
ISS					35	mA
IIH	Input High Current				10	µA
IIL	Input Low Current	Except TxCLKI which has pullup of 20 kΩ	-10			µA
	Digital Input Capacitance				10	pF
VOH	Output High Voltage		2.4			V
VOL	Output Low Voltage				0.4	V
RXA	Input Resistance		100k			Ω
RXA	Input Capacitance				25	pF

TRANSMITTER SPECIFICATIONS

TRANSMITTER POWER

(All power measurements are measured at 73M214 TxA pin.)

TRANSMITTER POWER	CONDITIONS	MIN	NOM	MAX	UNITS
QAM/DPSK Transmitter Power	With or without CCITT tones	-9.8		-8.2	dBm
CCITT Guard Tone	550	-14.8		-12.8	dBm
	1800	-16.0		-14.0	dBm
FSK Transmitter Power	103/V.21	-10.0		-8.0	dBm
Answer Tone Power		-10.0		-8.0	dBm
DTMF Transmitter Power	Columns	-7.0		-5.0	dBm
	Rows	-9.0		-7.0	dBm
	Twist	-3.0		-1.0	dB

TRANSMITTER FREQUENCY
(All tones are digitally derived from the clock input and have the input clock frequency tolerance.)

TRANSMITTER FREQUENCY		CONDITIONS		MIN	NOM	MAX	UNITS
QAM/DPSK Carrier Frequencies		Originate			1200.0		Hz
		Answer			2400.0		Hz
FSK Tone Frequencies							
103	Originate	Space	1070		1066.7		Hz
		Mark	1270		1269.4		Hz
	Answer	Space	2025		2021.1		Hz
		Mark	2225		2226.1		Hz
V.21	Originate	Space	1180		1181.6		Hz
		Mark	980		978.3		Hz
	Answer	Space	1850		1850.0		Hz
		Mark	1650		1651.6		Hz
Special Tone Frequencies							
Answer Tone			2100		2104.1		Hz
CCITT Guard Tones			550		556.5		Hz
			1800		1786.0		Hz
DTMF Dialing Tone Frequencies							
Low Group		Columns	697		698.2		Hz
			770		771.9		Hz
			852		853.3		Hz
			941		942.3		Hz
High Group		Rows	1209		1209.5		Hz
			1336		1335.7		Hz
			1477		1476.9		Hz
			1663		1634.0		Hz

TRANSMITTER DISTORTION

TRANSMITTER DISTORTION	CONDITIONS	MIN	NOM	MAX	UNITS
QAM/DPSK Carrier Suppresion	Measured at TxA	35			dB
CCITT Guard Tone Distortion	800-1600 Hz band			-60	dB
	0-10 kHz band			-45	dB
Answer Tone Distortion	800-1600 Hz band			-60	dB
	0-10 kHz band			-40	dB
FSK Output Bias Distortion	Transmit dotting 300 bit/s	-6		6	%
FSK Opposite Band Distortion				-60	dB
DTMF Tone Distortion	700-2900 Hz band			-29	dB

RECEIVER SPECIFICATIONS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Carrier VCO					
Capture Range	Carrier offset	-10		10	Hz
Carrier Jitter	50-65 Hz			30	°C
Data Clock Recovery Capture Range	From system clock div. by 24576 (600 Hz symbol clock)	±250			ppm
Data Delay Time	RxA to RxD	30		75	ms
Retrain Request Threshold	If enabled	10-3		10-2	BER
Carrier Detect					
Threshold		-48		-43	dBm
Hysteresis		2			dB
Answer Tone Detect	2100/2225 Hz				
Threshold		-48		-43	dBm
Hysteresis		2			dB
Call Progress Detect	350-650 Hz dual tone				
Threshold		-40		-30	dBm
Hysteresis		2			dB

PERFORMANCE DATA

(This performance data was taken using an AEA tester and the 73D2404 MEU board.)

BER PERFORMANCE

(-20dBm receive level 10-5 BER)

PARAMETER	MINIMUM SNR REQUIRED
2400 bit/s Originate	16.5 dB SNR
2400 bit/s Answer	16.0 dB SNR
1200 bit/s Originate	9.0 dB SNR
1200 bit/s Answer	8.0 dB SNR
0-300 bit/s Originate	9.0 dB SNR
0-300 bit/s Answer	7.5 dB SNR

DYNAMIC RANGE

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
2400 bit/s Originate	10-5 BER @ 17dB SNR	-45		0	dBm
2400 bit/s Answer	10-5 BER @ 17dB SNR	-45		0	dBm
1200 bit/s Originate	10-5 BER @ 12dB SNR	-45		0	dBm
1200 bit/s Answer	10-5 BER @ 12dB SNR	-45		0	dBm
0-300 bit/s Originate	10-5 BER @ 12dB SNR	-45		0	dBm
0-300 bit/s Answer	10-5 BER @ 12dB SNR	-45		0	dBm

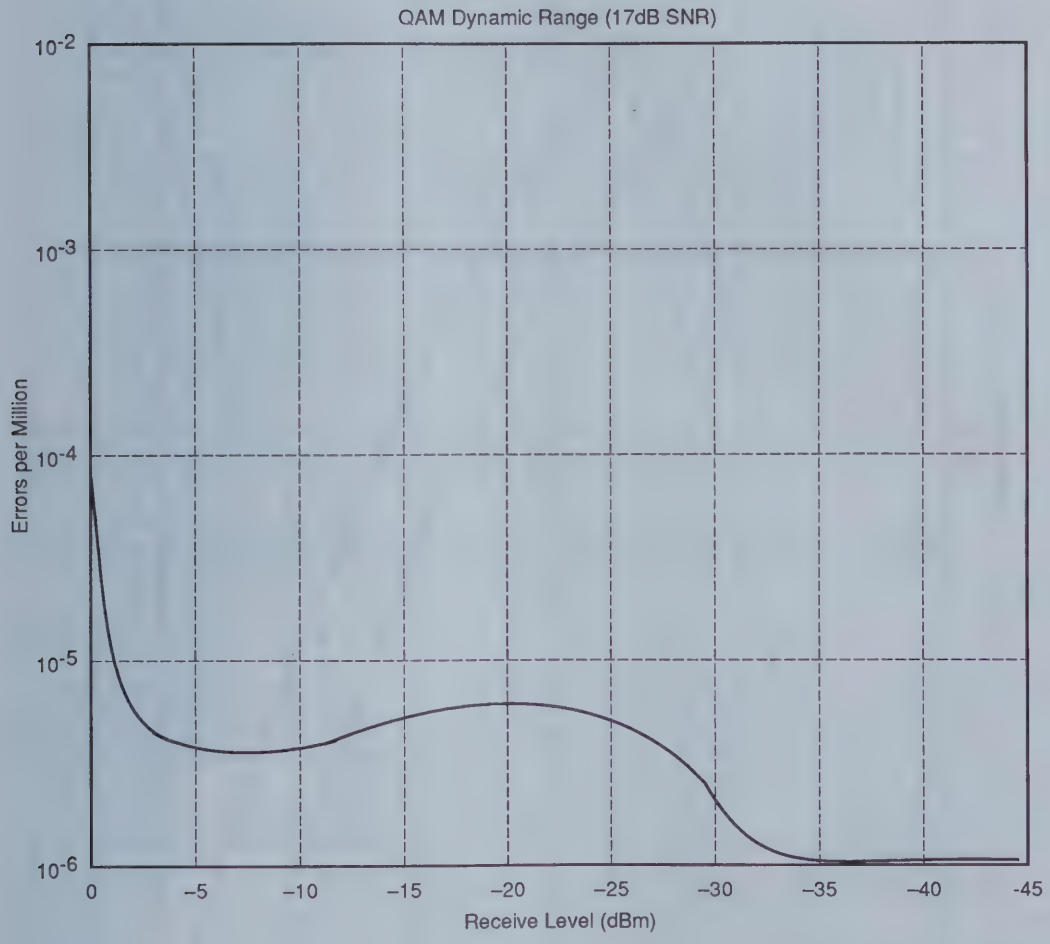


FIGURE 4: QAM Dynamic Range

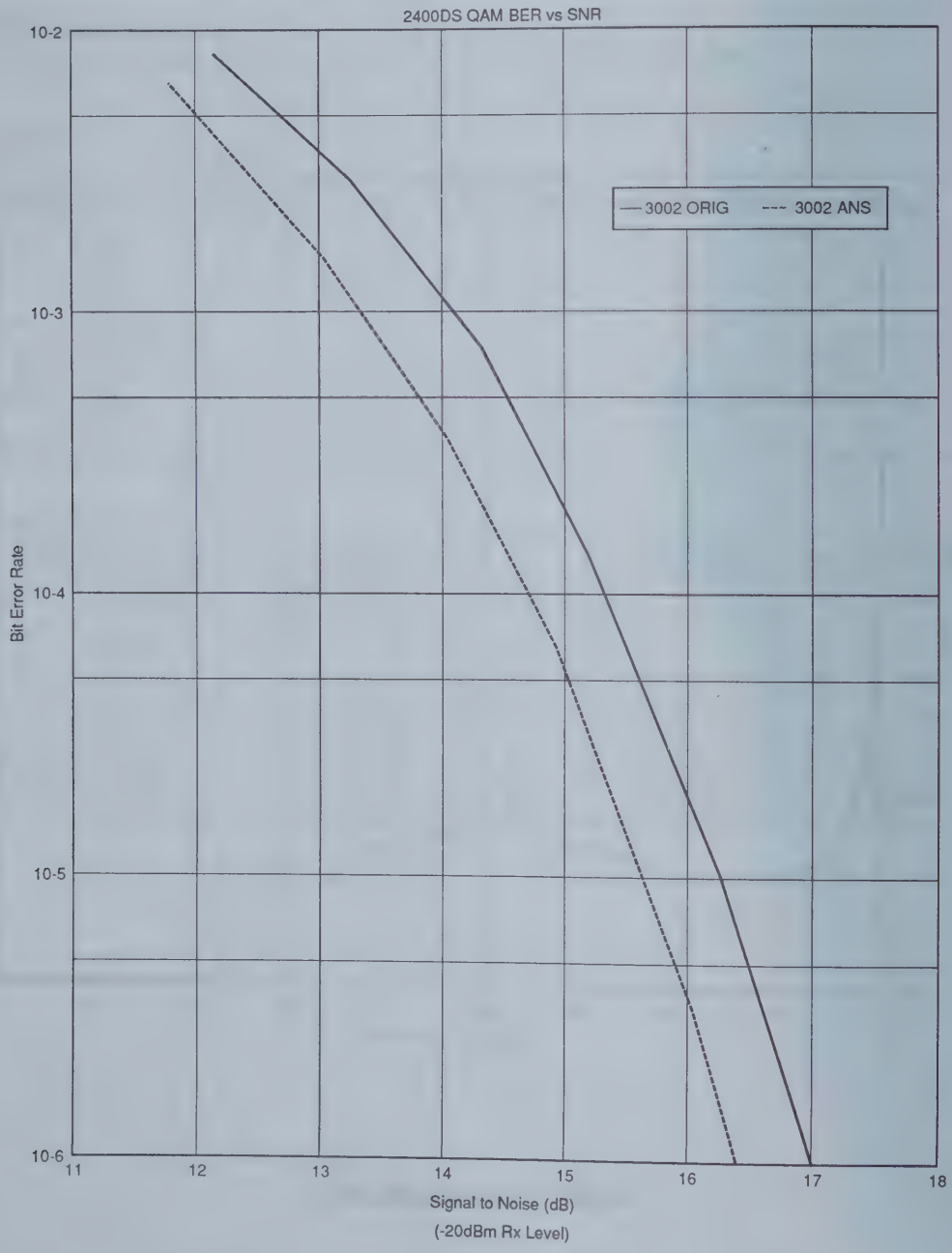


FIGURE 5: BER vs. SNR

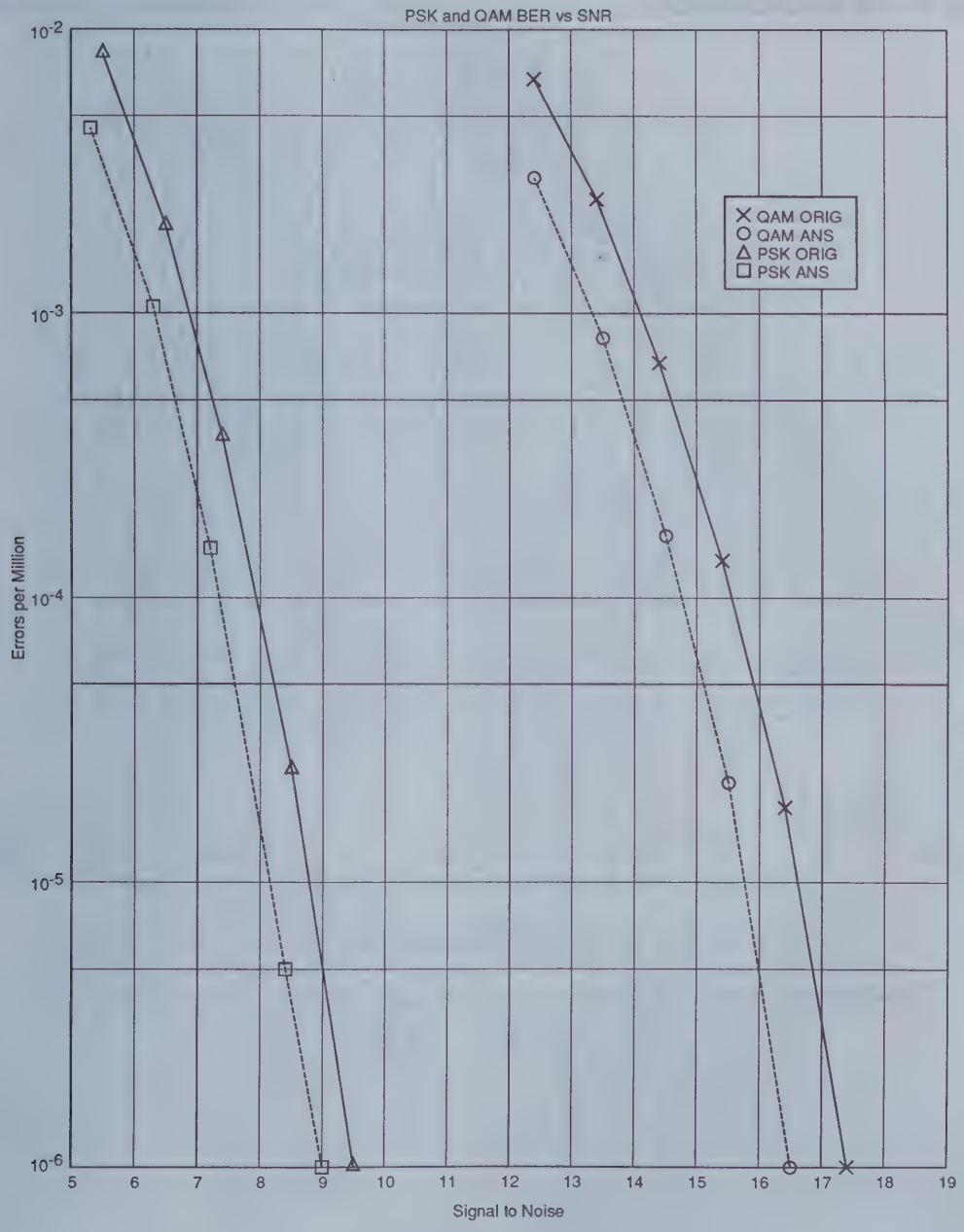


FIGURE 6: QAM and PSK BER vs. SNR with -20dBm Receive Level

APPLICATION INFORMATION

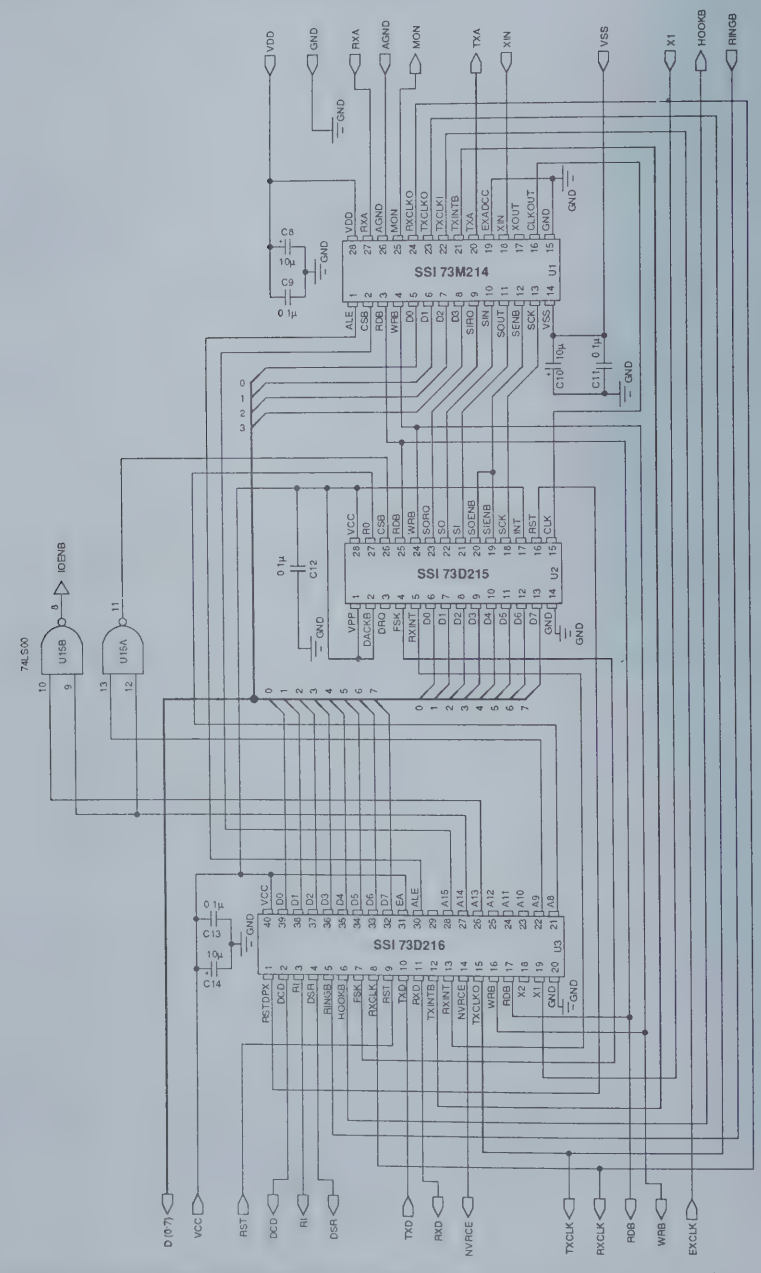


FIGURE 7: SSI 73D2404 System Interconnect

APPLICATION INFORMATION (Continued)

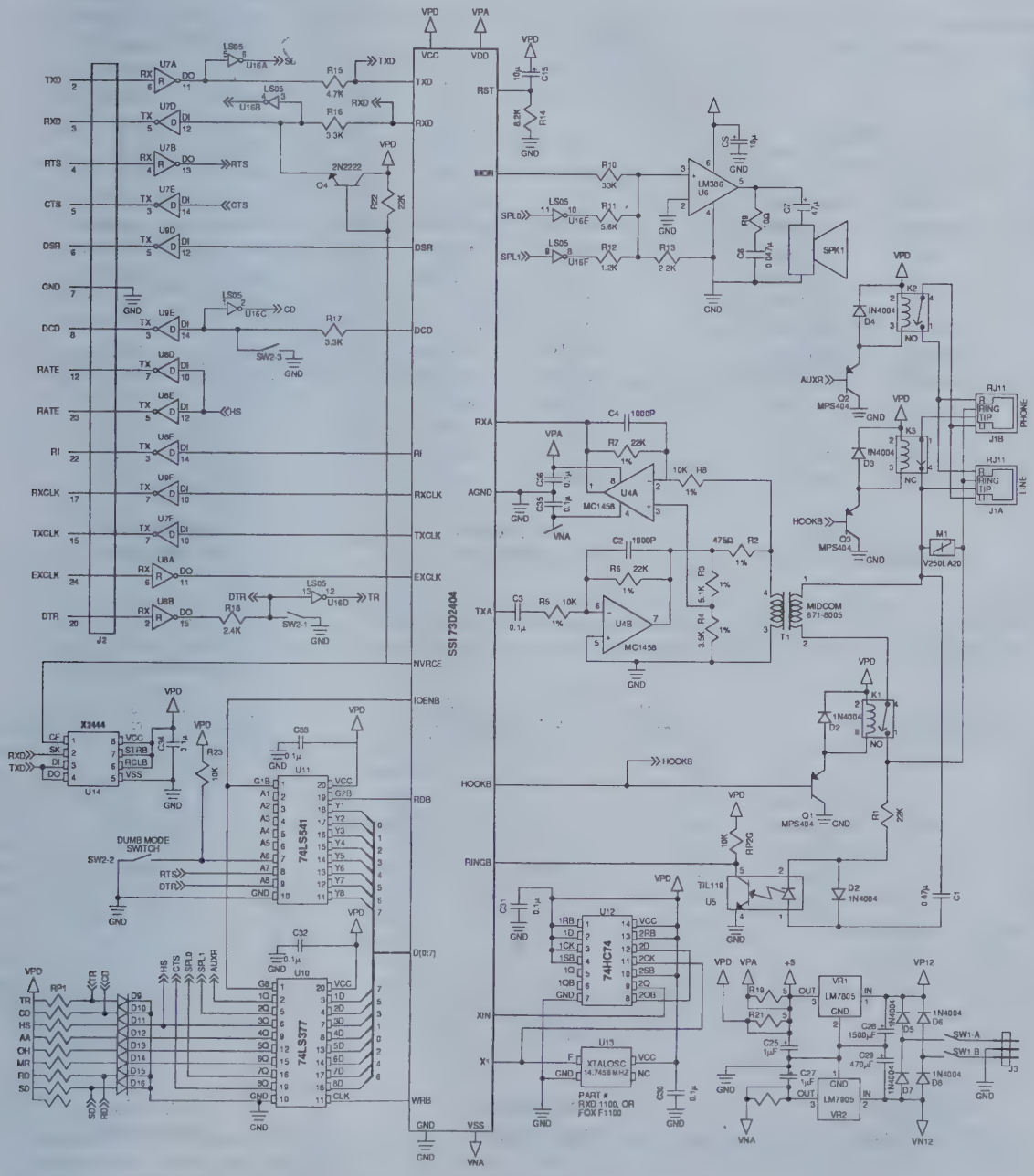
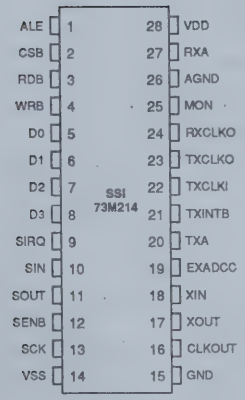


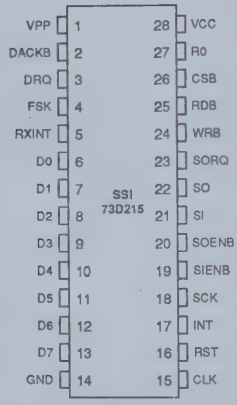
FIGURE 8: Sample Application Circuit

SSI 73D2404
V.22 bis 2400 Bit/s
Modem Device Set

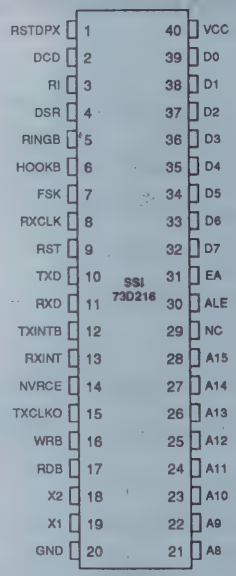
PACKAGE PIN DESIGNATIONS (TOP VIEW)



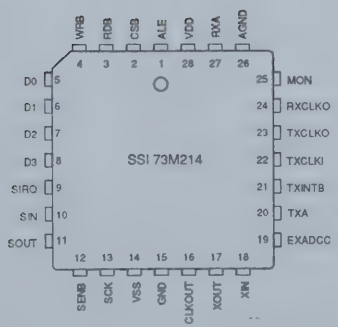
SSI 73M214
28-PIN DIP, CERDIP



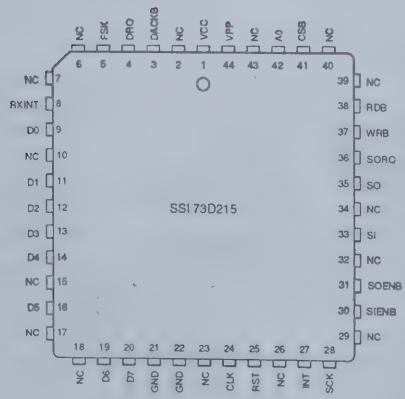
SSI 73D215
28-PIN DIP



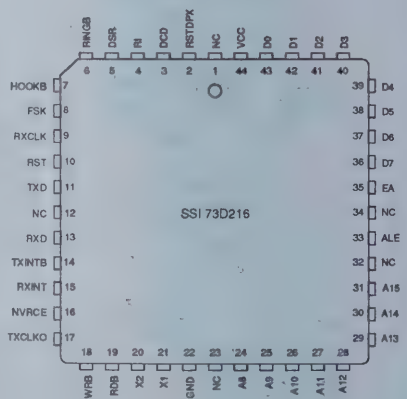
SSI 73D216
40-PIN DIP



SSI 73M214
28-PIN PLCC



SSI 73D215
44-PIN PLCC



SSI 73D216
44-PIN PLCC

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 73D2404 Dual-In-Line Package	SSI 73D2404-CP	
28-pin Plastic DIP		73M214-IP
28-pin Plastic DIP		73D215-CP
40-pin Plastic DIP		73D216-CP
SSI 73D2404 Surface Mount Package	SSI 73D2404-CH	
28-pin Plastic Leaded Chip Carrier		73M214-IH
44-pin Plastic Leaded Chip Carrier		73D215-CH
44-pin Plastic Leaded Chip Carrier		73D216-CH

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NOTES:

SSI 73M450/450F
Universal Asynchronous Receiver/Transmitter

July, 1989

DESCRIPTION

The SSI 73M450 is a Universal Asynchronous Receiver/Transmitter (UART) circuit which is pin- and function-compatible with industry-standard 16C450-type UARTs. It is primarily used in the interface between the serial data port and the parallel peripheral bus in 8-bit microprocessor systems. The 73M450F is a fast version of the UART that does not require wait states for operation with newer, higher-speed processors. Both versions are designed in CMOS for low-power quiescent operation. The 73M450 and 73M450F require only a single 5-volt supply and are available in either a 40-pin DIP or 44-pin PLCC package.

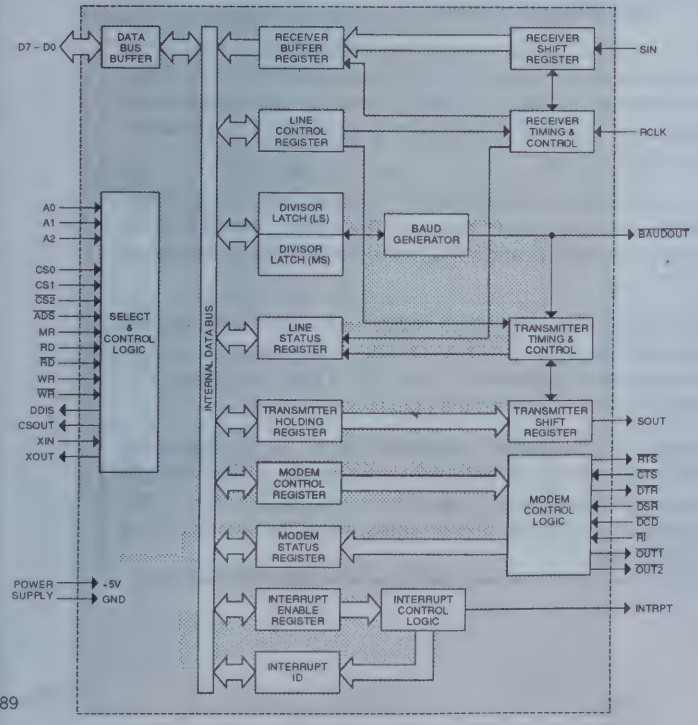
FEATURES

- Compatible with industry-standard UARTs
- High-speed version for zero wait-state operation with higher-speed busses

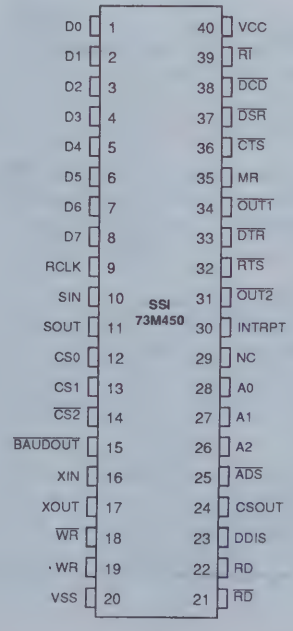
FEATURES (Continued)

- Fully CMOS for low-power quiescent operation
- High drive current for directly driving large loads
- Full double buffering
- Independent control of transmit, receive, line status and data set interrupts
- Contains modem control function including $\overline{CTS}$, $\overline{TRS}$, $\overline{DSR}$, $\overline{DTR}$, $\overline{RI}$ and $\overline{DCD}$
- Programmable serial interface characteristics include:
  - 5, 6, 7 or 8-bit characters
  - even, odd or no-parity bit generation and detection
  - 1, 1 1/2 or 2 stop-bit generation
  - baud rate generation (dc to 56K baud)
- Full status reporting capabilities
- Available in 40-pin DIP or 44-pin PLCC

BLOCK DIAGRAM



PIN DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

0789

PIN DESCRIPTION

BUS INTERFACE

NAME	DIP	PLCC	TYPE	DESCRIPTION
$\overline{ADS}$	25	28	I	Address Strobe: The rising edge of this signal is used for latching the Register Address and Chip Select inputs, thus facilitating interface to a multiplexed Address/Data bus. If not required, $\overline{ADS}$ should be tied permanently low.
CS0, CS1, $\overline{CS2}$	12-14	14-16	I	Chip Select: The UART is selected when CS0 and CS1 are high and $\overline{CS2}$ is low. Chip selection is complete when the decoded chip select signal is latched with an active (low) $\overline{ADS}$ input. This enables communication between the UART and the CPU.
A0-2	28-26	31-29	I	Register Select Address: These pins determine which of the UART registers is being selected during a read or write on the UART Data Bus. The contents of the DLAB bit in the UART's Line Control Register (see Table 1) also controls which register is referenced.
RD, $\overline{RD}$	22,21	25,24	I	Read Strobe: A request to read status information or data from a selected register may be made by pulling RD high or $\overline{RD}$ low while the chip is selected. Since only one input is required for a read, tie either RD permanently low or $\overline{RD}$ permanently high if not used.
WR, $\overline{WR}$	19, 18,	21, 20	I	Write Strobe: A request to write control words or data into a selected register may be made by pulling WR high or $\overline{WR}$ low while the chip is selected. Since only one input is required for a write, tie either WR permanently low or $\overline{WR}$ permanently high if not used.
D0-7	1-8	2-9	I/O	UART Data Bus (three-state): This bus provides bi-directional communications between the UART and the CPU; data, control words and status information are transferred via this bus.
CSOUT	24	27	O	Chip Select Out: When high, indicates that the chip has been selected by active CS0, CS1 and $\overline{CS2}$ inputs. No data transfer can be initiated until the CSOUT signal is a logic "1." CSOUT goes low when the chip is deselected.
DDIS	23	26	O	Driver Disable: Goes low when the CPU is reading data from the UART. A high-level DDIS output can be used to disable an external transceiver (if used between the CPU and UART on the D0-D7 Data Bus) at all times, except when the CPU is reading data.

BUS INTERFACE (Continued)

NAME	DIP	PLCC	TYPE	DESCRIPTION
INTRPT	30	33	O	Interrupt: Goes high whenever any one of the following interrupt types has an active high condition and is enabled via the IER: Receiver Error Flag, Received Data Available, Transmitter Holding Register Empty and Modem Status. The INTRPT signal is reset low upon the appropriate interrupt service or a Master Reset operation.

DATA I/O

NAME	DIP	PLCC	TYPE	DESCRIPTION
SIN	10	11	I	Serial Input: Input for serial data from the communications link (peripheral device, modem or data set).
SOUT	11	13	O	Serial Output: Output for serial data to the communications link (peripheral device,modem or data set). This signal is set high upon a Master Reset.

MODEM CONTROL

NAME	DIP	PLCC	TYPE	DESCRIPTION
$\overline{\text{RTS}}$	32	36	O	Request To Send: This output is programmed by bit 1 of the Modem Control Register and is used in modem handshaking to signify that the UART has data to transmit. This signal is set high upon Master Reset or during loop mode operation.
$\overline{\text{CTS}}$	36	40	I	Clear To Send: A modem status input whose condition corresponds to the complement of the CTS bit (bit 4) of the Modem Status Register. When $\overline{\text{CTS}}$ is low, it indicates that communications have been established and that data may be transmitted.
$\overline{\text{DTR}}$	33	37	O	Data Terminal Ready: This output is programmed by bit 0 of the Modem Control Register, and is used in modem handshaking to signify that the UART is available to communicate. This signal is set high upon Master Reset or during loop mode operation.
$\overline{\text{DSR}}$	37	41	I	Data Set Ready: A modem status input whose condition corresponds to the complement of the DSR bit (bit 5) of the Modem Status Register. When $\overline{\text{DSR}}$ is low, it indicates that the modem is ready to establish communications.

MODEM CONTROL (Continued)

NAME	DIP	PLCC	TYPE	DESCRIPTION
$\overline{DCD}$	38	42	I	Data Carrier Detect: A modem status input whose condition corresponds to the complement of the DCD bit (bit 7) of the Modem Status Register. When $\overline{DCD}$ is low, it indicates that the modem is receiving a carrier.
$\overline{RI}$	39	43	I	Ring Indicator: A modem status input whose condition corresponds to the complement of the RI bit (bit 6) of the Modem Status Register. When $\overline{RI}$ is low, it indicates that a telephone ringing signal is being received.
$\overline{OUT1}$ $\overline{OUT2}$	34 31	38 35	O O	Output 1, 2: User designated outputs that can be set to an active low by setting bit 2 ($\overline{OUT1}$) or bit 3 ($\overline{OUT2}$) of the Modem Control Register high. These output signals are set high upon Master Reset or during loop mode operation.

GENERAL & CLOCKS

NAME	DIP	PLCC	TYPE	DESCRIPTION
VCC	40	44	I	+5V Supply, ±10%: Bypass with 0.1 µF capacitor to VSS.
VSS	20	22	I	System Ground.
MR	35	39	I	Master Reset: When high, this input clears all UART control logic and registers, except for the Receiver Buffer, Transmitter Holding and Divisor Latches; also, the state of output signals SOUT, INTRPT, $\overline{OUT1}$, $\overline{OUT2}$, $\overline{RTS}$ and $\overline{DTR}$ are affected by an active MR input. This input is buffered with a TTL-compatible Schmitt Trigger.
XIN, XOUT	16,17	18,19	I/O	External System Clock I/O: These two pins connect the main timing reference (crystal or signal clock) to the UART. Additionally, XIN may be driven by an external clock source.
RCLK	9	10	I	Receiver Clock: This input is the 16X baud rate clock for the receiver section of the chip.
$\overline{BAUDOUT}$	15	17	O	Baud Generator Output: 16X clock signal for the transmitter section of the UART, equal to the main reference oscillator frequency divided by the specified divisor in the Baud Generator Divisor Latches. May also be used for the receiver section by tying this output to the RCLK input of the chip.
NC	29	1,12 23, 34	-	No Connection: These pins have no internal connection and may be left floating.

TABLE 1: Control Register Address Table

DLAB	A2	A1	A0	REGISTER
0	0	0	0	Receiver Buffer (read), Transmitter Holding Register (write)
0	0	0	1	Interrupt Enable
X	0	1	0	Interrupt Identification (read only)
X	0	1	1	Line Control
X	1	0	0	Modem Control
X	1	0	1	Line Status
X	1	1	0	Modem Status
X	1	1	1	Scratch
1	0	0	0	Divisor Latch (least significant byte)
1	0	0	1	Divisor Latch (most significant byte)

TABLE 2: UART Reset Functions

REGISTER/SIGNAL	RESET CONTROL	RESET STATE
Interrupt Enable Register	Master Reset	All bits low (0-3 forced and 4-7 permanent)
Interrupt Identification Register	Master Reset	Bit 0 is high; bits 1 & 2 are low; bits 3-7 are permanently low
Line Control Register	Master Reset	All bits low
Modem Control Register	Master Reset	All bits low
Line Status Register	Master Reset	All bits low, except bits 5 & 6 are high
Modem Status Register	Master Reset	Bits 0-3 are low; bits 4-7 = input signal
SOUT	Master Reset	High
INTRPT (RCVR Errs)	Read LSR/MR	Low
INTRPT (RCVR Data Ready)	Read RBR/MR	Low
INTRPT (THRE)	Read IIR/Write THR/MR	Low
INTRPT (Modem Status Changes)	Read MSR/MR	Low
$\overline{OUT2}$	Master Reset	High
$\overline{RTS}$	Master Reset	High
$\overline{DTR}$	Master Reset	High
$\overline{OUT1}$	Master Reset	High

CONTROL REGISTER OVERVIEW

REGISTER		REGISTER ADDRESS (A2-A0) & DLAB	DATA BIT NUMBER D7	D6	D5	D4	D3	D2	D1	D0
RECEIVER BUFFER REGISTER (READ ONLY)	RBR	000 DLAB = 0	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
TRANSMIT HOLDING REGISTER (WRITE ONLY)	THR	000 DLAB = 0	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
INTERRUPT ENABLE REGISTER	IER	001 DLAB = 0	0	0	0	0	ENABLE MODEM STATUS INTERRUPT	ENABLE REC. LINE STATUS INTERRUPT	ENABLE THR EMPTY INTERRUPT	ENABLE REC. DATA AVAILABLE INTERRUPT
INTERRUPT ID REGISTER (READ ONLY)	IIR	010 DLAB = X	0	0	0	0	0	INTERRUPT ID BIT 1	INTERRUPT ID BIT 0	"0" IF INTERRUPT PENDING
LINE CONTROL REGISTER	LCR	011 DLAB = X	DIVISOR LATCH ACCESS (DLAB)	SET BREAK	STICK PARITY	EVEN PARITY SELECT (EPS)	PARITY ENABLE (PEN)	NUMBER OF STOP BITS (STB)	WORD LENGTH SELECT 1 (WLS1)	WORD LENGTH SELECT 0 (WLS0)
MODEM CONTROL REGISTER	MCR	100 DLAB = X	0	0	0	LOOP	OUT2	OUT1	REQUEST TO SEND (RTS)	DATA TERMINAL READY (DTR)
LINE STATUS REGISTER	LSR	101 DLAB = X	0	TRANSMIT-TER EMPTY (TEMT)	TRANSMIT HOLDING REGISTER EMPTY(THRE)	BREAK INTERRUPT (BI)	FRAMING ERROR (FE)	PARITY ERROR (PE)	OVERRUN ERROR (OE)	DATA READY (DR)
MODEM STATUS REGISTER (READ ONLY)	MSR	110 DLAB = X	DATA CARRIER DETECT (DCD)	RING INDICATOR (RI)	DATA SET READY (DSR)	CLEAR TO SEND (CTS)	DELTA DATA CARR. DETECT (DDCD)	TRAILING EDGE RING INDICATOR (TERI)	DELTA DATA SET READY (DDSR)	DELTA CLEAR TO SEND (DCTS)
SCRATCH REGISTER	SCR	111 DLAB = X	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DIVISOR LATCH (LS)	DLL	000 DLAB = 1	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DIVISOR LATCH (MS)	DLM	001 DLAB = 1	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8

REGISTER BIT DESCRIPTIONS

RECEIVER BUFFER REGISTER (RBR) (READ ONLY)
UART ADDRESS: A2 - A0 = 000, DLAB = 0

This read only register contains the parallel received data with start, stop, and parity bits (if any) removed. The high order bits for less than 8 data bits/character will be set to 0.

TRANSMIT HOLDING REGISTER (THR) (WRITE ONLY)
UART ADDRESS: A2 - A0 = 000, DLAB = 0

This write only register contains the parallel data to be transmitted. The data is sent LSB first with start, stop, and parity bits (if any) added to the serial bit stream as the data is transferred.

INTERRUPT ENABLE REGISTER (IER)
UART ADDRESS: A2 - A0 = 001, DLAB = 0

This 8-bit register enables the four types of interrupts of the UART to separately activate the chip Interrupt (INTRPT) output signal. It is possible to totally disable the interrupt system by resetting bits 0 through 3 of the Interrupt Enable Register. Similarly, by setting the appropriate bits of this register to a logic 1, selected interrupts can be enabled. Disabling the interrupt system inhibits the Interrupt Identification Register and the active (high) INTRPT output from the chip. All other system functions operate in their normal manner, including the setting of the Line Status and Modem Status Registers.

BIT	NAME	COND.	DESCRIPTION
D0	Received Data	1	This bit enables the Received Data Available Interrupt when set to logic 1.
D1	Transmitter Holding Register Empty	1	This bit enables the Transmitter Holding Register Empty Interrupt when set to logic 1.
D2	Receiver Line Status Interrupt	1	This bit enables the Receiver Line Status Interrupt when set to logic 1.
D3	Modem Status	1	This bit enables the Modem Status Interrupt when set to logic 1.
D4 - D7	Not Used	0	These three bits are always logic 0.

INTERRUPT ID REGISTER (IIR) (READ ONLY)
UART ADDRESS: A2 - A0 = 010

The IIR register gives prioritized information as to the status of interrupt conditions. When accessed, the IIR freezes the highest priority interrupt pending and no other interrupts are acknowledged until the particular interrupt is serviced by the CPU. The order of interrupt priorities is shown in the table below.

BIT	NAME	COND.	DESCRIPTION
D0	Interrupt Pending	0	This bit can be used in either a hardwired prioritized or polled environment to indicate whether an interrupt is pending. When bit 0 is a logic 0, an interrupt is pending and the IIR contents may be used as a pointer to the appropriate interrupt service routine.
		1	When bit 0 is a logic 1, no interrupt is pending.
D1, D2	Interrupt ID bits 0, 1	Table below	These two bits of the IIR are used to identify the highest priority interrupt pending as indicated in the following table.
D3 - D7	Not Used	0	These five bits of the IIR are always logic 0.

INTERRUPT PRIORITY TABLE

D2	D1	D0	PRIORITY	TYPE	SOURCE	RESET
0	0	1	-	None	None	N/A
1	1	0	Highest	Receiver Line Status	Overrun Error, Parity Error, Framing Error or Break Interrupt	Reading the Line Status Register
1	0	0	Second	Receive Data Available	Receive Data Available	Reading the Rcvr. Buffer Register
0	1	0	Third	Transmit Holding Register Empty	Transmit Holding Register Empty	Reading IIR Register (if source of interrupt) or Writing to Transmit Holding Register
0	0	0	Fourth	Modem Status	Clear to Send or Data Set Ready or Ring Indicator or Data Carrier Det.	Reading the Modem Status Register

LINE CONTROL REGISTER (LCR)
UART ADDRESS: A2 - A0 = 011

The user specifies the format of the asynchronous data communications exchange via the Line Control Register. In addition to controlling the format, the user may retrieve the contents of the Line Control Register for inspection. This feature simplifies system programming and eliminates the need for separate storage in system memory of the line characteristics.

BIT	NAME	COND.		DESCRIPTION
D0	Word Length Select 0 (WLS0)			Bits D0 and D1 select the number of data bits per character as shown:
D1	Word Length Select 1 (WLS1)	D1	D0	Word Length
		0	0	5 bits
		0	1	6 bits
		1	0	7 bits
		1	1	8 bits
D2	Number of Stop Bits (STB)	0 or 1		This bit specifies the number of stop bits in each transmitted character. If bit 2 is a logic 0, one stop bit is generated in the transmitted data. If bit 2 is a logic 1 when a 5-bit word length is selected via bits 0 and 1, one-and-a-half stop bits are generated. If bit 2 is a logic 1 when either a 6, 7, or 8-bit word length is selected, two stop bits are generated. The receiver checks the first stop bit only, regardless of the number of stop bits selected.
D3	Parity Enable (PEN)	1		This is the Parity Enable (PEN) bit. When set to a logic 1, a parity bit is generated (transmit data) or checked (receive data) between the last data word bit and stop bit of the serial data. (The parity bit is used to produce an even or odd number of 1's when the data word bits and the parity bit are summed).
D4	Even Parity Select (EPS)	1 or 0		This is the Even Parity Select (EPS) bit. When bit 3 is a logic 1 and bit 4 is a logic 0, an odd number of logic 1's is transmitted or checked in the data word bits and parity bit. When bit 3 is a logic 1 and bit 4 is a logic 1, an even number of logic 1's is transmitted or checked.

LINE CONTROL REGISTER (LCR) (Continued)

BIT	NAME	COND.		DESCRIPTION
D5	Stick Parity	1 or 0		This is the Stick Parity bit. When bit 3 is a logic 1 and bit 5 is a logic 1, the parity bit is transmitted, and checked by the receiver as a logic 0 if bit 4 is a logic 1 or as a logic 1 if bit 4 is a logic 0.
		D5	D4	Parity
		0	0	ODD Parity
		0	1	EVEN Parity
		1	0	MARK Parity
		1	1	SPACE Parity
D6	Set Break	1		This is the Break Control bit. When set to a logic 1, the serial out (SOUT) is forced to a logic 0 state. The break is disabled by setting bit 6 to a logic 0. This bit acts only on SOUT and has no effect on the transmitter logic. See note below.
D7	Divisor Latch Access Bit (DLAB)	1		The Divisor Latch Access Bit (DLAB) must be set high (logic 1) to access the Divisor Latches of the baud generator during a Read or Write operation. It must be set low (logic 0) to access the Receiver Buffer, the Transmitter Holding Register, or the Interrupt Enable Register.

NOTE: This feature enables the CPU to alert a terminal in a computer communications system. If the following sequence is followed, no erroneous or extraneous characters will be transmitted because of the break.

1. Load an all 0's pad character in response to THRE.
2. Set break in response to the next THRE.
3. Wait for the Transmitter to be idle. (TEMT = 1), and clear break when normal transmission has to be restored.

During the break, the Transmitter can be used as a character timer to accurately establish the break duration.

MODEM CONTROL REGISTER (MCR)
UART ADDRESS: A2 - UA0 = 100

The Modem Control Register controls the interface with the modem, data set or peripheral device. Bits D1 and D0 are also available as read only bits in the UART Control Register in the Modem Registers.

BIT	NAME	COND.	DESCRIPTION
D0	DTR	1	This bit controls the Data Terminal Ready ($\overline{DTR}$) output. When bit 0 is set to a logic 1, the $\overline{DTR}$ output is forced to a logic 0. When bit 0 is reset to a logic 0, the $\overline{DTR}$ output is forced to a logic 1.
D1	RTS	1	This bit controls the Request to Send ($\overline{RTS}$) output. When bit 1 is set to a logic 1, the $\overline{RTS}$ output is forced to a logic 0. When bit 1 is reset to a logic 0, the $\overline{RTS}$ output is forced to a logic 1.
D2	OUT1	1	This bit controls the Output 1 ($\overline{OUT1}$) signal, which is an auxiliary user-designated output. When bit 2 is set to a logic 1, the $\overline{OUT1}$ output is forced to a logic 0. When bit 2 is reset to a logic 0, the $\overline{OUT1}$ output is forced to a logic 1.
D3	OUT2	0	This bit controls the Output 2 ($\overline{OUT2}$) signal, which is an auxiliary user-designated output. When bit 3 is set to a logic 1, the $\overline{OUT2}$ output is forced to a logic 0. When bit 3 is reset to a logic 0, $\overline{OUT2}$ output is forced to a logic 1.
D4	LOOP	1	This bit provides a local loopback feature for diagnostic testing of the UART. When bit 4 is set to logic 1, the following occurs: the transmitter Serial Output (SOUT) is set to the logic 1 state; the receiver Serial Input (SIN) is disconnected; the output of the Transmitter Shift Register is "looped back" into the Receiver Shift Register input; the four Modem Control inputs ($\overline{CTS}$, $\overline{DSR}$, $\overline{DCD}$ and $\overline{RI}$) are disconnected; the four Modem Control outputs ($\overline{DTR}$, $\overline{RTS}$, $\overline{OUT1}$ and $\overline{OUT2}$) are internally connected to the four Modem Control inputs, and the Modem Control output pins are forced to their inactive state (high). In the diagnostic mode, data that is transmitted is immediately received. This feature allows the processor to verify the transmit and received-data paths of the UART. In the diagnostic mode, the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational, but the interrupts' sources are now the lower four bits of the Modem Control Register instead of the four Modem Control inputs. The interrupts are still controlled by the Interrupt Enable Register.
D5-D7		0	These bits are permanently set to logic 0.

LINE STATUS REGISTER (LSR)
UART ADDRESS: A2 - A0 = 101

This register provides status information to the CPU concerning the data transfer. Bits 1-4 are the error conditions that produce a Receiver Line Status interrupt whenever any of the corresponding conditions are detected. The Line Status Register is intended for read operation only. Writing to this register is not recommended as this operation is used for factory testing.

BIT	NAME	COND.	DESCRIPTION
D0	DR	1	The Data Ready (DR) bit is set to a 1 whenever a complete incoming character has been received and transferred into the Receiver Buffer Register. DR is reset to 0 by reading the data in the Receiver Buffer Register.
D1	OE	1	The Overrun Error (OE) bit indicates that the data in the Receiver Buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer Register, thereby destroying the previous character. OE is reset to 0 whenever the CPU reads the contents of the Line Status Register.
D2	PE	1	The Parity Error (PE) bit indicates that the received character did not have the correct parity. PE is reset to 0 whenever the CPU reads the Line Status Register.
D3	FE	1	The Framing Error (FE) bit indicates that the received character did not have a valid stop bit. FE is reset to 0 whenever the CPU reads the contents of the Line Status Register.
D4	BI	1	The Break Interrupt (BI) bit indicates that a break has been received. A break occurs whenever the received data is held to 0 for a full data word (start + data + stop). BI is reset to 0 whenever the CPU reads the Line Status Register.
D5	THRE	1	The Transmit Holding Register Empty (THRE) is set to a logic 1 when a character is transferred from the Transmit Holding Regsiter into the Transmit Shift Register, indicating that the UART is ready to accept a new character for transmission. In addition, this bit causes the UART to issue an interrupt to the CPU when the THRE Interrupt enable is set high. THRE is reset to 0 when the CPU loads a character into the Transmit Holding Register.
D6	TEMT	1	The Transmit Empty (TEMT) indicates that both the Transmit Holding Register and the Transmit Shift Registers are empty. TEMT is reset to 0 whenever the TSR or THR contains a data character.
D7	-	0	Always zero.

MODEM STATUS REGISTER (MSR) (READ ONLY)
UART ADDRESS: A2 - A0 = 110

This register provides the current state of the control signals from the modem or peripheral device. In addition, four bits provide change information. Whenever bit 0, 1, 2 or 3 is set to logic 1, a Modem Status Interrupt is generated; reset to logic 0 occurs whenever they are read. In Loop Mode CTS, DSR, RI and DCD are taken from RTS, DTR, OUT1, and OUT2 in the Modem Control Register respectively.

BIT	NAME	COND.	DESCRIPTION
D0	DCTS	1	The Delta Clear to Send (DCTS) bit indicates that the $\overline{CTS}$ input to the chip has changed state since the last time it was read by the CPU.
D1	DDSR	1	The Delta Data Set Ready (DDSR) bit indicates that the $\overline{DSR}$ input to the chip has changed state since the last time it was read by the CPU.
D2	TERI	1	The Trailing Edge of the Ring Indicator (TERI) detect bit indicates that the $\overline{RI}$ input to the chip has changed from an Off (logic 0) to an On (logic 1) condition.
D3	DDCD	1	The Delta Data Carrier Detect (DDCD) bit indicates that the $\overline{DCD}$ input to the chip has changed state.
D4	CTS	1	This bit is the complement of the Clear To Send ($\overline{CTS}$) input. If bit 4 (loop) of the MCR is set to a 1, this bit is equivalent to RTS in the MCR.
D5	DSR	1	This bit is the complement of the Data Set Ready ($\overline{DSR}$) input. If bit 4 of the MCR is set to a 1, this bit is the equivalent of DTR in the MCR.
D6	RI	1	This bit is the complement of the Ring Indicator ($\overline{RI}$) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to OUT1 in the MCR.
D7	DCD	1	This bit is the complement of the Data Carrier Detect ($\overline{DCD}$) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to OUT2 in the MCR.

SCRATCH REGISTER (SCR)
ADDRESS: A2 - A0 = 111

This 8-bit Read/Write Register does not control the UART in any way. It is intended as a scratchpad register to be used by the programmer to hold data temporarily.

DIVISOR LATCH (LS) (DLL)
ADDRESS: A2 - A0 = 000, DLAB = 1

This write-only register contains the least significant byte of the divisor which is used to control the rate of the programmable baud generator.

DIVISOR LATCH (MS) (DLM)
ADDRESS: A2 - A0 = 001, DLAB = 1

This write-only register contains the most significant byte of the divisor which is used to control the rate of the programmable baud generator.

PROGRAMMABLE BAUD GENERATOR

The UART contains a programmable Baud Generator that is capable of taking any clock input (DC to 4 MHz) and dividing it by any divisor from 1 to 2^{16}-1. The output frequency of the Baud Generator is 16 x the Baud [divisor # = (frequency input)/(baud rate x 16)]. Two 8-bit latches store the divisor in a 16-bit binary format. These Divisor Latches must be loaded during initialization in order to ensure desired operation of the Baud Generator. Upon loading either of the Divisor Latches, a 16-bit Baud counter is immediately loaded. This prevents long counts on initial load.

Tables 3 and 4 illustrate the use of the Baud Generator with crystal frequencies of 1.8432 MHz and 3.072 MHz respectively. For baud rates of 38400 and below, the error obtained is minimal. The accuracy of the desired baud rate is dependent on the crystal frequency chosen.

TABLE 3: Baud Rates Using 1.8432 MHz Crystal

DESIRED BAUD RATE	DIVISOR USED TO GENERATE 16 X CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	2304	-
75	1536	-
110	1047	0.026
134.5	857	0.058
150	768	-
300	384	-
600	192	-
1200	96	-
1800	64	-
2000	58	0.69
2400	48	-
3600	32	-
4800	24	-
7200	16	-
9600	12	-
19200	6	-
38400	3	-
56000	2	2.86

TABLE 4: Baud Rates Using 3.072 MHz Crystal

DESIRED BAUD RATE	DIVISOR USED TO GENERATE 16 X CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	3840	-
75	2560	-
110	1745	0.026
134.5	1428	0.034
150	1280	-
300	640	-
600	320	-
1200	160	-
1800	107	0.312
2000	96	-
2400	80	-
3600	53	0.628
4800	40	-
7200	27	1.23
9600	20	-
19200	10	-
38400	5	-

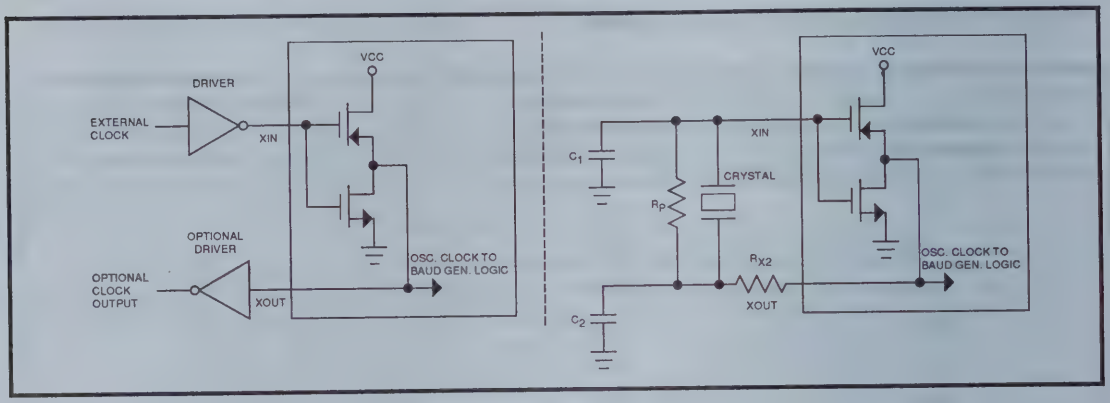


FIGURE 1: Typical Clock Circuits

TYPICAL CRYSTAL OSCILLATOR NETWORK

CRYSTAL	RP	RX2	C1	C2
1.8 - 3.1 MHz	1 MΩ	1.5K	10-30 pF	40-60 pF

ABSOLUTE MAXIMUM RATINGS

(TA = -40°C to +85°C, VCC = 5V ± 10%, unless otherwise noted. Operation above absolute maximum ratings may permanently damage the device.)

PARAMETER	CONDITIONS	RATING
VCC Supply Voltage		+14V
Storage Temperature		–65°C to 150°C
Lead Temperature	Soldering, 10 sec.	260°C
Applied Voltage		–0.3 to Vcc + 0.3

DC CHARACTERISTICS
(TA = –40°C to +85°C, VCC = 5V ± 10%, unless otherwise noted.)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
VILX	Clock input Low voltage		–0.5		0.8	V
VIHX	Clock input High Voltage		2.0		Vcc	V
VIL	Input Low Voltage		–0.5		0.8	V
VIH	Input High Voltage		2.0		Vcc	V
VOL	Output Low Voltage	IOL = 4.0 mA (except XOUT)			0.4	V
VOH	Output High Voltage	IOH = 5.0 mA on all outputs except XOUT	2.4			V
ICC	Average Power Supply	See Note 1		5	10	mA
	Current	See Note 2			50	µA
IIL	Input Leakage	VCC=5.25V, VSS=0V. All other pins floating.			±10	µA
ICL	Clock Leakage	VIN=0V, 5.25V			±10	µA
IOZ	3-State Leakage	VCC=5.25V, VSS=0V, VOUT=0V, 5.25V 1) Chip deselected 2) Chip & write mode selected			±20	µA
VILMR	MR Schmitt VIL				0.8	V
VIHMR	MR Schmitt VIH		2.0			V

Note 1: VCC = 5.25V, TA = 25°C; No loads on outputs. SIN, $\overline{DSR}$, $\overline{DCD}$, $\overline{CTS}$, $\overline{RI}$ = 2.4V. All other inputs = 0.4V. Baud Rate Gen. = 4 MHz; Baud Rate = 50 KHz.
Note 2: VCC = 5.5V, TA = –40°C; No output load; CMOS-level inputs, XIN = Vcc

CAPACITANCE
(TA = 25°C, VCC = VSS = 0V, fc = 1 MHz, unmeasured pins returned to VSS)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
CXTAL2	Clock Input Capacitance			15	20	pF
CXTAL1	Clock Output Capacitance			20	30	pF
CI	Input Capacitance			6	10	pF
CO	Output Capacitance			10	20	pF

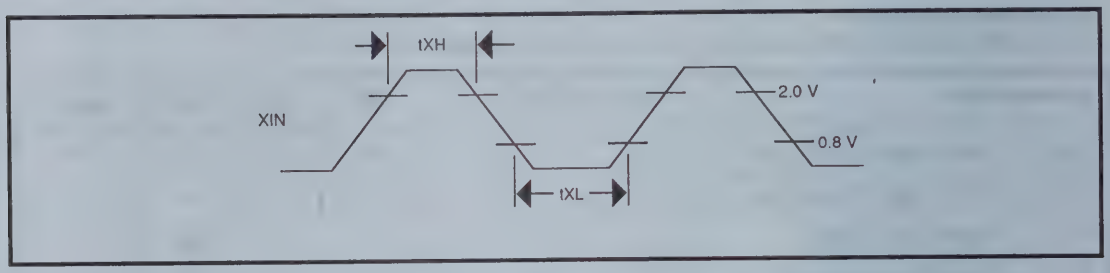


FIGURE 2: External Clock Input* (4 MHz Maximum)

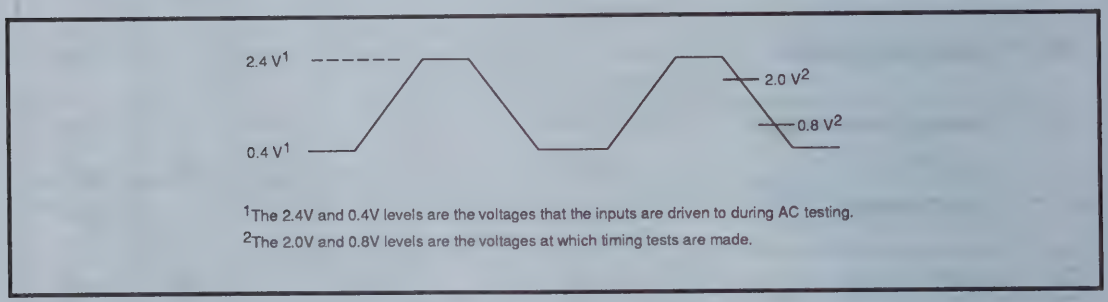

2.4 V1
0.4 V1
2.0 V2
0.8 V2
1The 2.4V and 0.4V levels are the voltages that the inputs are driven to during AC testing.
2The 2.0V and 0.8V levels are the voltages at which timing tests are made.

FIGURE 3: AC Test Points*

*All timings are referenced to valid 0 and valid 1.

AC CHARACTERISTICS (TA = -40°C to +85°C, VCC = 5V ± 10%, unless otherwise noted.)

READ & WRITE CYCLE (Refer to Figures 4 & 5.)

PARAMETER		CONDITIONS	73M450		73M450F		UNITS
			MIN	MAX	MIN	MAX	
tADS	Address Strobe Width		60		50		ns
tAS	Address Setup Time		60		30		ns
tAH	Address Hold Time		0		0		ns
tCS	Chip Select Setup Time		60		30		ns
tCH	Chip Select Hold Time		0		0		ns
tCSC	Chip Select Output Delay from Select	100 pF load See Note 3		100		80	ns
tCSR	RD, $\overline{RD}$ Delay from Chip Select	See Note 3	50		30		ns
tAR	RD, $\overline{RD}$ Delay from Address	See Note 3	60		30		ns

READ & WRITE CYCLE (Continued)

PARAMETER		CONDITIONS	73M450		73M450F		UNITS
			MIN	MAX	MIN	MAX	
tRD	RD, $\overline{RD}$ Strobe Width		125		80		ns
tRC	Read Cycle Delay		175		50		ns
tAD	Address to Read Data	73M450F only		NA		160	ns
RC	Read Cycle	See Note 1	360		210		ns
tRDD	RD, $\overline{RD}$ to Driver Disable Delay	100 pF load See Note 2		60		50	ns
tRVD	Delay from RD, $\overline{RD}$ to Data	100 pF load		125		80	ns
tHZ	RD, $\overline{RD}$ to Floating Data Delay	100 pF load See Note 2	0	100	0	60	ns
tRA	Address Hold Time from RD, $\overline{RD}$	See Note 3	20		20		ns
tRCS	Chip Select Hold Time from RD, $\overline{RD}$	See Note 3	20		20		ns
tCSW	WR, $\overline{WR}$ Delay from Select	See Note 3	50		30		ns
tAW	WR, $\overline{WR}$ Delay from Address	See Note 3	60		30		ns
tWR	WR, $\overline{WR}$ Strobe Width		100		80		ns
tWC	Write Cycle Delay		200		50		ns
WC	Write Cycle=tAW+tWR+tWC		360		160		ns
tDS	Data Setup Time		40		30		ns
tDH	Data Hold Time		40		30		ns
tWA	Address Hold Time from WR, $\overline{WR}$	See Note 3	20		20		ns
tWCS	Chip Select Hold time from WR, $\overline{WR}$	See Note 3	20		20		ns
tMRW	Master Reset Pulse Width		5		1		µs
tXH	Duration of Clock High Pulse	External Clock (4 MHz max.)	100		100		ns
tXL	Duration of Clock Low Pulse	External Clock (4 MHz max.)	100		100		ns

Note 1: RC = tAR + tRD + tRC for 73M450
RC = tAD + tRC for 73M450F
Note 2: Charge and discharge time is determined by VOL, VOH and the external loading.
Note 3: Applicable only when $\overline{ADS}$ is tied low.

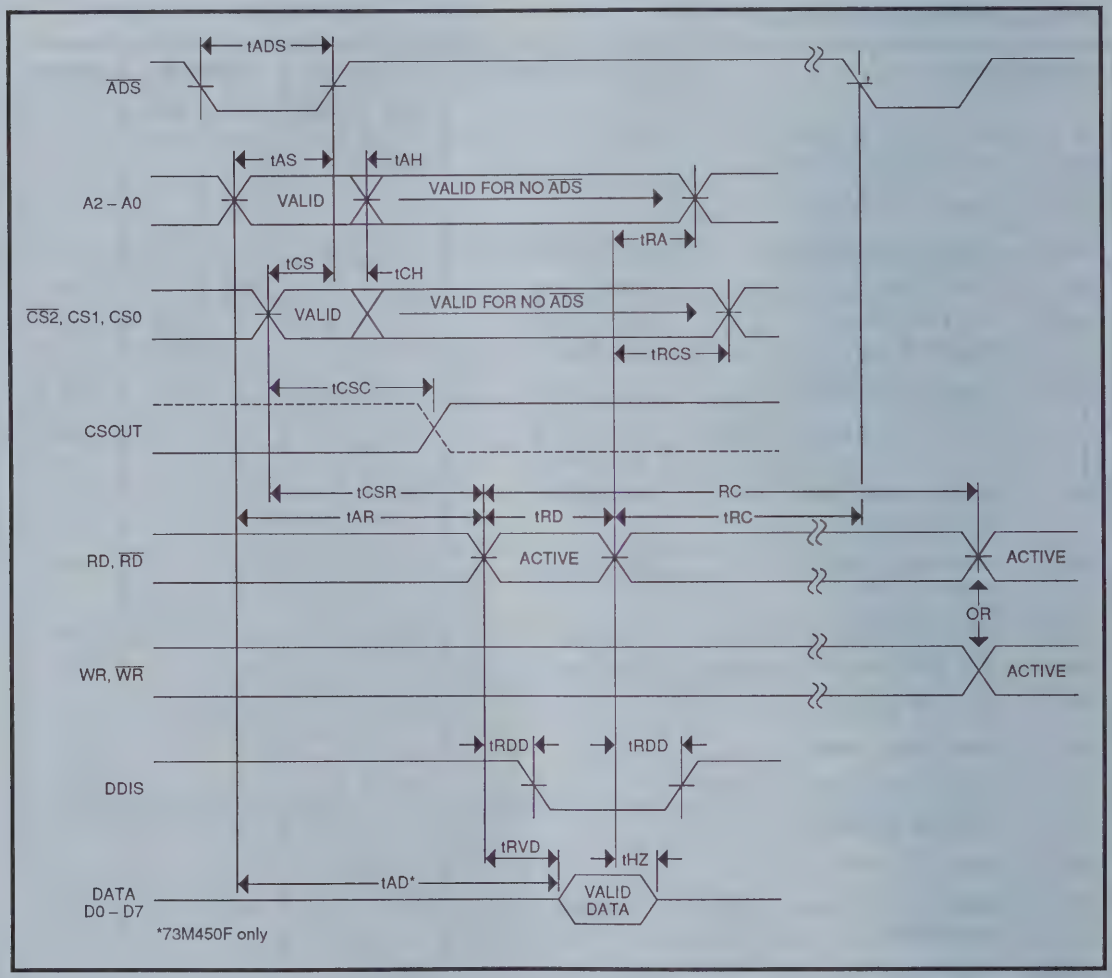


FIGURE 4: Read Cycle Timing

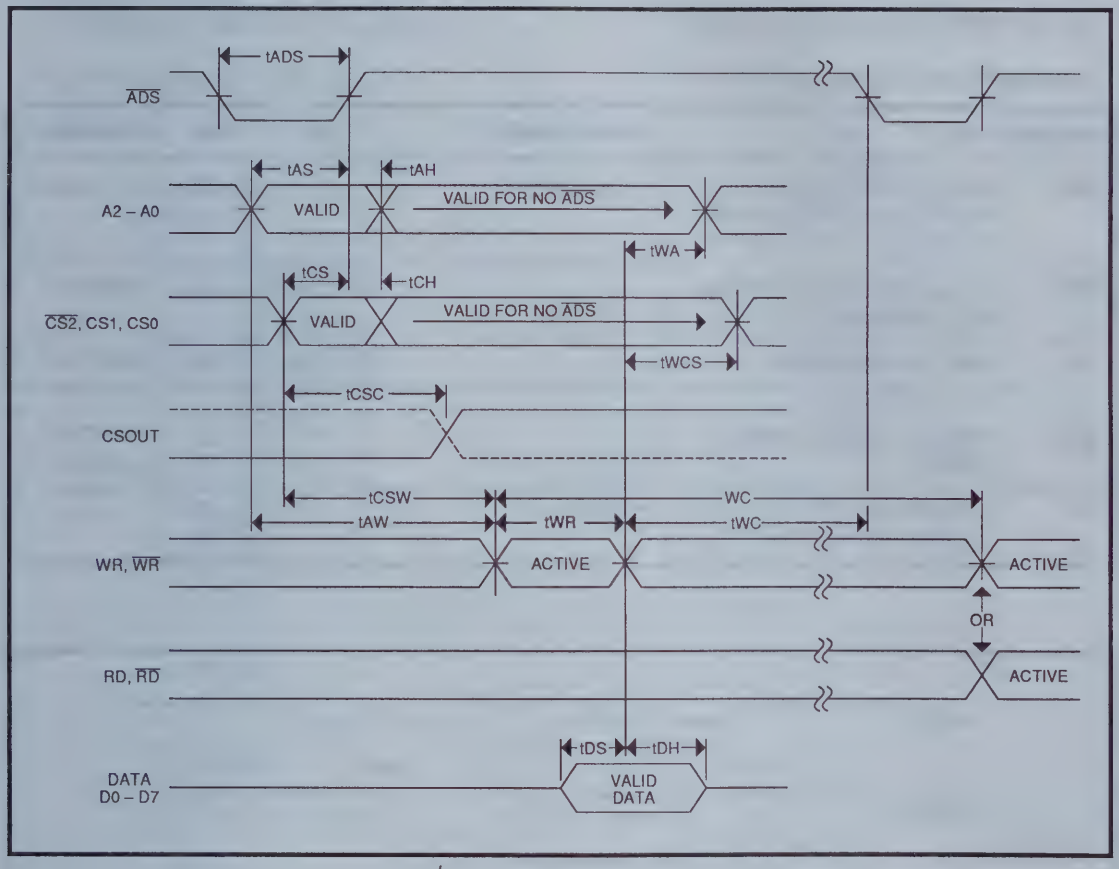


FIGURE 5: Write Cycle Timing

AC CHARACTERISTICS (Continued)

TRANSMITTER (Refer to Figure 6.)

PARAMETER		CONDITIONS	MIN	MAX	UNITS
tHR	Delay from rising edge of WR, $\overline{WR}$ (WR THR)to Reset Interrupt	100 pF load		175	ns
tIRS	Delay form Initial INTR Reset to Transmit Start		24	40	BAUDOUT cycles
tSI	Delay from Initial Write to Interrupt		16	32	BAUDOUT cycles
tSTI	Delay from Stop to Interrupt (THRE)		8	8	BAUDOUT cycles
tIR	Delay from RD, $\overline{RD}$ (RD IIR) to Reset Interrupt (THRE)	100 pF load		250	ns

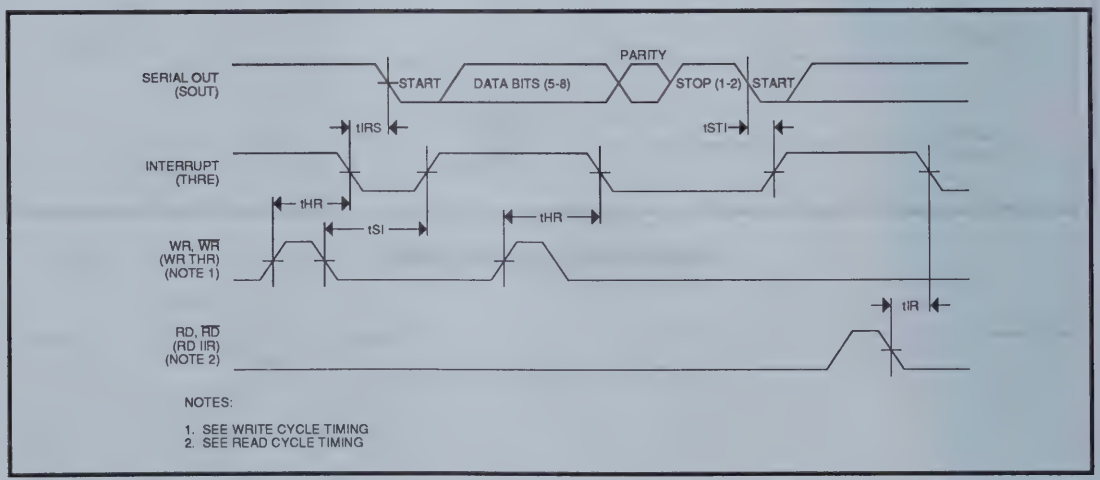


FIGURE 6: Transmitter Timing

AC CHARACTERISTICS (Continued)

MODEM CONTROL (Refer to Figure 7.)

PARAMETER		CONDITIONS	MIN	MAX	UNITS
tMDO	Delay from WR, $\overline{WR}$ (WR MCR) to Output	100 pF load		200	ns
tSIM	Delay to Set Interrupt from Modem Input	100 pF load		250	ns
tRIM	Delay to Reset Interrupt from RD, $\overline{RD}$ (RS MSR)	100 pF load		250	ns

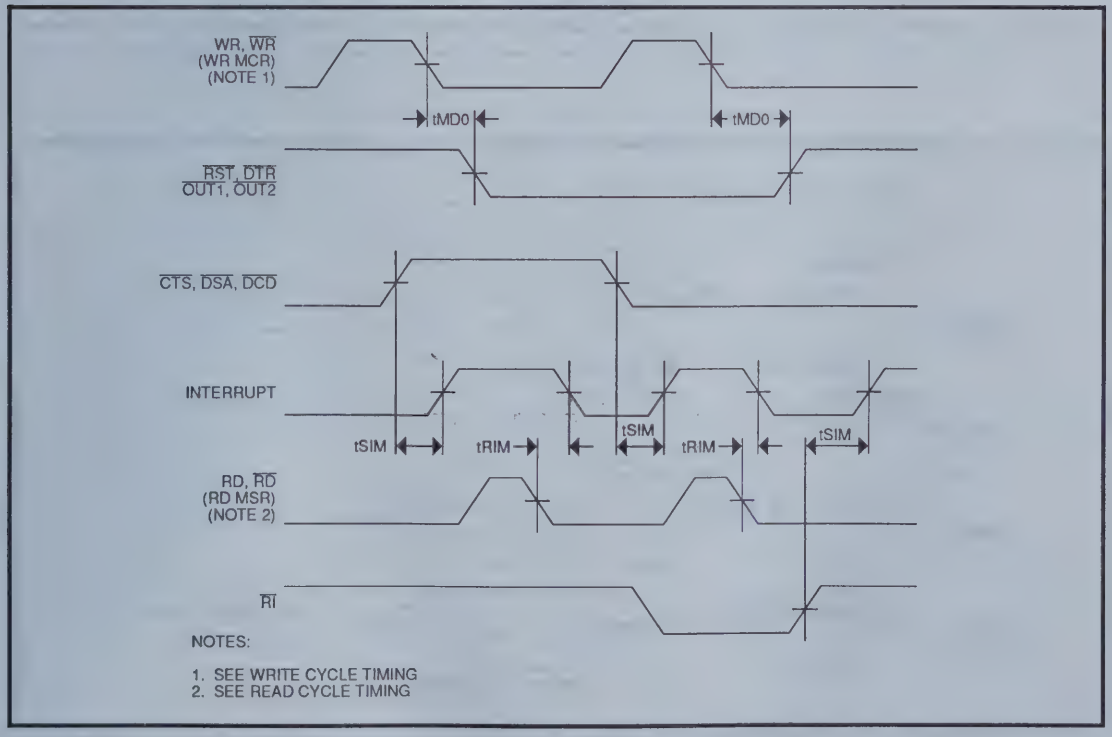


FIGURE 7: Modem Controls Timing

AC CHARACTERISTICS (Continued)

BAUD GENERATOR (Refer to Figure 8.)

PARAMETER		CONDITIONS	MIN	MAX	UNITS
N	Baud Divisor		1	2^{16}-1	
tBLD	Baud Output Negative Edge Delay	100 pF load		125	ns
tBHD	Baud Output Positive Edge Delay	100 pF load		125	ns
tLW	Baud Output Down Time	fX=2 MHz, div. by 2, 100 pF load	425		ns
tHW	Baud Output Up Time	fX=3 MHz, div. by 3, 100 pF load	250		ns

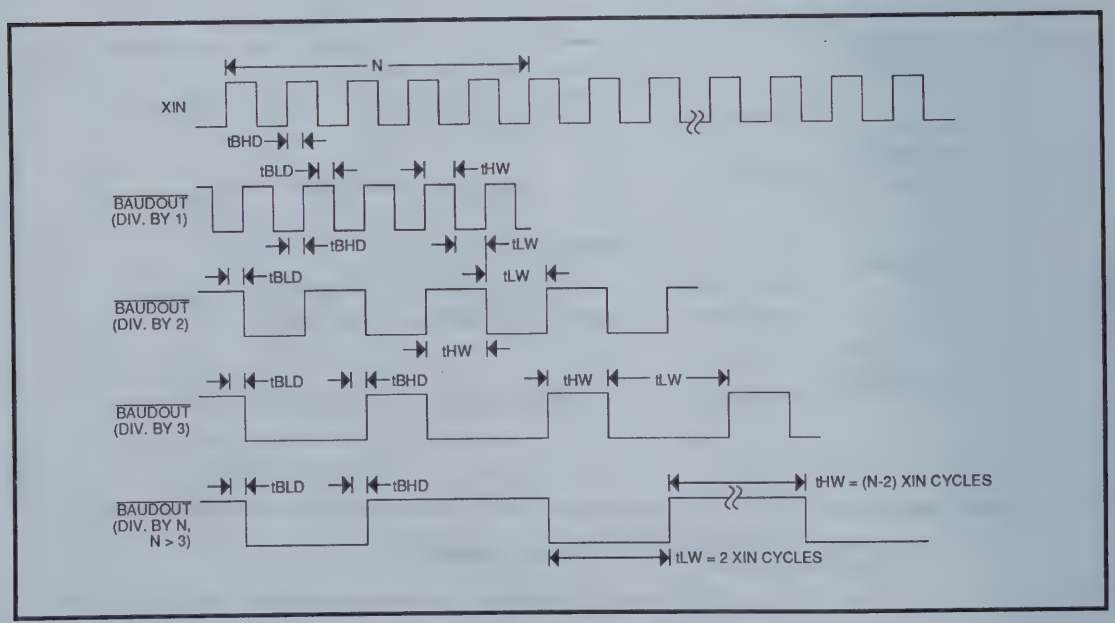


FIGURE 8: $\overline{\text{BAUDOUT}}$ Timing

AC CHARACTERISTICS (Continued)

RECEIVER (Refer to Figure 9.)

PARAMETER		CONDITIONS	MIN	MAX	UNITS
tSCD	Delay from RCLK to Sample Time			2	µs
tSINT	Delay from Stop to Set Interrupt	RCLK=tXH & tXL		1	RCLK cycles
tRINT	Delay from RD, $\overline{RD}$ (RD RBR/RDLSR) to Reset Interrupt	100 pF load		1	µs

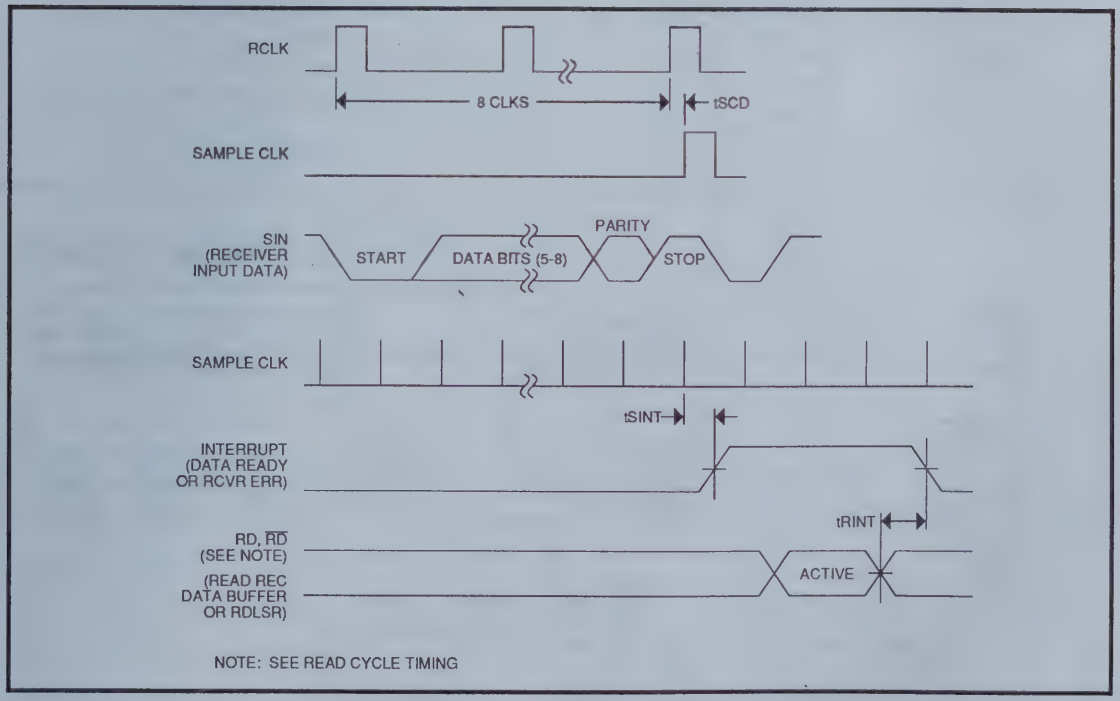


FIGURE 9: Receiver Timing

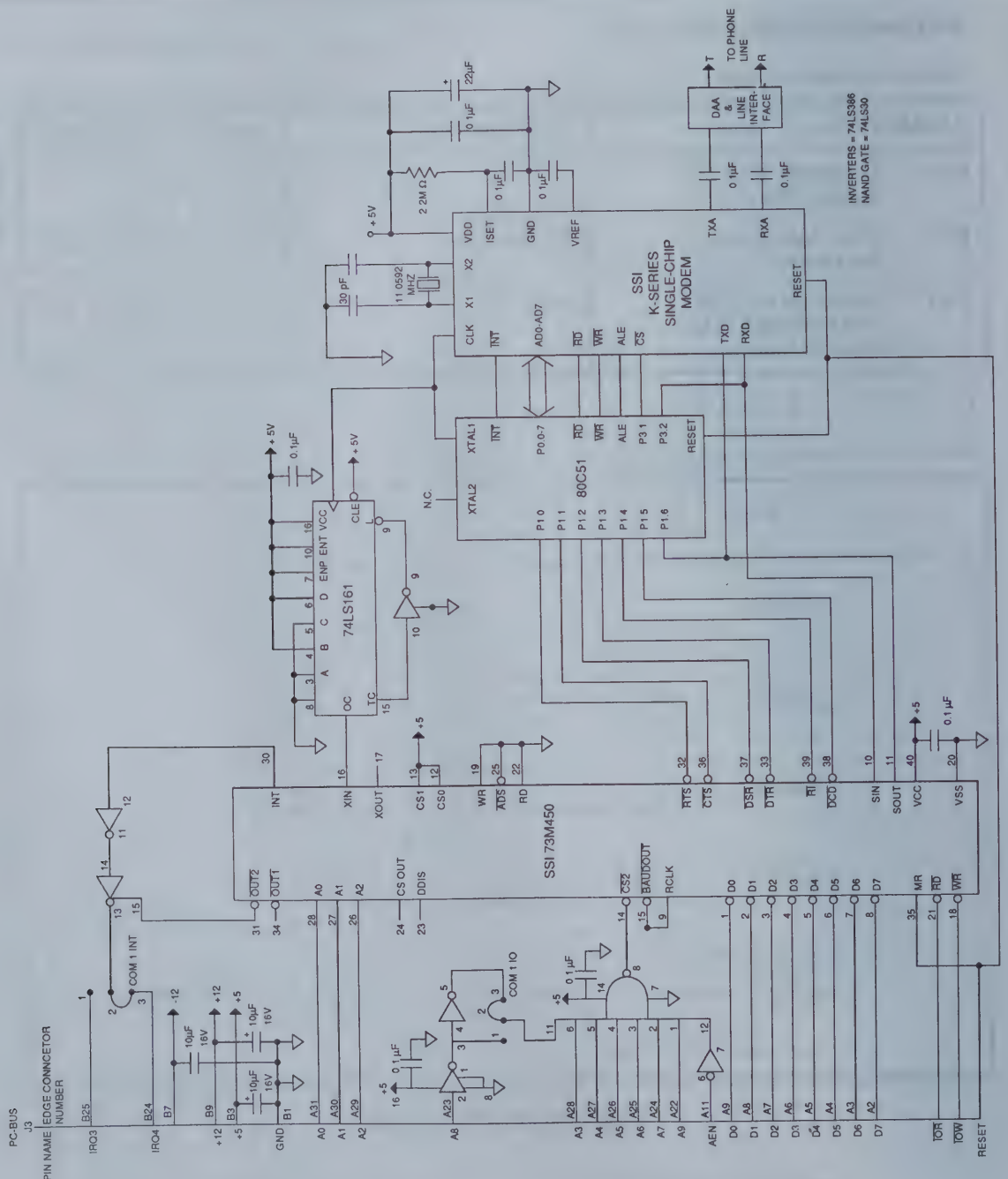
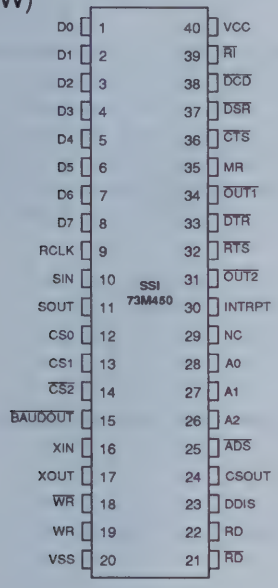
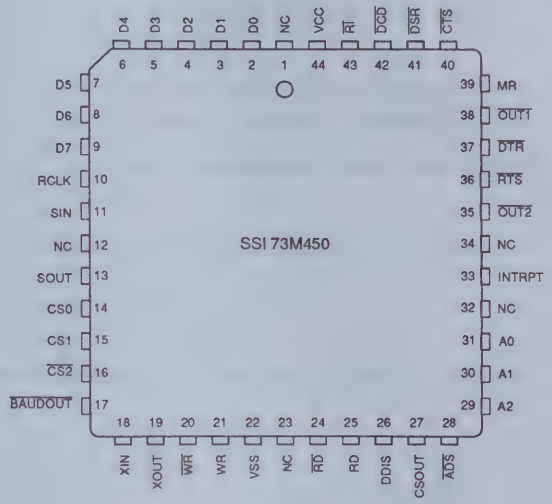


FIGURE 10: Typical Application Showing Modem Interface To PC-Bus Via SSI 73M450 UART

PACKAGE PIN DESIGNATIONS
(TOP VIEW)



40 - Pin DIP



44 - Pin PLCC

ORDERING INFORMATION

PART DESCRIPTION		ORDER NO.	PKG. MARK
SSI 73M450	40-pin PDIP	SSI 73M450-IP	73M450-IP
	44-pin PLCC	SSI 73M450-IH	73M450-IH
SSI 73M450F	40-pin PDIP	SSI 73M450F-IP	73M450F-IP
	44-pin PLCC	SSI 73M450F-IH	73M450F-IH

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SSI 73M450L/450LF
Universal Asynchronous Receiver/Transmitter

July, 1989

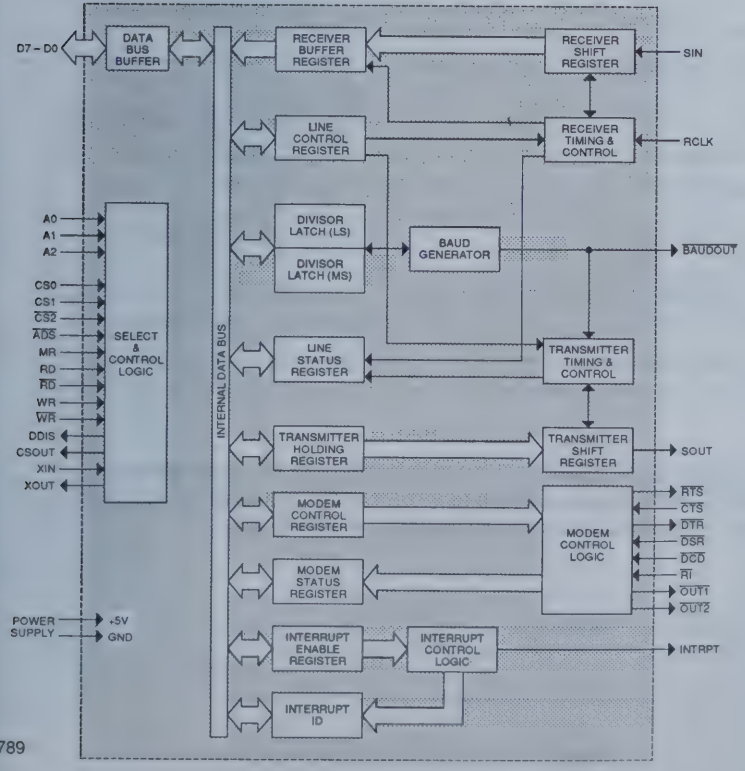
DESCRIPTION

The SSI 73M450L is an enhanced version of the SSI 73M450 Universal Asynchronous Receiver/Transmitter (UART). The enhancement allows the chip to be placed into low-power operation by shutting off the crystal oscillator. The SSI 73M450LF is a fast version of the chip. Both versions require a single 5V supply, and are available in 40-pin DIP and 44-pin PLCC.

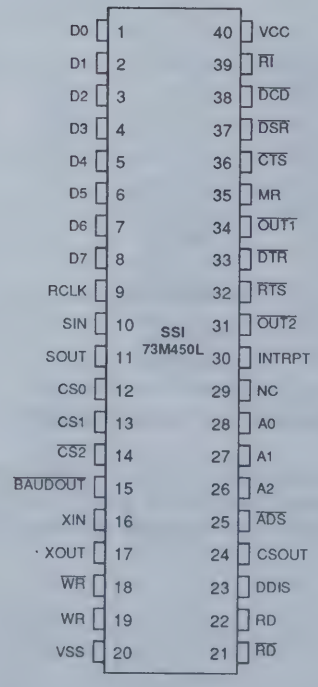
FEATURES

- **Pin and register compatible with the SSI 73M450/450F**
- **Bit programmable oscillator disable provides a shut-down mode while retaining memory**
- **High drive current for directly driving large loads**
- **Available in 40-pin DIP and 44-pin PLCC**

BLOCK DIAGRAM



PIN DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

0789

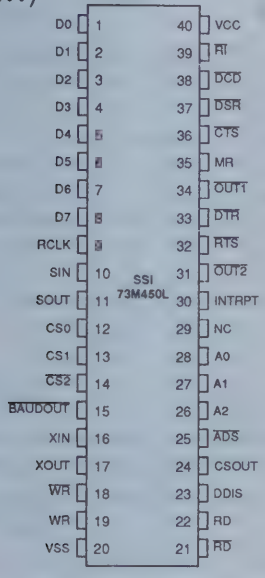
CONTROL REGISTER OVERVIEW

REGISTER		REGISTER ADDRESS (A2-A0) & DLAB	DATA BIT NUMBER D7	D6	D5	D4	D3	D2	D1	D0
RECEIVER BUFFER REGISTER (READ ONLY)	RBR	000 DLAB = 0	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
TRANSMIT HOLDING REGISTER (WRITE ONLY)	THR	000 DLAB = 0	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
INTERRUPT ENABLE REGISTER	IER	001 DLAB = 0	0	0	SSI MODE	0	ENABLE MODEM STATUS INTERRUPT	ENABLE REC. LINE STATUS INTERRUPT	ENABLE THR EMPTY INTERRUPT	ENABLE REC. DATA AVAILABLE INTERRUPT
INTERRUPT ID REGISTER (READ ONLY)	IIR	010 DLAB = X	0	0	0	0	0	INTERRUPT ID BIT 1	INTERRUPT ID BIT 0	"0" IF INTERRUPT PENDING
LINE CONTROL REGISTER	LCR	011 DLAB = X	DIVISOR LATCH ACCESS (DLAB)	SET BREAK	STICK PARITY	EVEN PARITY SELECT (EPS)	PARITY ENABLE (PEN)	NUMBER OF STOP BITS (STB)	WORD LENGTH SELECT 1 (WLS1)	WORD LENGTH SELECT 0 (WLS0)
MODEM CONTROL REGISTER	MCR	100 DLAB = X	OSC OFF	0	0	LOOP	OUT2	OUT1	REQUEST TO SEND (RTS)	DATA TERMINAL READY (DTR)
LINE STATUS REGISTER	LSR	101 DLAB = X	0	TRANSMIT-TER EMPTY (TEMT)	TRANSMIT HOLDING REGISTER EMPTY(THRE)	BREAK INTERRUPT (BI)	FRAMING ERROR (FE)	PARITY ERROR (PE)	OVERRUN ERROR (OE)	DATA READY (DR)
MODEM STATUS REGISTER (READ ONLY)	MSR	110 DLAB = X	DATA CARRIER DETECT (DCD)	RING INDICATOR (RI)	DATA SET READY (DSR)	CLEAR TO SEND (CTS)	DELTA DATA CARR. DETECT (DDCD)	TRAILING EDGE RING INDICATOR (TERI)	DELTA DATA SET READY (DDSR)	DELTA CLEAR TO SEND (DCTS)
SCRATCH REGISTER	SCR	111 DLAB = X	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DIVISOR LATCH (LS)	DLL	000 DLAB = 1	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DIVISOR LATCH (MS)	DLM	001 DLAB = 1	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8

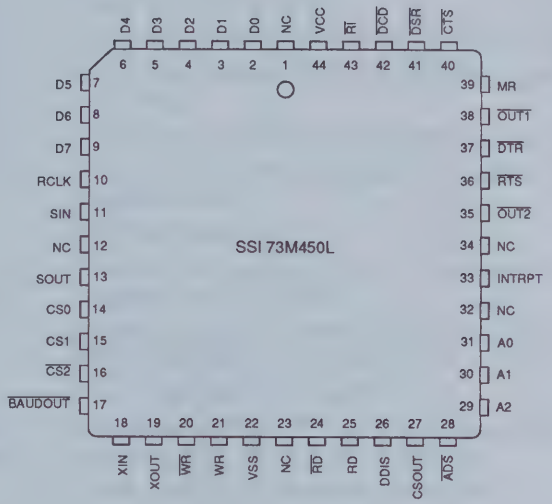
POWER SHUT-DOWN OPERATION

The oscillator of the SSI 73M450L/450LF is placed into power shut-down by setting bits D5 of the Interrupt Enable Register (IER) and D7 of the Modem Control Register (MCR) to a "1." During shut-down, the contents of all registers are retained. Resetting bit D7 of the MCR returns the chip to normal operation.

PACKAGE PIN DESIGNATIONS
(TOP VIEW)



40 - Pin DIP



44 - Pin PLCC

ORDERING INFORMATION

PART DESCRIPTION		ORDER NO.	PKG. MARK
SSI 73M450L	40-pin PDIP	SSI 73M450L-IP	73M450L-IP
	44-pin PLCC	SSI 73M450L-IH	73M450L-IH
SSI 73M450LF	40-pin PDIP	SSI 73M450LF-IP	73M450LF-IP
	44-pin PLCC	SSI 73M450LF-IH	73M450LF-IH

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NOTES:

SSI 73M550/550F
Universal Asynchronous Receiver/Transmitter with FIFOs

July, 1989

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DESCRIPTION

The SSI 73M550 is a Universal Asynchronous Receiver/Transmitter (UART) with receive and transmit FIFO buffers. The 16-byte FIFO registers are active during the FIFO mode, allowing the UART to reduce CPU overhead and accomodate Direct Memory Access (DMA) transfers. This mode is supported by interrupt functions and selectable interrupt trigger levels in both the RCVR and TXMR FIFO.

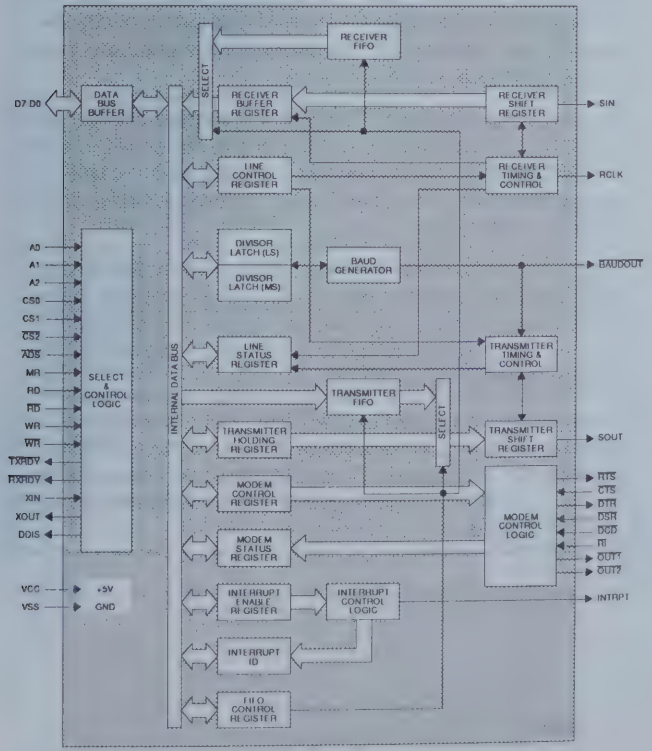
The 73M550 is functionally identical to the SSI 73M450 in the CHARACTER mode. Pins 24 (CSOUT) and 29

(Continued)

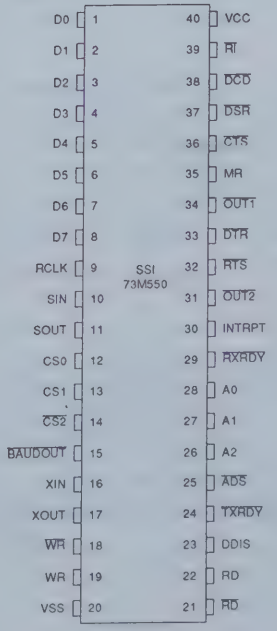
FEATURES

- **16 bytes of receive and transmit FIFO buffering available in FIFO mode reduces CPU overhead**
- **Supports DMA transfers with $\overline{\text{TXRDY}}$ and $\overline{\text{RXRDY}}$ pins**
- **Backwards-compatible with the 73M450 in CHARACTER mode**
- **Oscillator disable allows a static low-power state**
- **Bit-programmable high impedance state of INTRPT pin**
- **High drive current for directly driving large loads**
- **High speed version available with faster timing specifications**
- **Full double buffering**
- **Independent control transmit, receive, line status and data set interrupts**
- **Contains modem control functions including $\overline{\text{CTS}}$, $\overline{\text{TRS}}$, $\overline{\text{DSR}}$, $\overline{\text{DTR}}$, $\overline{\text{RI}}$ and $\overline{\text{DCD}}$**
- **Full status reporting capabilities**
- **Available in 40-pin DIP, 44-pin PLCC and special versions in 28-pin DIP and PLCC**
- **CMOS design for low-power operation**

BLOCK DIAGRAM



PIN DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

DESCRIPTION (Continued)

(NC) of the 73M450 have been replaced by $\overline{\text{TXRDY}}$ and $\overline{\text{RXRDY}}$, respectively on the 73M550. The chip is automatically put into the CHARACTER mode upon power-up, and subsequent mode changes are accomplished via software control.

The 73M550F is a fast version of the UART for higher performance applications. All versions are designed in CMOS for low-power consumption, and require a single 5V supply. The 73M550 and 73M550F are available in 40-pin DIP and 44-pin PLCC, and also space-saving 28-pin DIP and PLCC versions.

PIN DESCRIPTION

BUS INTERFACE

NAME	DIP	PLCC	TYPE	DESCRIPTION
$\overline{\text{ADS}}$	25	28	I	Address Strobe: The rising edge of this signal is used for latching the Register Address and Chip Select inputs, thus facilitating interface to a multiplexed Address/Data bus. $\overline{\text{ADS}}$ is also required when register address signals (A2, A1, A0) are not stable for the duration of the read or write cycle. If not required, $\overline{\text{ADS}}$ should be tied permanently low.
CS0, CS1, $\overline{\text{CS2}}$	12-14	14-16	I	Chip Select: The UART is selected when CS0 and CS1 are high and $\overline{\text{CS2}}$ is low. Chip selection is complete when the decoded chip select signal is latched with the rising edge of an active (low) $\overline{\text{ADS}}$ input. This enables communication between the UART and the CPU. If $\overline{\text{ADS}}$ is permanently low, then chip select should be stabilized for the duration of the tCSW parameter.
A0-A2	28-26	31-29	I	Register Select Address: These pins determine which of the UART registers is being selected during a read or write on the UART Data Bus. The contents of the DLAB bit in the UART's Line Control Register (see Table 1) also controls which register is referenced.
RD, $\overline{\text{RD}}$	22,21	25,24	I	Read Strobe: A request to read status information or data from a selected register may be made by pulling RD high or $\overline{\text{RD}}$ low while the chip is selected. Since only one input is required for a read, tie either RD permanently low or $\overline{\text{RD}}$ permanently high if not used.
WR, $\overline{\text{WR}}$	19, 18,	21, 20	I	Write Strobe: A request to write control words or data into a selected register may be made by pulling WR high or $\overline{\text{WR}}$ low while the chip is selected. Since only one input is required for a write, tie either WR permanently low or $\overline{\text{WR}}$ permanently high if not used.

BUS INTERFACE (Continued)

NAME	DIP	PLCC	TYPE	DESCRIPTION
D0-D7	1-8	2-9	I/O	UART Data Bus (three-state): This bus provides bi-directional communications between the UART and the CPU; data control words and status information are transferred via this bus.
$\overline{\text{TXRDY}}$	1-8	2-9	I/O	Transmitter Ready Signal for DMA Transfer: Remains low as long as XMIT FIFO is not completely full. In FIFO mode, DMA transfer modes 0 and 1 are allowed. In the character mode, only DMA transfer mode 0 is allowed. DMA mode 0 supports single DMA transfer mode between CPU bus cycles. DMA mode 1 supports multiple DMA transfers until the XMIT FIFO has been filled.
$\overline{\text{RXRDY}}$	29		O	Receiver Ready Signal for DMA Transfer: Remains low until RCVR FIFO has been emptied. In FIFO mode DMA transfer modes 0 and 1 are allowed. In the character mode only DMA mode 0 is allowed. DMA mode 0 supports single DMA transfer made between CPU bus cycles. DMA mode 1 supports multiple DMA transfers until the RCVR FIFO has been emptied.
DDIS	23	26	O	Driver Disable: Goes low when the CPU is reading data from the UART. A high-level DDIS output can be used to disable an external transceiver (if used between the CPU and UART on the D0-D7 Data Bus) at all times, except when the CPU is reading data.
INTRPT	30	33	O	Interrupt: Goes high whenever any one of the following interrupt types has an active high condition and is enabled via the IER: Receiver Error Flag, Received Data Available; Timeout (FIFO mode only); Transmitter Holding Register Empty and Modem Status. The INTRPT signal is reset low upon the appropriate interrupt service or a Master Reset operation.

DATA I/O

NAME	DIP	PLCC	TYPE	DESCRIPTION
SIN	10	11	I	Serial Input: Input for serial data from the communications link (peripheral device, modem or data set).
SOUT	11	13	O	Serial Output: Output for serial data to the communications link (peripheral device,modem or data set). This signal is set high upon a Master Reset.

MODEM CONTROL

NAME	DIP	PLCC	TYPE	DESCRIPTION
$\overline{RTS}$	32	36	O	Request To Send: This output is programmed by $\overline{RTS}$ bit (D1) of the Modem Control Register and represents the compliment of that bit. I is used in modem handshaking to signify that the UART has data to transmit. This signal is set high upon Master Reset or during loop mode operation.
$\overline{CTS}$	36	40	I	Clear To Send: A modem status input whose condition corresponds to the complement of the CTS bit (D4) of the Modem Status Register. When $\overline{CTS}$ is low, it indicates that communications have been established and that data may be transmitted.
$\overline{DTR}$	33	37	O	Data Terminal Ready: This output is programmed by DTR bit (D0) of the Modem Control Register, and represents the compliment of that bit. It is used in modem handshaking to signify that the UART is available to communicate. This signal is set high upon Master Reset or during loop mode operation.
$\overline{DSR}$	37	41	I	Data Set Ready: A modem status input whose condition is complimented and reflected in the DSR bit (D5) of the Modem Status Register. When $\overline{DSR}$ is low, it indicates that the modem is ready to establish communications.
$\overline{DCD}$	38	42	I	Data Carrier Detect: A modem status input whose condition is complemented and reflected in the DCD bit (D7) of the Modem Status Register. When $\overline{DCD}$ is low, it indicates that the modem is receiving a carrier.
$\overline{RI}$	39	43	I	Ring Indicator: A modem status input whose condition is complimented and reflected in the RI bit (D6) of the Modem Status Register. When $\overline{RI}$ is low, it indicates that a telephone ringing signal is being received.
$\overline{OUT1}$ $\overline{OUT2}$	34 31	38 35	O O	Output 1, 2: User designated outputs that can be set to an active low by setting bit 2 ($\overline{OUT1}$) or bit 3 ($\overline{OUT2}$) of the Modem Control Register high. These output signals are set high upon Master Reset or during loop mode operation.

GENERAL & CLOCKS

NAME	DIP	PLCC	TYPE	DESCRIPTION
VCC	40	44	I	+5V Supply, ±10%: Bypass with 0.1 µF capacitor to VSS.
VSS	20	22	I	System Ground
MR	35	39	I	Master Reset: When high, this input clears all UART control logic and registers, except for the Receiver Buffer, Transmitter Holding and Divisor Latches; also, the state of output signals SOUT, INTRPT, $\overline{OUT1}$, $\overline{OUT2}$, $\overline{RTS}$ and $\overline{DTR}$ are affected by an active MR input. This input is buffered with a TTL-compatible Schmitt Trigger. See Table 2.
XIN, XOUT	16,17	18,19	I/O	External System Clock I/O: These two pins connect the main timing reference (crystal or signal clock) to the UART. Additionally, XIN may be driven by an external clock source.
RCLK	9	10	I	Receiver Clock: This input is the 16X baud rate clock for the receiver section of the chip.
$\overline{BAUDOUT}$	15	17	O	Baud Generator Output: 16X clock signal for the transmitter section of the UART. The clock is equal to the main reference oscillator frequency divided by the specified divisor in the Baud Generator Divisor Latches. May also be used for the receiver section by tying this output to the RCLK input of the chip.
N/C		1,12 23, 34	-	No Connection: These pins have no internal connection and may be left floating.

TABLE 1: Control Register Address Table

DLAB	A2	A1	A0	REGISTER
0	0	0	0	Receiver Buffer (read), Transmitter Holding Register (write)
0	0	0	1	Interrupt Enable
X	0	1	0	Interrupt Identification (read only)
X	0	1	0	FIFO Control (write)
X	0	1	1	Line Control
X	1	0	0	Modem Control
X	1	0	1	Line Status
X	1	1	0	Modem Status
X	1	1	1	Scratch
1	0	0	0	Divisor Latch (least significant byte)
1	0	0	1	Divisor Latch (most significant byte)

TABLE 2: UART Reset Functions

REGISTER/SIGNAL	RESET CONTROL	RESET STATE
Interrupt Enable Register	Master Reset	All bits low (0-3 & 5 forced and 4, 6 & 7 permanent)
Interrupt Identification Register	Master Reset	Bit 0 is high; bits 1, 2, 3, 6 & 7 are low; bits 4 & 5 are permanently low
Line Control Register	Master Reset	All bits low
Modem Control Register	Master Reset	All bits low (bits 5, 6 & 7 permanent)
Line Status Register	Master Reset	All bits low, except bits 5 & 6 are high
Modem Status Register	Master Reset	Bits 0-3 are low; bits 4-7 = input signal
SOUT	Master Reset	High
INTRPT (RCVR Errs)	Read LSR/MR	Low
INTRPT (RCVR Data Ready)	Read RBR/MR	Low
INTRPT (THRE)	Read IIR/Write THR/MR	Low
INTRPT (Modem Status Changes)	Read MSR/MR	Low
$\overline{OUT2}$	Master Reset	High
$\overline{RTS}$	Master Reset	High
$\overline{DTR}$	Master Reset	High
$\overline{OUT1}$	Master Reset	High
FIFO Control Register	Master Reset	All bits low
RCVR FIFO	MR/FCR1 and FCR0/ΔFCR0	All bits low
XMIT FIFO	MR/FCR2 and FCR0/ΔFCR0	All bits low

CONTROL REGISTER OVERVIEW

REGISTER		REGISTER ADDRESS (A2-A0) & DLAB	DATA BIT NUMBER D7	D6	D5	D4	D3	D2	D1	D0
RECEIVER BUFFER REGISTER (READ ONLY)	RBR	000 DLAB=0	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
TRANSMIT HOLDING REGISTER (WRITE ONLY)	THR	000 DLAB=0	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
INTERRUPT ENABLE REGISTER (READ ONLY)	IER	001 DLAB=0	0	0	ENABLE SSI MODE (NOTE 1)	0	ENABLE MODEM STATUS INTERRUPT	ENABLE REC. LINE STATUS INTERRUPT	ENABLE THR EMPTY INTERRUPT	ENABLE REC. DATA AVAILABLE INTERRUPT
INTERRUPT ID REGISTER (READ ONLY)	IIR	010 DLAB=X	FIFOs ENABLED (NOTE 1)	FIFOs ENABLED (NOTE 1)	SSI MODE RXRDY FOR DMA	SSI MODE TXRDY FOR DMA	INTERRUPT ID BIT 2 (NOTE 1)	INTERRUPT ID BIT 1	INTERRUPT ID BIT 0	"0" IF INTERRUPT PENDING
FIFO CONTROL REGISTER (WRITE ONLY)	FCR	010 DLAB=X	RCVR TRIGGER (MSB)	RCVR TRIGGER (LSB)	SSI MODE XMIT TRIGGER (MSB)	SSI MODE XMIT TRIGGER (LSB)	DMA MODE SELECT	XMIT FIFO RESET	RCVR FIFO RESET	FIFO ENABLE
LINE CONTROL REGISTER	LCR	001 DLAB=X	DIVISOR LATCH ACCESS (DLAB)	SET BREAK	STICK PARITY	EVEN PARITY SELECT (EPS)	PARITY ENABLE (PEN)	NUMBER OF STOP BITS (STB)	WORD LENGTH SELECT 1 (WLS1)	WORD LENGTH SELECT 0 (WLS0)
MODEM CONTROL REGISTER	MCR	100 DLAB=X	SSI MODE OSC OFF	0	0	LOOP	OUT 2	OUT 1	REQUEST TO SEND (RTS)	DATA TERMINAL READY (DTR)
LINE STATUS REGISTER	LSR	101 DLAB=X	ERROR IN RCVR FIFO (NOTE 1)	TRANS-MITTER EMPTY (TEMT)	TRANSMIT HOLDING REGISTER EMPTY(THRE)	BREAK INTERRUPT (BI)	FRAMING ERROR (FE)	PARITY ERROR (PE)	OVERRUN ERROR (OE)	DATA READY (DR)
MODEM STATUS REGISTER (READ ONLY)	MSR	110 DLAB=X	DATA CARRIER DETECT (DCD)	RING INDICATOR (RI)	DATA SET READY (DSR)	CLEAR TO SEND (CTS)	DELTA DATA CARR. DETECT (DDCD)	TRAILING EDGE RING INDICATOR (TERI)	DELTA DATA SET READY (DDSR)	DELTA CLEAR TO SEND (DCTS)
SCRATCH REGISTER	SCR	111 DLAB=X	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DIVISOR LATCH (MS)	DLL	000 DLAB=1	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DIVISOR LATCH (MS)	DLM	001 DLAB=1	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8

NOTE 1: THESE BITS ARE RESET TO 0 IN THE 73M450 MODE (Character Mode)

REGISTER BIT DESCRIPTIONS

RECEIVER BUFFER REGISTER (RBR) (READ ONLY)
UART ADDRESS: A2 - A0 = 000, DLAB = 0

This read only register contains the parallel received data with start, stop, and parity bits (if any) removed. The high order bits for less than 8 data bits/character will be set to 0.

TRANSMIT HOLDING REGISTER (THR) (WRITE ONLY)
UART ADDRESS: A2 - A0 = 000, DLAB = 0

This write only register contains the parallel data to be transmitted. The data is sent LSB first with start, stop, and parity bits (if any) added to the serial bit stream as the data is transferred.

INTERRUPT ENABLE REGISTER (IER)
UART ADDRESS: A2 - A0 = 001, DLAB = 0

This 8-bit register enables the five types of interrupts of the UART to separately activate the chip Interrupt (INTRPT) output signal. It is possible to totally disable the interrupt system by resetting bits 0 through 3 of the Interrupt Enable Register. Similarly, by setting the appropriate bits of this register to a logic 1, selected interrupts can be enabled. Disabling the interrupt system inhibits the Interrupt Identification Register and the active (high) INTRPT output from the chip. All other system functions operate in their normal manner, including the setting of the Line Status and Modem Status Registers.

BIT	NAME	COND	DESCRIPTION
D0	Received Data	1	When set to logic 1 this bit enables the Received Data Available Interrupt, and timeout interrupts in FIFO mode.
D1	Transmitter Holding Register Empty	1	When set to logic 1 this bit enables the Transmitter Holding Register Empty Interrupt.
D2	Receiver Line Status Interrupt	1	When set to logic 1 this bit enables the Receiver Line Status Interrupt.
D3	Modem Status	1	When set to logic 1 this bit enables the Modem Status Interrupt.
D4	Not Used	0	This bit are is always logic 0.
D5	SSI Mode	1	When set to logic 1, this bit enables the SSi Mode. In the SSi Mode the oscillator can be turned off via bit D7 in the Modem Control Register, and the XMIT THRE interrupt trigger set via bits D4 & D5 of the FIFO Control Register.
D6-D7	Not used	0	These two bits are always logic 0.

INTERRUPT ID REGISTER (IIR) (READ ONLY)
UART ADDRESS: A2 - A0 = 010

The IIR register gives prioritized information as to the status of interrupt conditions and also allows for DMA transfer operations in a polled FIFO manner under the SSi mode. When accessed, the IIR freezes the highest priority interrupt pending and no other interrupts are acknowledged until the particular interrupt is serviced by the CPU. The order of interrupt priorities is shown in the table below.

BIT	NAME	COND	DESCRIPTION
D0	Interrupt Pending	0	This bit can be used in either a prioritized interrupt or polled environment to indicate whether an interrupt is pending. When bit 0 is a logic 0, an interrupt is pending and the IIR contents may be used as a pointer to the appropriate interrupt service routine.
		1	When bit 0 is a logic 1, no interrupt is pending.
D1, D2 D3	Interrupt ID bits 0, 1, 2	See table Page 10	These three bits of the IIR are used to identify the highest priority interrupt pending as indicated in the following table. Bit D3 is reset to 0 when FIFO mode is disabled.
D4	SSI mode TXRDY for DMA	1	This bit function is available only when SSi mode is enabled (bit D5 in IER is set). This bit is the compliment of $\overline{\text{TXRDY}}$ pin and is used to support DMA transfers in a polled environment. A logic 1 indicates transmitter is less than full and is ready for DMA transfer.
		0	A logic 0 indicates transmitter is full and not ready for DMA transfer. Also when SSI mode is disabled this bit will be reset to 0.
D5	SSI mode RXRDY for DMA	1	This bit function is available only when SSi mode is enabled (bit D5 in IER is set). This bit is the compliment of $\overline{\text{RXRDY}}$ pin and is used to support DMA transfers in a polled environment. A logic 1 indicates receiver is not empty and is ready for DMA transfer.
		0	A logic 0 indicates receiver is empty and not ready for DMA transfer. Also when SSi mode is disabled this bit will be reset to 0.
D6, D7	FIFOS enabled	1	These two bits are set to logic 1 when bit D0 in FCR is set to 1 (FIFO mode enabled).
		0	These two bits are reset to logic 0 when bit D0 in FCR is reset to 0 (FIFO mode disabled).

INTERRUPT PRIORITY TABLE

D3	D2	D1	D0	PRIORITY	TYPE	SOURCE	RESET
0	0	0	1	–	None	None	N/A
0	1	1	0	Highest	Receiver Line Status	Overrun Error, Parity Error, Framing Error or Break Interrupt	Reading the Line Status Register
0	1	0	0	Second	Receive Data Available	Receive Data Available or RCVR FIFO trigger level reached	Reading the Receiver Buffer Register or the RCVR FIFO drops below trigger level
1	1	0	0	Second	Character Timeout Indicator	No characters have been removed from or input to the RCVR FIFO during the last 4 character times and there is at least 1 character in it during this time	Reading the Receiver Buffer Register
0	0	1	0	Third	Transmit Holding Register Empty	Transmit Holding Register Empty or below XMIT FIFO trigger level	Reading IIR Register (if source of interrupt) or Writing to Transmit Holding Register or XMIT FIFO trigger level reached
0	0	0	0	Fourth	Modem Status	Clear to Send or Data Set Ready or Ring Indicator or Data Carrier Detect	Reading the Modem Status Register

FIFO CONTROL REGISTER (FCR) (WRITE ONLY)
UART ADDRESS: A2 - A0 = 010

This is a write only register at the same location as the IIR read only Register. This register is used to enable the FIFOs, clear the FIFOs, set the XMIT and RCVR FIFO trigger level, and select the type of DMA signalling.

BIT	NAME	COND	DESCRIPTION
D0	FIFO Enable	1	Setting this bit to logic 1 enables both XMIT and RCVR FIFOs. This bit must be written as 1 when other FCR bits are written to or they will not be programmed.
		0	Resetting this bit to logic 0 disables the FIFO mode (enables the 73M450 mode) and clears data in both FIFOs when changing from FIFO mode to 73M450 mode and vice versa, data is automatically cleared from FIFOs.
D1	RCVR FIFO Reset	1	Setting this bit to logic 1 clears all data in the RCVR FIFO and resets its counter logic to 0. The shift register is not cleared. The logic 1 written into this bit is self clearing.
D2	XMIT FIFO Reset	1	Setting this bit to logic 1 clears all data in the XMIT FIFO and resets its counter logic to 0. The shift register is not cleared. The logic 1 written into this bit is self clearing.

FIFO CONTROL REGISTER (FCR) (WRITE ONLY) (Continued)

BIT	NAME	COND	DESCRIPTION
D3	DMA Mode Select	1	Setting this bit to logic 1 will enable DMA mode 1. In this mode pins $\overline{TXRDY}$ and $\overline{RXRDY}$ and bits D4 and D5 in IIR, support multiple DMA transfers.
		0	Resetting this bit to logic 0 will enable DMA mode 0. In this mode, pins $\overline{TXRDY}$ and $\overline{RXRDY}$ and bits D4 and D5 in IIR support single DMA transfers.
D5, D4	SSI Mode XMIT Trigger (MSB, LSB)	0/1	These two bits are active in the SSi mode only. The value written into D5 and D4 determine the XMIT FIFO trigger level as described in table below. The THRE interrupt will occur if the XMIT FIFO is below the trigger level and will reset when the XMIT FIFO is filled to trigger level.
D7, D6	RCVR Trigger (MSB, LSB)	0/1	The value written into D7 and D6 determining the RCVR FIFO trigger level as described in table below. The received data available interrupt will occur if the RCVR FIFO is filled to or above the trigger level and will reset when the RCVR FIFO drops below the trigger level.

D5	D4	XMIT FIFO Trigger Level (Bytes)
0	0	01
0	1	04
1	0	08
1	1	14

D7	D6	RCVR FIFO Trigger Level (Bytes)
0	0	01
0	1	04
1	0	08
1	1	14

LINE CONTROL REGISTER (LCR)
UART ADDRESS: A2 - A0 = 011

The user specifies the format of the asynchronous data communications exchange via the Line Control Register. In addition to controlling the format the user may retrieve the contents of the Line Control Register for inspection. This feature simplifies system programming and eliminates the need for separate storage in system memory of the line characteristics.

BIT	NAME	COND		DESCRIPTION
D0/D1	Word Length Select 0 (WLS0)			Bits D0 and D1 select the number of data bits per character as shown:
	Word Length Select 1 (WLS1)	D1	D0	Word Length
		0	0	5 bits
		0	1	6 bits
		1	0	7 bits
		1	1	8 bits
D2	Number of Stop Bits (STB)	0 or 1		This bit specifies the number of stop bits in each transmitted character. If bit D2 is a logic 0, one stop bit is generated in the transmitted data. If bit D2 is a logic 1 when a 5-bit word length is selected via bits D0 and D1, one-and-a-half stop bits are generated. If bit D2 is a logic 1 when either a 6, 7, or 8-bit word length is selected, two stop bits are generated. The receiver checks the first stop bit only, regardless of the number of stop bits selected.
D3	Parity Enable (PEN)	1		This is the Parity Enable (PEN) bit. When set to a logic 1, a parity bit is generated (transmit data) or checked (receive data) between the last data word bit and stop bit of the serial data. (The parity bit is used to produce an even or odd number of 1's when the data word bits and the parity bit are summed).
D4	Even Parity Select (EPS)	1 or 0		This is the Even Parity Select (EPS) bit. When bit D3 is a logic 1 and bit D4 is a logic 0, an odd number of logic 1's is transmitted or checked in the data word bits and parity bit. When bit D3 is a logic 1 and bit D4 is a logic 1 an even number of logic 1's is transmitted or checked.
D5	Stick Parity	1 or 0		This is the Stick Parity bit. When bit D3 is a logic 1 and bit D5 is a logic 1 the parity bit is transmitted and checked by the receiver as a logic 0 if bit D4 is a logic 1 or as a logic 1 if bit D4 is a logic 0.
		D5	D4	Parity
		0	0	ODD Parity
		0	1	EVEN Parity
		1	0	MARK Parity
		1	1	SPACE Parity

LINE CONTROL REGISTER (LCR) (Continued)

BIT	NAME	COND	DESCRIPTION
D6	Set Break	1	This is the Break Control bit. It causes a break condition to be sent to the receiving UART. When set to a logic 1 the serial out (SOUT) is forced to a logic 0 state. The break is disabled by setting bit D6 to a logic 0. This bit acts only on SOUT and has no effect on the transmitter logic. See note below.
D7	Divisor Latch Access Bit (DLAB)	1	The Divisor Latch Access Bit (DLAB) must be set high (logic 1) to access the Divisor Latches of the baud generator during a Read or Write operation. It must be set low (logic 0) to access the Receiver Buffer, the Transmitter Holding Register, or the Interrupt Enable Register.

NOTE: This feature enables the CPU to alert a terminal in a computer communications system. If the following sequence is followed, no erroneous or extraneous characters will be transmitted because of the break.

1. Load an all 0's pad character in response to THRE.
2. Set break in response to the next THRE.
3. Wait for the Transmitter to be idle. (TEMT = 1), and clear break when normal transmission has to be restored.

During the break, the Transmitter can be used as a character timer to accurately establish the break duration.

MODEM CONTROL REGISTER (MCR)
UART ADDRESS: A2 - A0 = 100

The Modem Control Register controls the interface with the modem, data set or peripheral device.

BIT	NAME	COND	DESCRIPTION
D0	DTR	1	This bit controls the Data Terminal Ready ($\overline{DTR}$) output. When bit 0 is set to a logic 1 the $\overline{DTR}$ output is forced to a logic 0. When bit 0 is reset to a logic 0 the $\overline{DTR}$ output is forced to a logic 1.
D1	RTS	1	This bit controls the Request to Send ($\overline{RTS}$) output. When bit 1 is set to a logic 1 the $\overline{RTS}$ output is forced to a logic 0. When bit 1 is reset to a logic 0 the $\overline{RTS}$ output is forced to a logic 1.
D2	OUT1	1	This bit controls the Output 1 ($\overline{OUT1}$) signal, which is an auxiliary user-designated output. When bit D2 is set to a logic 1 the $\overline{OUT1}$ output is forced to a logic 0. When bit D2 is reset to a logic 0 the $\overline{OUT1}$ output is forced to a logic 1.
D3	OUT2	0	This bit controls the Output 2 ($\overline{OUT2}$) signal which is an auxiliary user-designated output. When bit D3 is set to a logic 1 the $\overline{OUT2}$ output is forced to a logic 0. When bit D3 is reset to a logic 0 $\overline{OUT2}$ output is forced to a logic 1.

MODEM CONTROL REGISTER (MCR) (Continued)

BIT	NAME	COND	DESCRIPTION
D4	LOOP	1	This bit provides a local loopback feature for diagnostic testing of the UART. When bit 4 is set to logic 1, the following occurs: the transmitter Serial Output (SOUT) is set to the logic 1 state; the receiver Serial Input (SIN) is disconnected; the output of the Transmitter Shift Register is "looped back" into the Receiver Shift Register input; the four Modem Control inputs ($\overline{CTS}$, $\overline{DSR}$, $\overline{DCD}$ and $\overline{RI}$) are disconnected; the four Modem Control outputs ($\overline{DTR}$, $\overline{RTS}$, $\overline{OUT1}$ and $\overline{OUT2}$) are internally connected to the four Modem Control inputs, and the Modem Control output pins are forced to their inactive state (high). In the diagnostic mode, data that is transmitted is immediately received. This feature allows the processor to verify the transmit and received-data paths of the UART. In the diagnostic mode, the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational, but the interrupts' sources are now the lower four bits of the Modem Control Register instead of the four Modem Control inputs. The interrupts are still controlled by the Interrupt Enable Register.
D5-D6		0	These bits are permanently set to logic 0.
D7	SSi Mode Osc. off	1	This bit is active in the SSi Mode only. When D7 is set the UART oscillator is tunred off placing the UART in a power shutdown state. All UART memory is retained during power shutdown.
		0	Resetting this bit enable the oscillator and powers up the UART.

LINE STATUS REGISTER (LSR)
UART ADDRESS: A2 - A0 = 101

This register provides status information to the CPU concerning the data transfer. Bits D1-D4 are the error conditions that produce a Receiver Line Status interrupt whenever any of the corresponding conditions are detected. The Line Status Register is intended for read operation only. Writing to this register is not recommended as this operation is used for factory testing.

BIT	NAME	COND	DESCRIPTION
D0	DR	0/1	The Data Ready (DR) bit is set to a 1 whenever a complete incoming character has been received and transferred into the Receiver Buffer Register. DR is reset to 0 by reading all data in the Receiver Buffer Register FIFO.
D1	OE	0/1	The Overrun Error (OE) bit is set when data in the Receiver Buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer Register, thereby destroying the previous character. OE is reset to 0 whenever the CPU reads the contents of the Line Status Register. In FIFO mode if data continues to fill the FIFO beyond the trigger level an overrun error will occur only after the FIFO is full and the next character has been completely received in (Continued)

LINE STATUS REGISTER (LSR) (Continued)

BIT	NAME	COND	DESCRIPTION
D1	OE	0/1	the shift register. OE is indicated to the CPU as soon as it occurs. The character in the shift register is overwritten but it is not transferred to the FIFO.
D2	PE	0/1	The Parity Error (PE) bit is set when the received character did not have the correct parity. PE is reset to 0 whenever the CPU reads the Line Status Register. In FIFO mode this error is revealed to the CPU when its associated character is at the top of the FIFO.
D3	FE	1	The Framing Error (FE) bit indicates that the received character did not have a valid stop bit. FE is reset to 0 whenever the CPU reads the contents of the Line Status Register. In the FIFO mode this error is revealed to the CPU when its associated character is at the top of the FIFO. The UART will try to resynchronize after a framing error. To do this it assumes that the framing error was due to the next start bit, so it samples the following start bit twice and then takes in the data that follows.
D4	BI	1	The Break Interrupt (BI) bit is set when a break has been received. A break occurs whenever the received data is held to 0 for a full data word (start + data + stop). BI is reset to 0 whenever the CPU reads the Line Status Register. In the FIFO mode this error is revealed to the CPU when its associated character is at the top of the FIFO. When break occurs only one zero character is loaded into the FIFO. The next character transfer is enabled after SIN goes to the marking (high) state and receives the next valid start bit.
D5	THRE	1	The Transmit Holding Register Empty (THRE) is set to a logic 1 when a character is transferred from the Transmit Holding Register into the Transmit Shift Register, indicating that the UART is ready to accept a new character for transmission. In addition this bit causes the UART to issue an interrupt to the CPU when the THRE Interrupt enable is set high. THRE is reset to 0 when the CPU loads a character into the Transmit Holding Register. In the FIFO mode this bit is set when the XMIT FIFO is filled below the trigger level and will reset when the FIFO is filled to the trigger level.
D6	TEMT	1	The Transmit Empty (TEMT) indicates that both the Transmit Holding Register and the Transmit Shift Registers are empty. TEMT is reset to 0 whenever the TSR or THR contains a data character. In the FIFO mode this bit is set whenever the XMIT FIFO and the transmitter shift register are both empty.
D7	Error in Rcvr FIFO	0	In the character mode this bit is reset to 0. In the FIFO mode this bit is set when there is at least one parity error, framing error or break indication in the FIFO. This bit is reset when the CPU reads the Line Status Register if there are no subsequent errors in the FIFO.
Note:	Bits D1-D4 are the error conditions that produce a Receiver Line Status interrupt whenever any of the corresponding conditions are detected and the interrupt is enabled.		

MODEM STATUS REGISTER (MSR) (READ ONLY)
UART ADDRESS: A2 - A0 = 110

This register provides the current state of the control signals from the modem or peripheral device. In addition four bits provide change information. Whenever bit D0, D1, D2 or D3 is set to logic 1 a Modem Status Interrupt is generated; reset to logic 0 occurs whenever they are read. In Loop Mode CTS, DSR, RI and DCD are taken from RTS, DTR, OUT1, and OUT2 in the Modem Control Register, respectively.

BIT	NAME	COND	DESCRIPTION
D0	DCTS	1	The Delta Clear to Send (DCTS) bit is set when the $\overline{CTS}$ input to the chip has changed state since the last time it was read by the CPU.
D1	DDSR	1	The Delta Data Set Ready (DDSR) bit is set when the $\overline{DSR}$ input to the chip has changed state since the last time it was read by the CPU.
D2	TERI	1	The Trailing Edge of the Ring Indicator (TERI) detect bit is set when the $\overline{RI}$ input to the chip has changed from an Off (logic 0) to an On (logic 1) condition.
D3	DDCD	1	The Delta Data Carrier Detect (DDCD) bit indicates that the $\overline{DCD}$ input to the chip has changed state.
D4	CTS	1	This bit is the complement of the Clear To Send ($\overline{CTS}$) input. If bit 4 (loop) of the MCR is set to a 1, this bit is equivalent to RTS in the MCR.
D5	DSR	1	This bit is the complement of the Data Set Ready ($\overline{DSR}$) input. If bit 4 of the MCR is set to a 1, this bit is the equivalent of DTR in the MCR.
D6	RI	1	This bit is the complement of the Ring Indicator ($\overline{RI}$) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to OUT1 in the MCR.
D7	DCD	1	This bit is the complement of the Data Carrier Detect ($\overline{DCD}$) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to OUT2 in the MCR.

SCRATCH REGISTER (SCR)
ADDRESS: A2 - A0 = 111

This 8-bit Read/Write Register does not control the UART in any way. It is intended as a scratchpad register to be used by the programmer to hold data temporarily.

DIVISOR LATCH (LS) (DLL)
ADDRESS: A2 - A0 = 000, DLAB = 1

This write-only register contains the least significant byte of the divisor which is used to control the rate of the programmable baud generator.

DIVISOR LATCH (MS) (DLM)
ADDRESS: A2 - A0 = 001, DLAB = 1

This write-only register contains the most significant byte of the divisor which is used to control the rate of the programmable baud generator.

PROGRAMMABLE BAUD GENERATOR

The UART contains a programmable Baud Generator that is capable of taking any clock input (DC to 8 MHz) and dividing it by any divisor from 2 to 2^{16}-1. 4 MHz is the highest input clock frequency recommended when the divisor = 1. The output frequency of the Baud Generator is 16 x the Baud [divisor # = (frequency input)/(baud rate x 16)]. Two 8-bit latches store the divisor in a 16-bit binary format. These Divisor Latches must be loaded during initialization in order to ensure desired operation of the Baud Generator. Upon loading either of the Divisor Latches, a 16-bit Baud counter is immediately loaded. This prevents long counts on initial load.

Tables 3, 4 and 5 illustrate the use of the Baud Generator with crystal frequencies of 1.8432 MHz, 3.072 MHz, and 8 MHz respectively. For baud rates of 38400 and below, the error obtained is minimal. The accuracy of the desired baud rate is dependent on the crystal frequency chosen.

DESIRED BAUD RATE (BIT RATE CLOCK)	DIVISOR USED TO GENERATE 16 X CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	2304	–
75	1536	–
110	1047	0.026
134.5	857	0.058
150	768	–
300	384	–
600	192	–
1200	96	–
1800	64	–
2000	58	0.69
2400	48	–
3600	32	–
4800	24	–
7200	16	–
9600	12	–
19200	6	–
38400	3	–
56000	2	2.86

TABLE 3: Baud Rates using 1.8432 MHZ Crystal

DESIRED BAUD RATE (BIT RATE CLOCK)	DIVISOR USED TO GENERATE 16 X CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	3840	–
75	2560	–
110	1745	0.026
134.5	1428	0.034
150	1280	–
300	640	–
600	320	–
1200	160	–
1800	107	0.312
2000	96	–
2400	80	–
3600	53	0.628
4800	40	–
7200	27	1.23
9600	20	–
19200	10	–
38400	5	–

TABLE 4: Baud Rates using 3.072 MHZ Crystal

DESIRED BAUD RATE (BIT RATE CLOCK)	DIVISOR USED TO GENERATE 16 X CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	10000	–
75	6667	0.005
110	4545	0.010
134.5	3717	0.013
150	3333	0.010
300	1667	0.020
600	833	0.040
1200	417	0.080
1800	277	0.080
2000	250	–
2400	208	0.160
3600	139	0.080
4800	104	0.160
7200	69	0.644
9600	52	0.160
19200	26	0.160
38400	13	0.160
56000	9	0.790
128000	4	2.344
256000	2	2.344

TABLE 5: Baud Rates using 8 MHZ Crystal

FIFO INTERRUPT MODE OPERATION

When the RCVR FIFO and receiver interrupts are enabled (FCR D0 = 1, IER D0 = 1) RCVR interrupts will occur as follows:

A. The receive data available interrupt will be issued to the CPU when the FIFO has reached its programmed trigger level; it will be cleared as soon as the FIFO drops below its programmed trigger level.

B. The IIR receive data available indication also occurs when the FIFO trigger level is reached and like the interrupt it is cleared when the FIFO drops below the trigger level.

C. The receiver line status interrupt (IIR = 06), as before, has higher priority than the received data available (IIR = 04) interrupt.

D. The data ready bit (LSRD0) is set as soon as a character is transferred from the shift register to the RCVR FIFO. It is reset when the FIFO is empty.

When RCVR FIFO and receiver interrupts are enabled, RCVR FIFO timeout interrupts will occur as follows:

A. A FIFO timeout interrupt will occur, if the following conditions exist:

- at least one character is in the FIFO
- the most recent serial character received was longer than 4 continuous character times ago (if 2 stop bits are programmed the second one is included in this time delay).
- the most recent CPU read of the FIFO was longer than 4 continuous character times ago.

This will cause a maximum character received to interrupt issued delay of 160 ms at 300 baud with a 12 bit character.

B. Character times are calculated by using the RCLK input for a clock signal (this makes the delay proportional to the baud rate).

C. When a timeout interrupt has occurred it is cleared and the timer reset when the CPU reads one character from the RCVR FIFO.

D. When a timeout interrupt has not occurred the timeout timer is reset after a new character is received or after the CPU reads the RCVR FIFO.

When the XMIT FIFO and transmitter interrupts are enabled (FCRD0 = 1, IERD1 = 1), XMIT interrupts will occur as follows:

A. The transmitter holding register interrupt occurs when the XMIT FIFO is below the trigger level. It is cleared as soon as the transmitter holding register is written to and reaches the trigger level or the IIR is read. If the SSi mode is disabled (IER D5 = 0) then the XMIT FIFO trigger level is set to 1 byte.

B. The transmitter FIFO empty indications will be delayed 1 character time minus the last stop bit time whenver the folowing occurs: THRE =1 and there have not been at least two bytes at the same time in the transmit FIFO since the last THRE = 1. The first transmitter interrupt after changing FCR D0 will be immediate, if it is enabled.

Character timeout and RCVR FIFO trigger level interrupts have the same priority as the current received data available interrupt; XMIT FIFO empty has the same priority as the current transmitter holding register empty interrupt.

FIFO MODE OPERATION

With FCR D0 = 1 resetting IER D0, IER D1, IER D2, IER D3 or all to zero puts the UART in the FIFO polled mode of operation. Since the RCVR and XMITTER are controlled separately either one or both can be in the polled mode of operation. In this mode the users program will check RCVR and XMITTER status via the LSR. As stated previously:

LSR D0 will be set as long as there is one byte in the RCVR FIFO

LSR D1 to LSR D4 will specify which error(s) has occurred. Character error status is handled the same way as when in the interrupt mode, the IIR is not affected since IER D2 = 0

LSR D5 will indicate when the XMIT FIFO is empty.

LSR D6 will indicate that both the XMIT FIFO and shift register are empty.

LSR D7 will indicate whether there are any errors in the RVCR FIFO.

There is no trigger level reached or timeout condition indicated in the FIFO Polled Mode, however, the RCVR and XMIT FIFOs are still fully capable of holding characters.

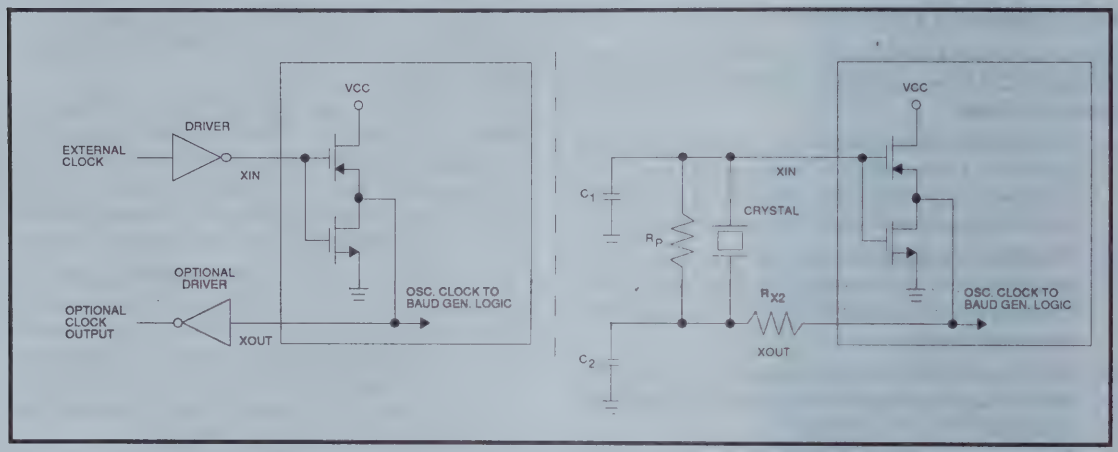


FIGURE 1: Typical Clock Circuits

TYPICAL CRYSTAL OSCILLATOR NETWORK

CRYSTAL	RP	RX2	C1	C2
1.8 - 8 MHz	1 MΩ	1.5K	10-30 pF	40-60 pF

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

(TA = -40°C to +85°C, VCC = 5V ± 10%, unless otherwise noted. Operation above absolute maximum ratings may permanently damage the device.)

PARAMETER	CONDITIONS	RATING
VCC Supply Voltage		+14V
Storage Temperature		–65°C to 150°C
Lead Temperature	Soldering, 10 sec.	260°C
Applied Voltage		–0.3 to Vcc + 0.3

DC CHARACTERISTICS

(TA = –40°C to +85°C, VCC = 5V ± 10%, Vss = 0V, unless otherwise noted; positive current is defined as entering the chip.)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
VILX	Clock input Low voltage		–0.5		0.8	V
VIHX	Clock input High Voltage		2.0		Vcc	V
VIL	Input Low Voltage		–0.5		0.8	V
VIH	Input High Voltage		2.0		Vcc	V
VOL	Output Low Voltage	IOL = 4.0 mA (except XOUT)			0.4	V
VOH	Output High Voltage	IOH = -5.0 mA on all outputs except XOUT	2.4			V
ICC	Average Power Supply	See Note 1		5	10	mA
	Current	See Note 2			50	µA
IIL	Input Leakage	VCC=5.25V, VSS=0V. All other pins floating.			±10	µA
ICL	Clock Leakage	VIN=0V, 5.25V			±10	µA
IOZ	3-State Leakage	VCC=5.25V, VSS=0V, VOUT=0V, 5.25V 1) Chip deselected 2) Chip & write mode selected			±20	µA
VILMR	MR Schmitt VIL				0.8	V
VIHMR	MR Schmitt VIH		2.0			V

Note 1: VCC = 5.25V, TA = 25°C; No loads on outputs. SIN, $\overline{DSR}$, $\overline{DCD}$, $\overline{CTS}$, $\overline{RI}$ = 2.4V. All other inputs = 0.4V. Baud Rate Gen. = 4 MHz; Baud Rate = 50 KHz.

Note 2: VCC = 5.5V, TA = –40°C; No output load; CMOS-level inputs, oscillator disabled

CAPACITANCE

(TA = 25°C, VCC = VSS = 0V, fc = 1 MHz, unmeasured pins returned to VSS)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
CXTAL2	Clock Input Capacitance			15	20	pF
CXTAL1	Clock Output Capacitance			20	30	pF
CI	Input Capacitance			6	10	pF
CO	Output Capacitance			10	20	pF

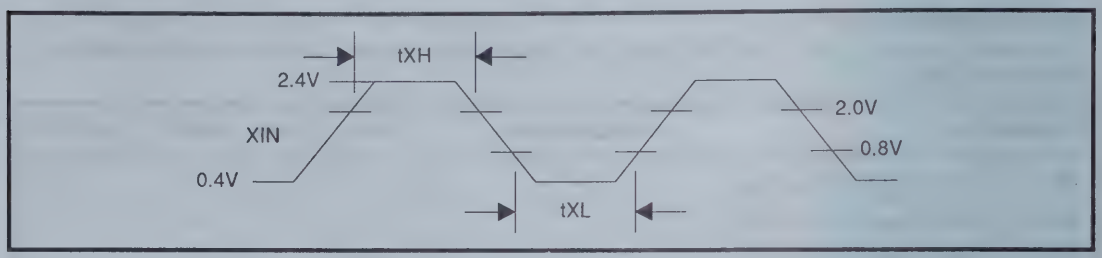


FIGURE 2: External Clock Input* (8 MHz Maximum)

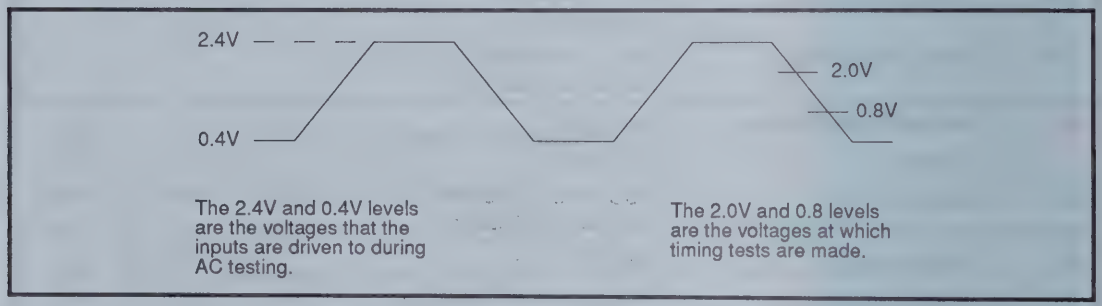

2.4V
0.4V
2.0V
0.8V
The 2.4V and 0.4V levels are the voltages that the inputs are driven to during AC testing.
The 2.0V and 0.8 levels are the voltages at which timing tests are made.

FIGURE 3: AC Test Points*

*All timings are referenced to valid 0 and valid 1.

AC CHARACTERISTICS (TA = -40°C to +85°C, VCC = 5V ± 10%, unless otherwise noted.)

READ & WRITE CYCLE (Refer to Figures 4 & 5.)

PARAMETER		CONDITIONS	73M550		73M550F		UNITS
			MIN	MAX	MIN	MAX	
tADS	Address Strobe Width		60		50		ns
tAS	Address Setup Time		60		30		ns
tAH	Address Hold Time		0		0		ns
tCS	Chip Select Setup Time		60		30		ns
tCH	Chip Select Hold Time		0		0		ns
tCSR	RD, $\overline{RD}$ Delay from Chip Select	See Note 3	30		30		ns
tAR	RD, $\overline{RD}$ Delay from Address	See Note 3	30		30		ns
tRD	RD, $\overline{RD}$ Strobe Width		125		80		ns
tRC	Read Cycle Delay		125		50		ns

READ & WRITE CYCLE (Continued)

PARAMETER		CONDITIONS	73M550		73M550F		UNITS
			MIN	MAX	MIN	MAX	
tAD	Address to Read Data	73M550F only	NA		160		ns
RC	Read Cycle	See Notes 1 & 4	280		210		ns
tRDD	RD, $\overline{RD}$ to Driver Disable Delay	100 pF load See Note 2		60		50	ns
tRVD	Delay from RD, $\overline{RD}$ to Data	100 pF load		125		80	ns
tHZ	RD, $\overline{RD}$ to Floating Data Delay	100 pF load See Note 2	0	100	0	60	ns
tRA	Address Hold Time from RD, $\overline{RD}$	See Note 3	20		20		ns
tRCS	Chip Select Hold Time from RD, $\overline{RD}$	See Note 3	20		20		ns
tCSW	WR, $\overline{WR}$ Delay from Select	See Note 3	30		30		ns
tAW	WR, $\overline{WR}$ Delay from Address	See Note 3	30		30		ns
tWR	WR, $\overline{WR}$ Strobe Width		100		80		ns
tWC	Write Cycle Delay		150		50		ns
WC	Write Cycle=tAW+tWR+tWC		280		160		ns
tDS	Data Setup Time		30		30		ns
tDH	Data Hold Time		30		30		ns
tWA	Address Hold Time from WR, $\overline{WR}$	See Note 3	20		20		ns
tWCS	Chip Select Hold time from WR, $\overline{WR}$	See Note 3	20		20		ns
tMRW	Master Reset Pulse Width		5		1		µs
tXH	Duration of Clock High Pulse	External Clock (8 MHz max.)	55		55		ns
tXL	Duration of Clock Low Pulse	External Clock (8 MHz max.)	55		55		ns

Note 1: RC = tAR + tRD + tRC for 73M550
RC = tAD + tRC for 73M550F

Note 2: Charge and discharge time is determined by VOL, VOH and the external loading.

Note 3: Applicable only when $\overline{ADS}$ is tied low.

Note 4: In FIFO mode R = 425 ns (minimum) between reads of the RCVR FIFO and the status registers (interrupt identification register or line status register).

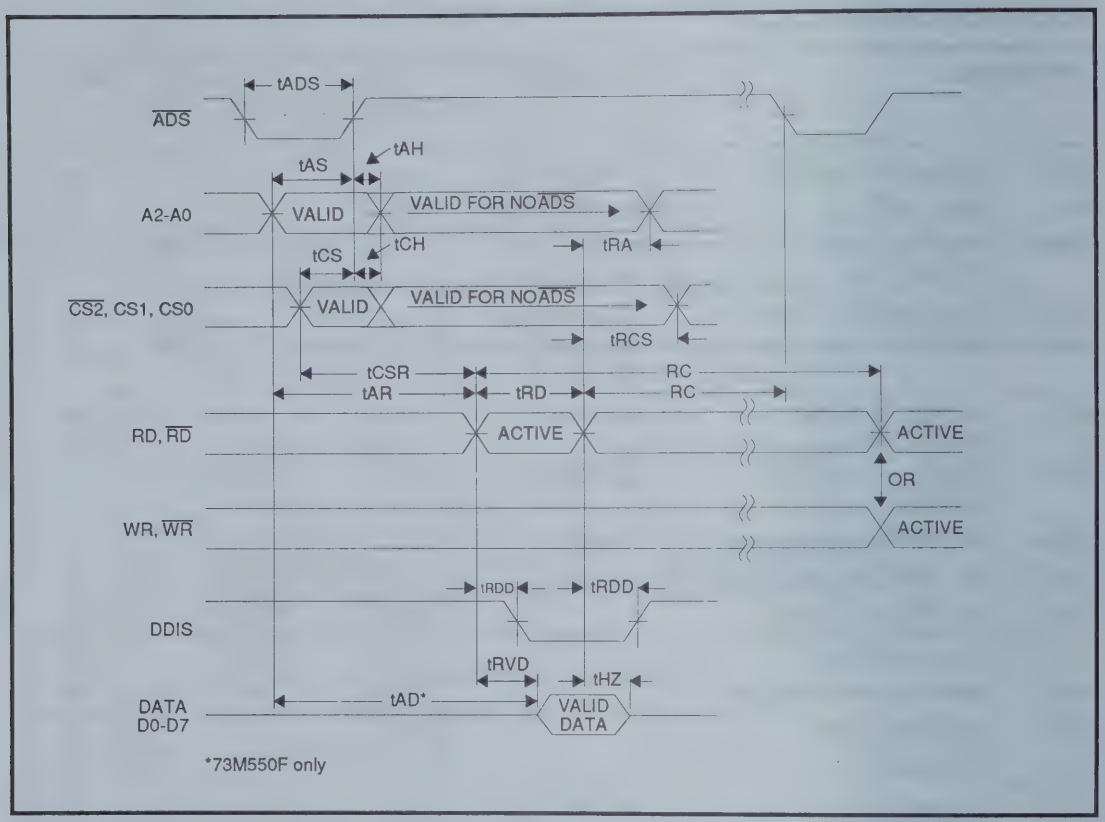


FIGURE 4: Read Cycle Timing

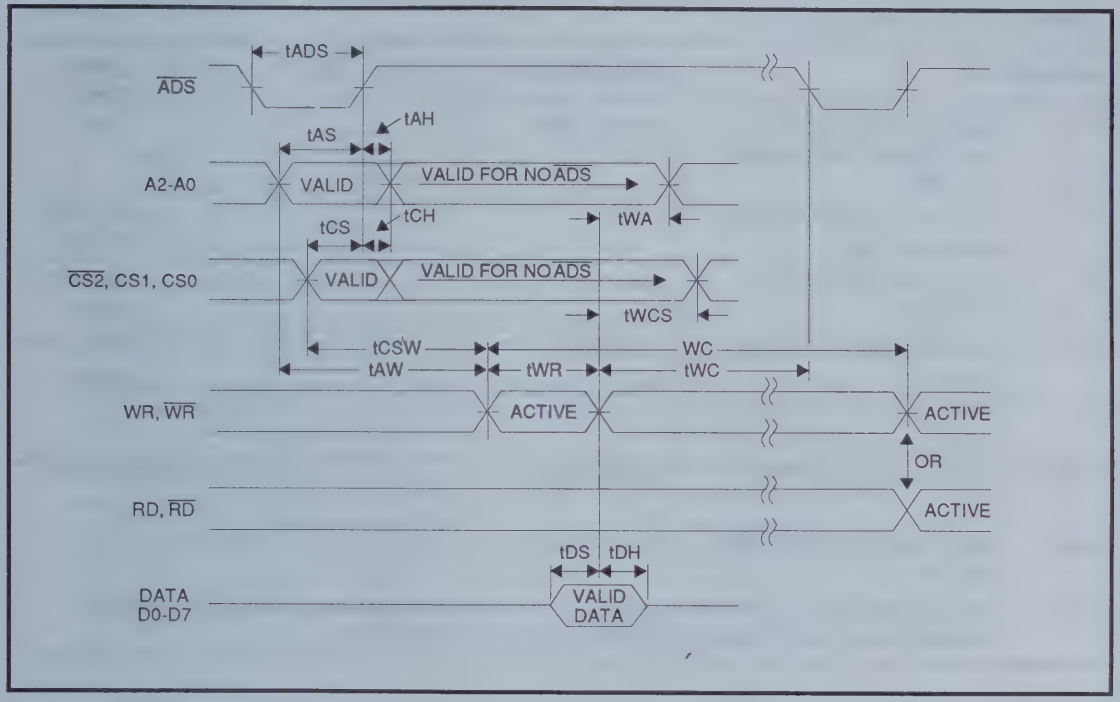


FIGURE 5: Write Cycle Timing

TRANSMITTER (Refer to Figure 6)

PARAMETER		CONDITIONS	MIN	MAX	UNITS
tHR	Delay from rising edge of WR, $\overline{WR}$ (WR THR)to Reset Interrupt	100 pF load		175	ns
tIRS	Delay form Initial INTR Reset to Transmit Start		8	24	BAUDOUT cycles
tSI	Delay from Initial Write to Interrupt	See Note 1	16	24	BAUDOUT cycles
tSTI	Delay from Stop to Interrupt (THRE)	See Note 1	8	8	BAUDOUT cycles
tIR	Delay from RD, $\overline{RD}$ (RD IIR) to Reset Interrupt (THRE)	100 pF load		250	ns
tSXA	Delay from Start to $\overline{TXRDY}$ active	100 pF load		8	BAUDOUT cycles
tWXI	Delay from Write to $\overline{TXRDY}$ inactive	100 pF load		195	ns
Note:	This delay will be lengthened by 1 character time, minus the last stop bit time if the transmitter interrupt delay circuit is active (see FIFO Interrupt mode operation).				

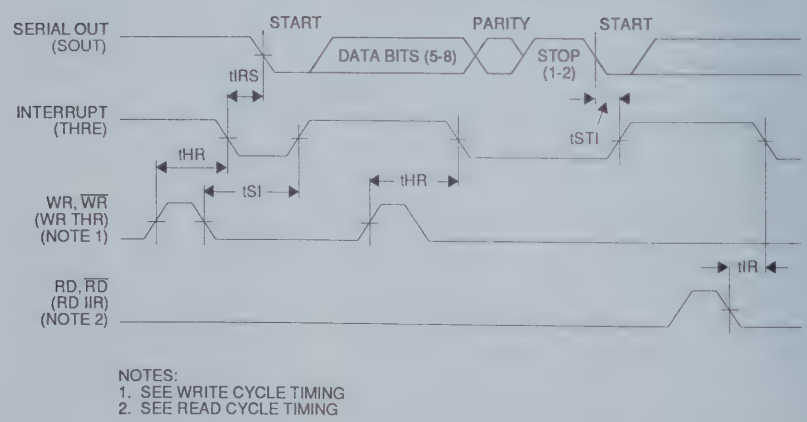


FIGURE 6: Transmitter Timing

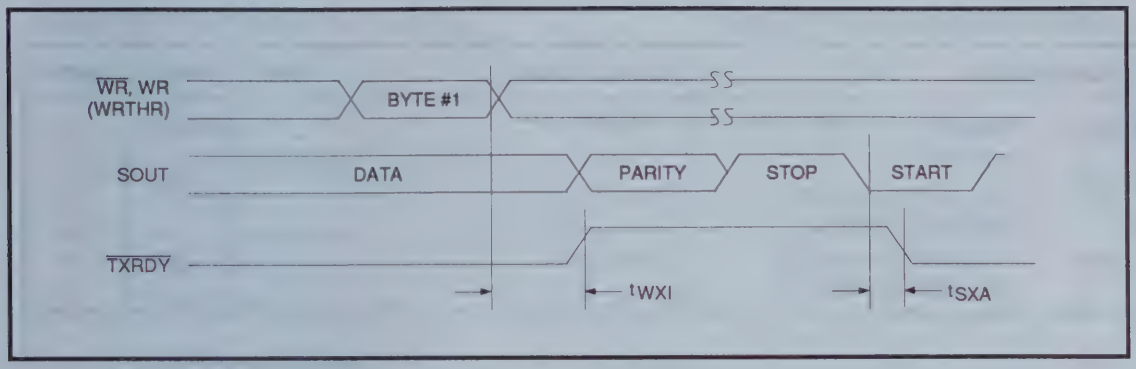


FIGURE 7: Transmitter Ready (Pin 24) FCR D0 = 0 or FCR D0 = 1 and FCR D3 = 0 (Mode 0)

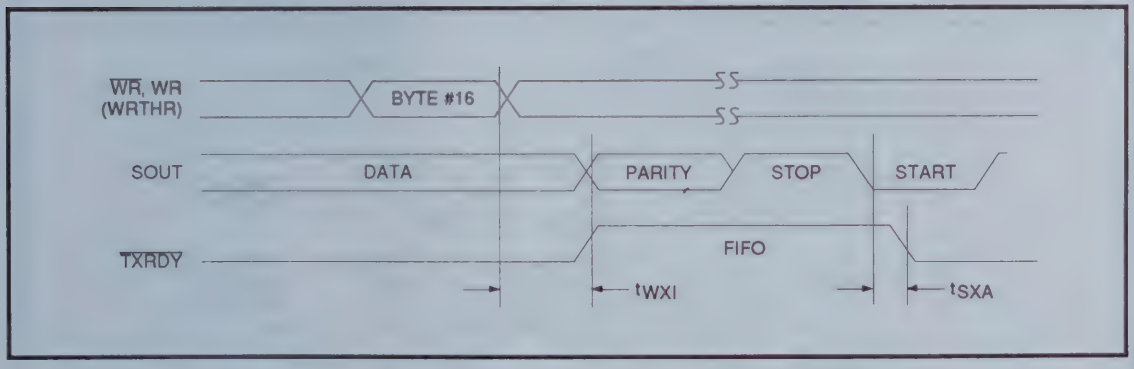


FIGURE 8: Transmitter Ready (Pin 24) FCR D0 = 1 and FCR D3 =1 (Mode 1)

MODEM CONTROL (Refer to Figure 9)

PARAMETER		CONDITIONS	MIN	MAX	UNITS
tMDO	Delay from WR, $\overline{WR}$ (WR MCR) to Output	100 pF load		200	ns
tSIM	Delay to Set Interrupt from Modem Input	100 pF load		250	ns
tRIM	Delay to Reset Interrupt from RD, $\overline{RD}$ (RD MSR)	100 pF load		250	ns

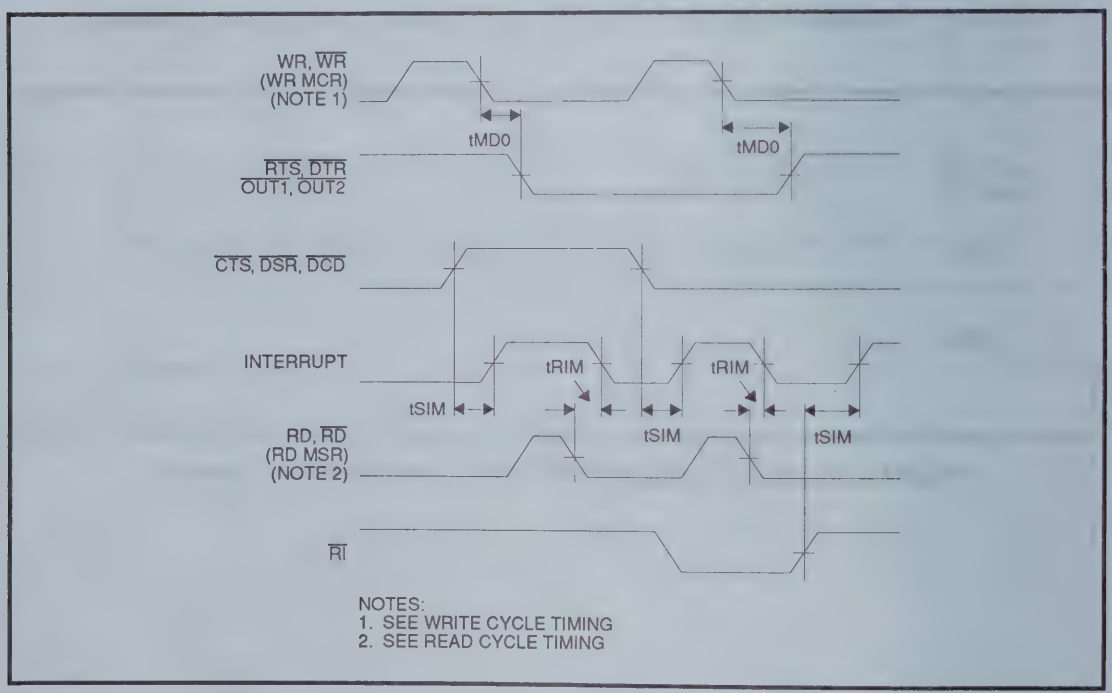


FIGURE 9: Modem Controls Timing

BAUD GENERATOR (Refer to Figure 10)

PARAMETER		CONDITIONS	MIN	MAX	UNITS
N	Baud Divisor		1	2^{16}-1	
tBLD	Baud Output Negative Edge Delay	100 pF load		125	ns
tBHD	Baud Output Positive Edge Delay	100 pF load		125	ns
tLW	Baud Output Down Time	fX=8 MHz, div. by 2, 100 pF load	100		ns
tHW	Baud Output Up Time	fX=8 MHz, div. by 2, 100 pF load	75		ns

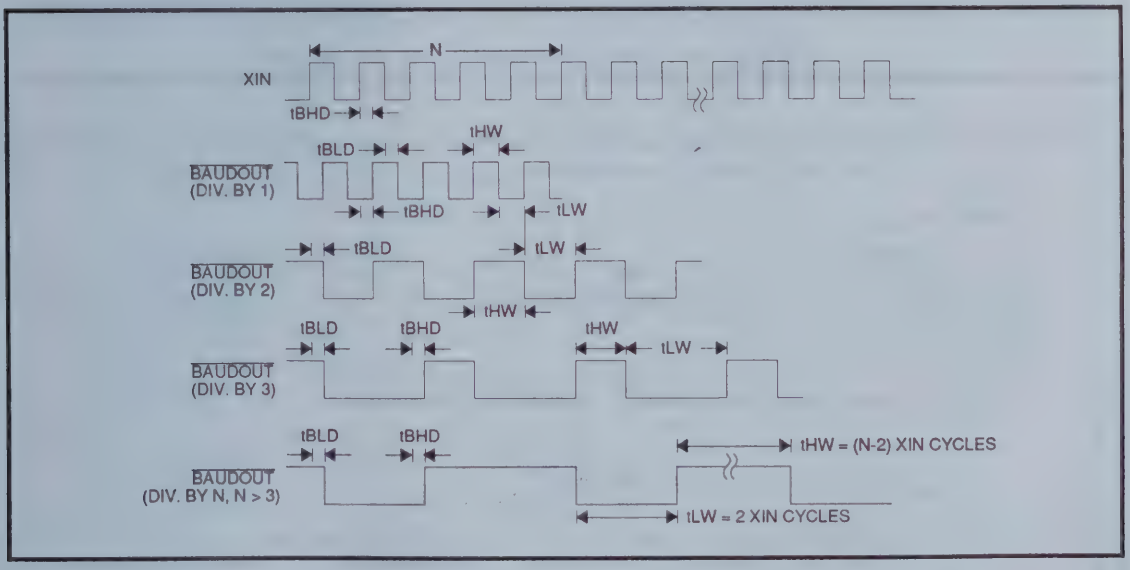
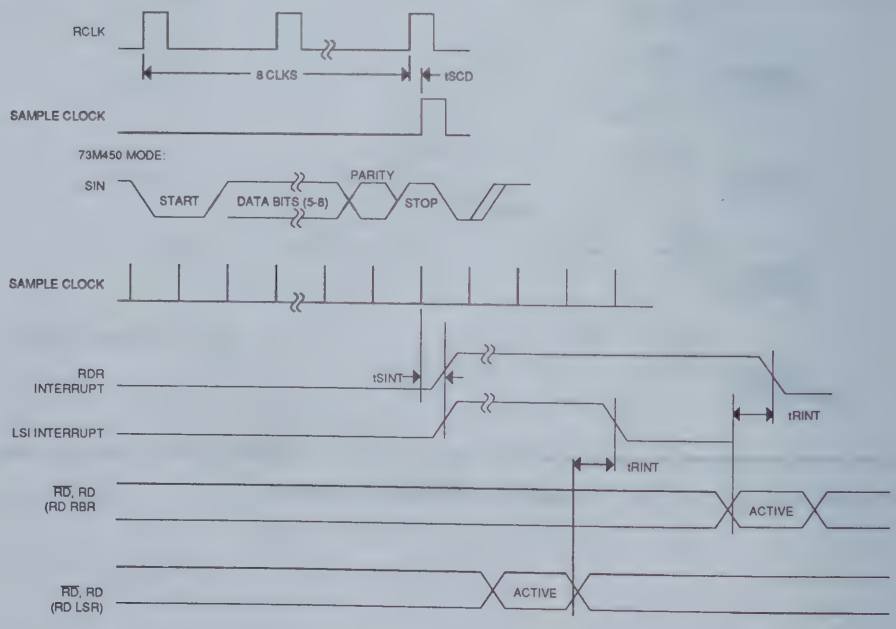


FIGURE 10: BAUDOUT Timing

RECEIVER (Refer to Figure 11)

PARAMETER		CONDITIONS	MIN	MAX	UNITS
tSCD	Delay from RCLK to Sample Time			2	µs
tSINT	Delay from Stop to Set Interrupt	RCLK=tXH & tXL See Note 1		1	RCLK cycles
tRINT	Delay from RD, $\overline{RD}$ (RD RBR/RD LSR) to Reset Interrupt	100 pF load		1	µs

Note 1: In the FIFO mode (FCR D0 = 1) the trigger level interrupts, the receiver data available indication, the active RXRDY indication and the overrrun error indication will be delayed 3 RCLKs. Status indicators (PE, FE, BI) will be delayed 3 RCLKs after the first byte has been received. For subsequently received bytes these indicators will be updated immediately after RD RBR goes inactive. Timeout interrupt is delayed 8 RCLKs.



NOTE: SEE READ CYCLE TIMING

FIGURE 11: Receiver Timing

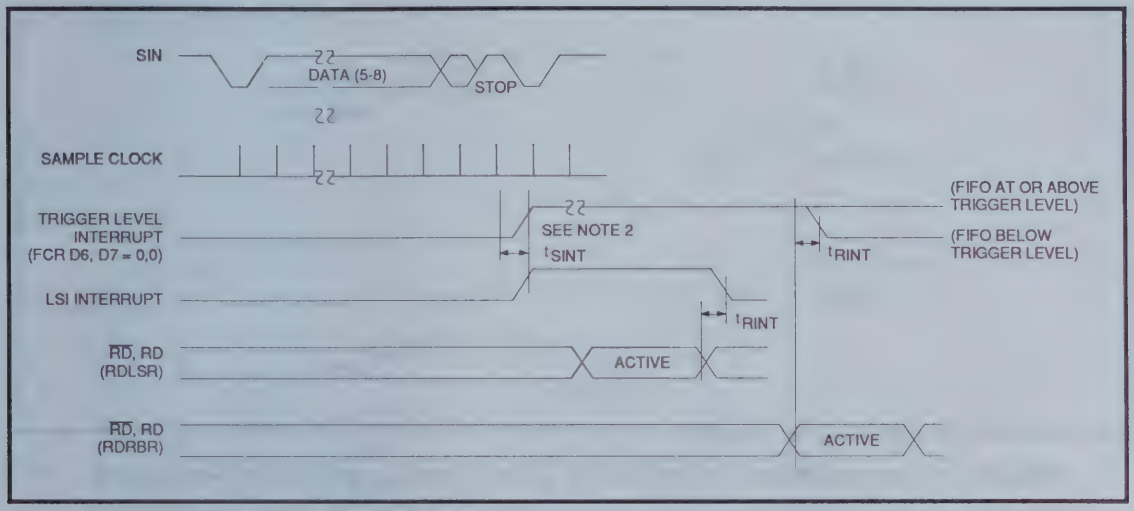


FIGURE 12: RCVR FIFO First Byte (This sets RBR)

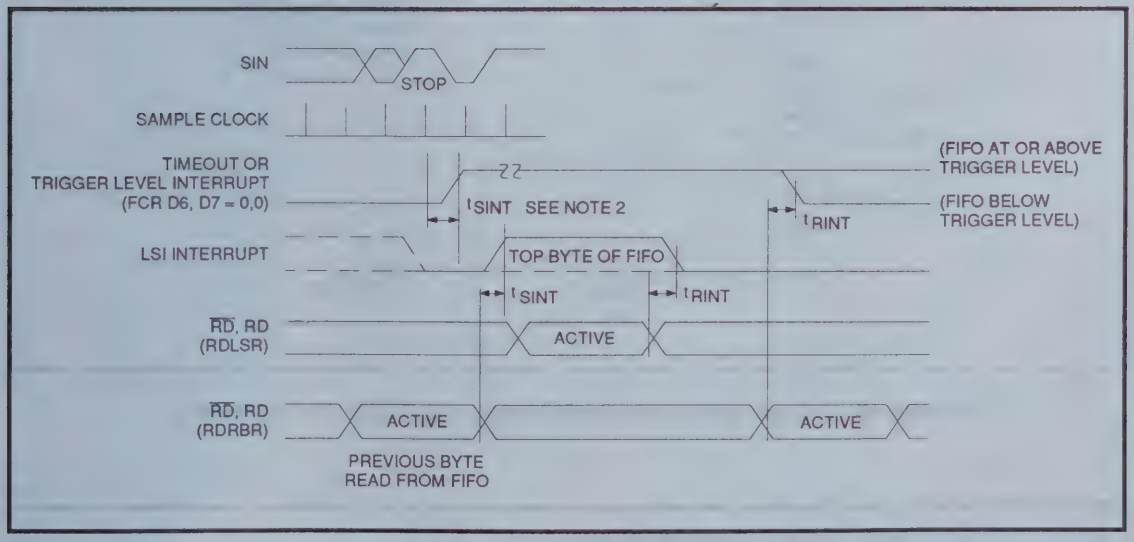


FIGURE 13: RCVR FIFO Bytes Other Than the First Byte (RBR is already set)

Note 1: This is the reading of the last byte in the FIFO

Note 2: If FCR D0 = 1, then tSINT = 3 RCLKs. For a timeout interrupt, tSINT = 8RCLKs.

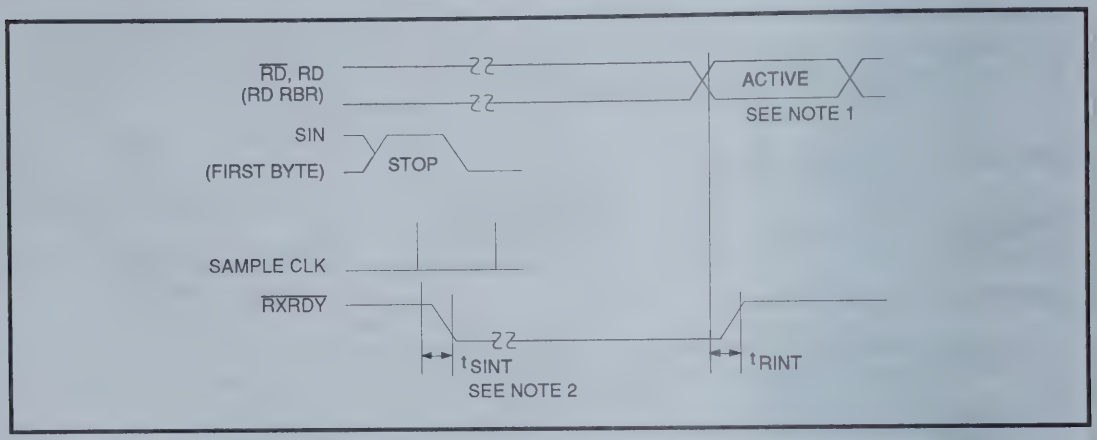


FIGURE 14: Receiver Ready (Pin 29) FCR D0 = 0 or FCR D0 = 1 and FCR D3 = 0 (Mode 0)

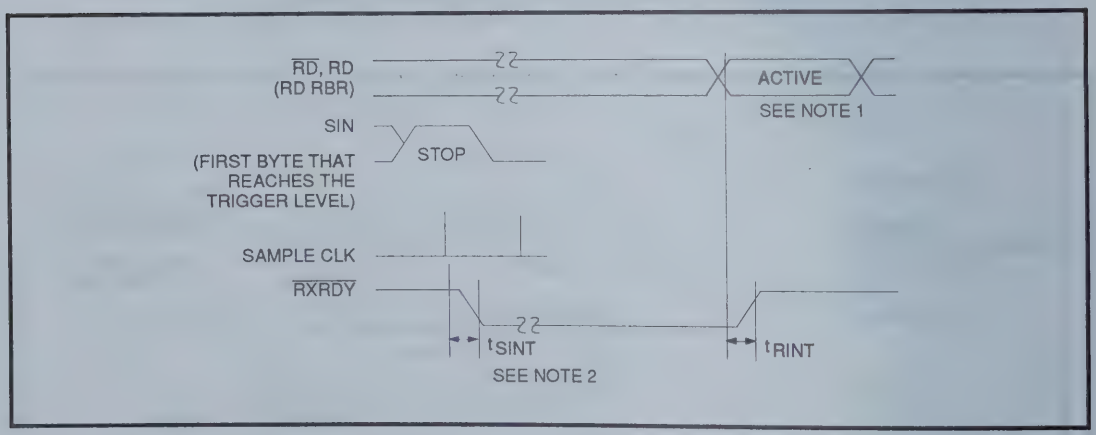


FIGURE 15: Receiver Ready (Pin 29) FCR D0 = 1 and FCR D3 = 1 (Mode 1)

Note 1: This is the reading of the last byte in the FIFO

Note 2: If FCR D0 = 1, then tSINT = 3 RCLKs. For a timeout interrupt, tSINT = 8RCLKs.

APPLICATIONS INFORMATION

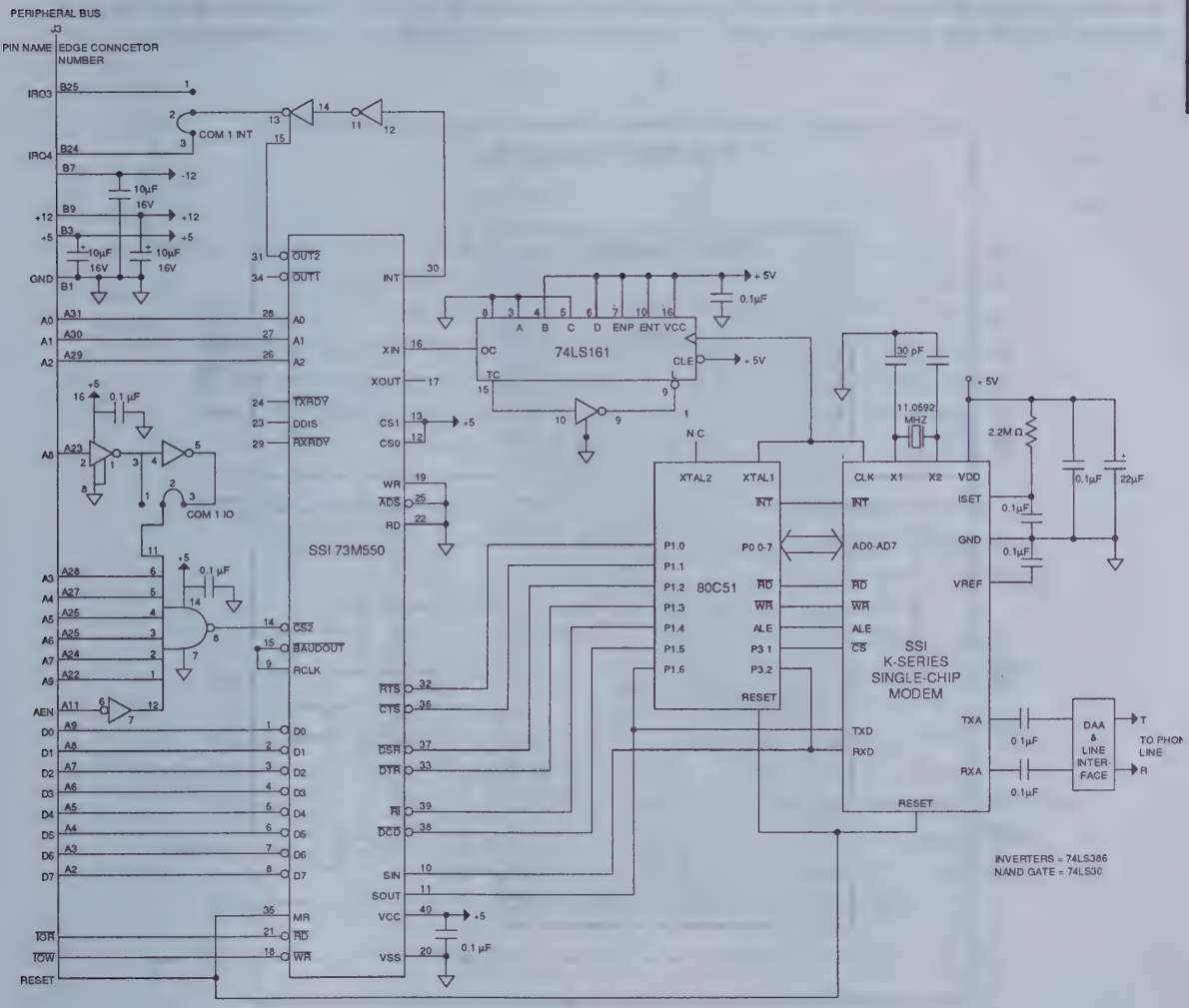
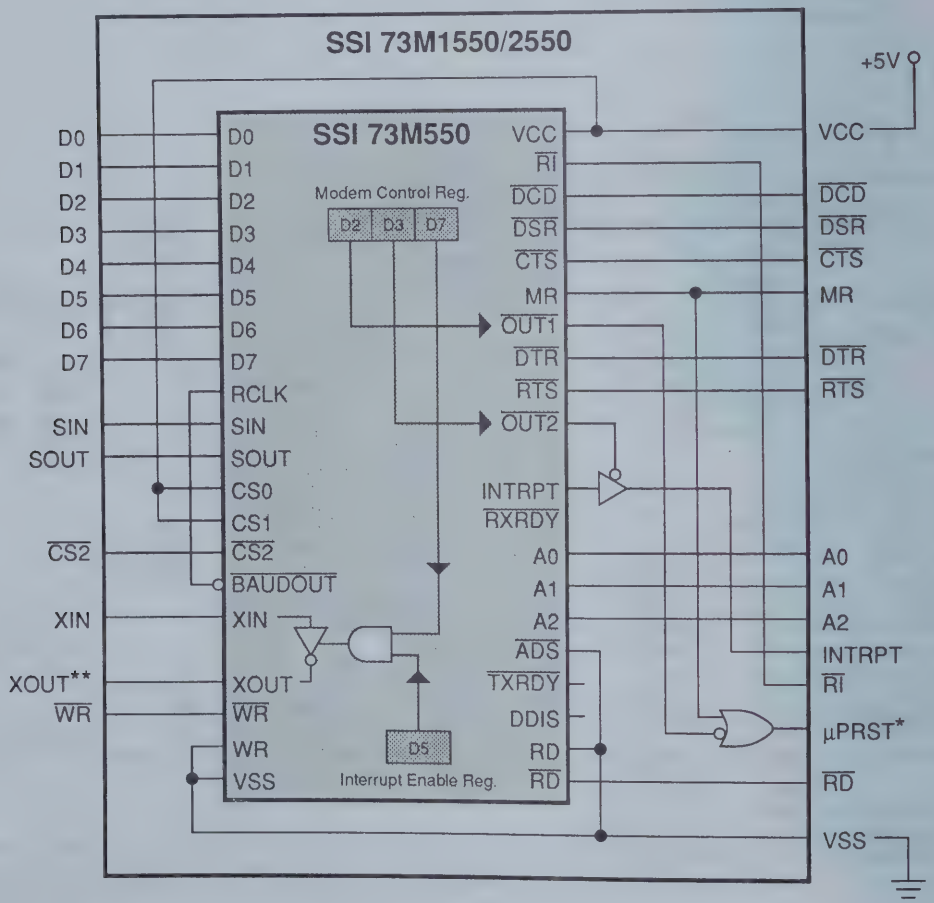


FIGURE 16: Typical Application Showing Modem Interface to Peripheral-Bus via SSI 73M550 UART

APPLICATIONS INFORMATION (Continued)

28-PIN VERSION

The 73M550 is available in two 28-pin configurations: SSI 73M1550 and SSI 73M2550. The relation between these two products and the 40-pin version is shown in the accompanying diagram. Note that the only difference between the 73M1550 and 73M2550 is that the 73M2550 adds the µPRST pin at the expense of the XOUT pin.

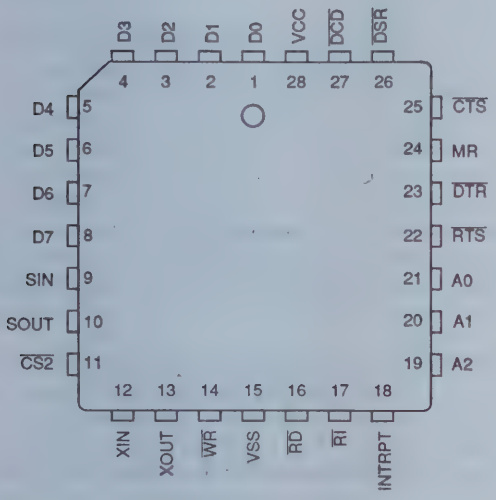


*SSI 73M2550 only.
**SSI 73M1550 only.

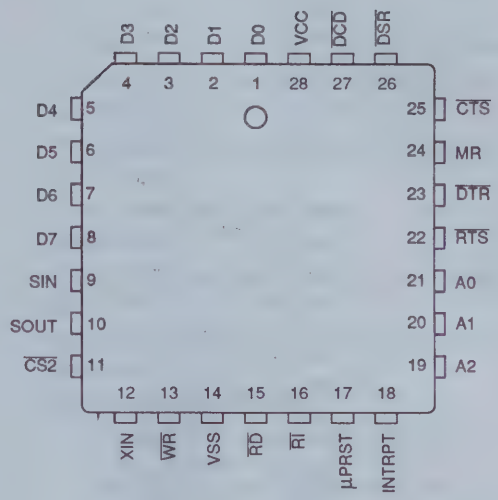
FIGURE 17: Adapter Diagram Showing Internal Connections and Bond-outs from 40-pin to 28-pin Packages

PACKAGE PIN DESIGNATIONS

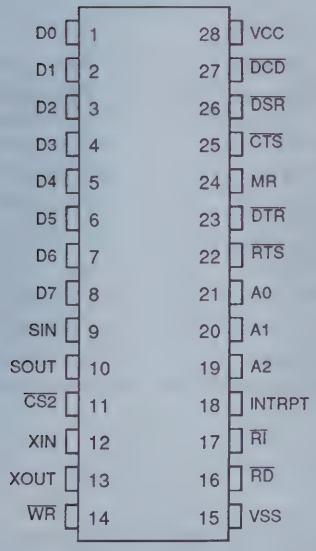
(Top View)



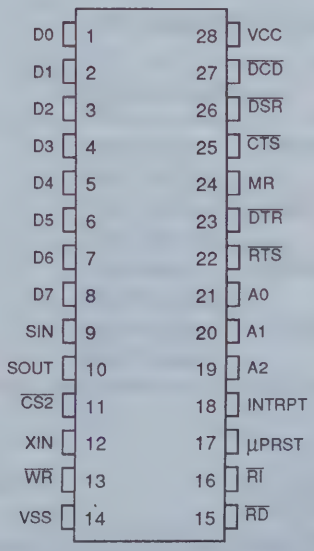
SSI 73M1550 UART
28-PIN PLCC



SSI 73M2550 UART
28-PIN PLCC



SSI 73M1550 UART
28-PIN DIP

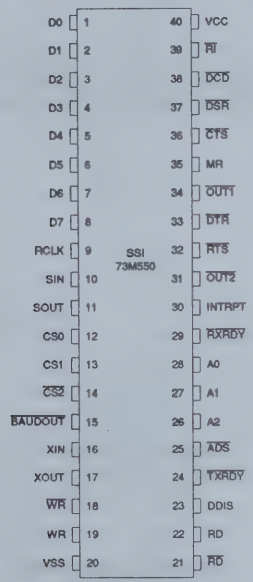


SSI 73M2550 UART
28-PIN DIP

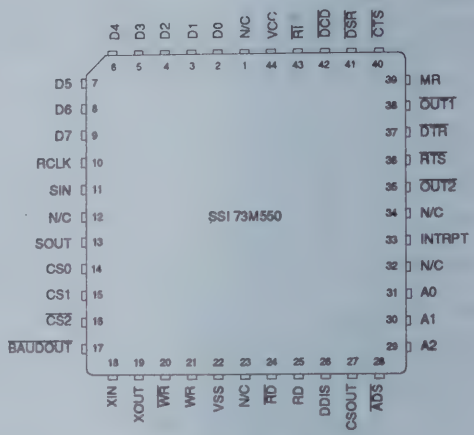
SSI 73M550/550F
Universal Asynchronous Receiver/Transmitter with FIFOs

PACKAGE PIN DESIGNATIONS (Continued)

(Top View)



SSI 73M550 40-Pin DIP



SSI 73M550 44-Pin PLCC

ORDERING INFORMATION

PART DESCRIPTION		ORDER NO.	PKG. MARK
SSI 73M550	40-pin PDIP	SSI 73M550-IP	73M550-IP
	44-pin PLCC	SSI 73M550-IH	73M550-IH
SSI 73M550F	40-pin PDIP	SSI 73M550F-IP	73M550F-IP
	44-pin PLCC	SSI 73M550F-IH	73M550F-IH
SSI 73M1550	28-pin PDIP	SSI 73M1550-IP	73M1550-IP
	28-pin PLCC	SSI 73M1550-IH	73M1550-IH
SSI 73M2550	28-pin PDIP	SSI 73M2550-IP	73M2550-IP
	28-pin PLCC	SSI 73M2550F-IH	73M2550F-IH

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SSI 73M1450/2450
Universal Asynchronous Receiver/Transmitter

July, 1989

2

DESCRIPTION

The SSI 73M1450 and 73M2450 are 28-pin UART ICs. These devices provide the majority of functions performed by the 40-pin SSI 73M450 UART (16C450 compatible), and include additional features. By eliminating redundant pins and minor functions, the 73M1450/2450 retain major compatibility with the 73M450 while reducing the device from a 40-pin package to a 28-pin package. The 73M1450/2450 are primarily used in the interface between a serial data port and the parallel peripheral bus in microprocessor systems.

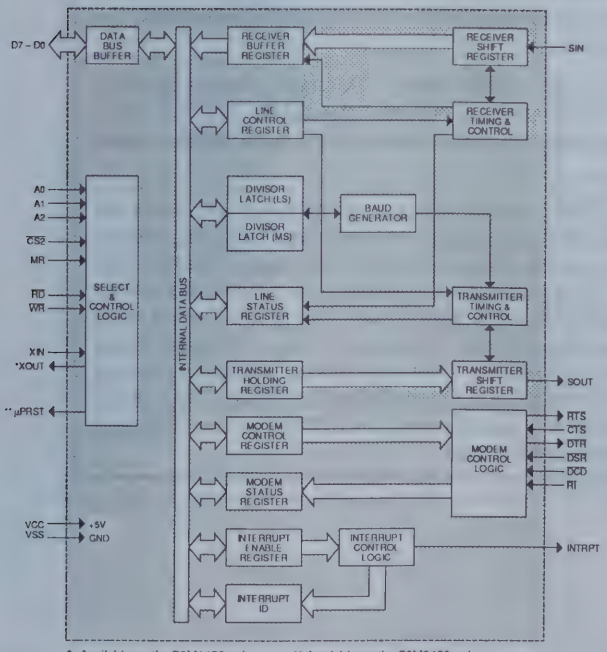
The 73M1450/2450 provide enhanced functions not found in the 73M450 UART. These functions include a bit-programmable oscillator disable for power conservation, a bit-programmable high impedance state on the INTRPT pin, and µPRST pin available on the 73M2450 for resetting external hardware.

(Continued)

FEATURES

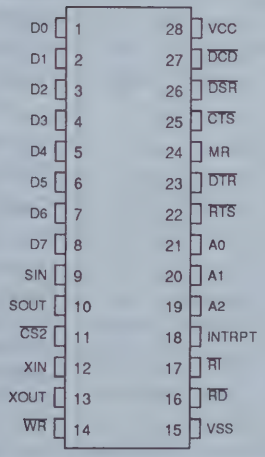
- **Compact, 28-pin DIP or PLCC package types**
- **Bit programmable oscillator disable provides a shut-down mode while retaining memory**
- **Bit programmable high impedance state of INTRPT pin**
- **µPRST pin for external hardware reset (73M2450)**
- **High drive current for directly driving large loads**
- **Full CMOS design for low-power, quiescent operation**
- **Available in two versions:**
  - **73M1450 features XIN & XOUT pins for crystal connection**
  - **73M2450 features XIN pin for external clock input, and µPRST pin for external hardware reset**

BLOCK DIAGRAM

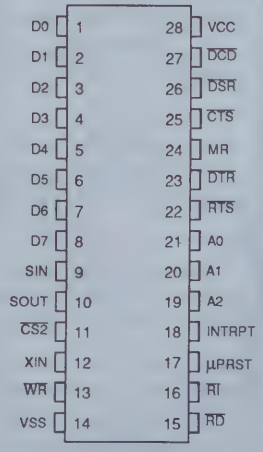


* Available on the 73M1450 only. ** Available on the 73M2450 only

PIN DIAGRAM



73M1450
28-Pin DIP



73M2450
28-Pin DIP

CAUTION: Use handling procedures necessary for a static sensitive component.

DESCRIPTION (Continued)

The 73M1450/2450 eliminates the following pins from a 73M450 UART in order to achieve the smaller, 28-pin package configuration: RCLK, CS0, CS1, $\overline{\text{BAUDOUT}}$, $\overline{\text{OUT1}}$, RD, DDIS, CSOUT, $\overline{\text{ADS}}$, $\overline{\text{OUT2}}$, and WR. The 73M1450 and 73M2450 differ in one feature only: the 73M1450 retains the XIN and XOUT pins found in the 73M450 for connection to the external crystal, the 73M2450 replaces the XOUT pin with a µPRST pin used for resetting external hardware. The 73M2450 is then driven with an external clock input at the XIN pin.

PIN DESCRIPTION

BUS INTERFACE

NAME	73M1450	73M2450	TYPE	DESCRIPTION
$\overline{\text{CS2}}$	11	11	I	Chip Select: The UART is selected when $\overline{\text{CS2}}$ is low. This enables communication between the UART and the CPU.
A0-2	21-19	21-19	I	Register Select Address: These pins determine which UART register is being selected during a read or write on the UART Data Bus. The contents of the DLAB bit (D7) in the Line Control Register (see Table 1) also controls which register is referenced.
$\overline{\text{RD}}$	16	15	I	Read Strobe: A request to read status information or data from a selected register may be made by pulling $\overline{\text{RD}}$ low while the chip is selected.
$\overline{\text{WR}}$	14	13	I	Write Strobe: A request to write control words or data into a selected register may be made by pulling $\overline{\text{WR}}$ low while the chip is selected.
D0-7	1-8	1-8	I/O	UART Data Bus (three-state): This bus provides bi-directional communications between the UART and the CPU; data, control words and status information are transferred via this bus.
INTRPT	18	18	O	Interrupt (three-state): Goes high whenever any one of the following interrupt types occurs: Received Data, Transmitter Holding Register Empty, Receiver Line Status, and Modem Status. These interrupt types must be enabled via the IER for the INTRPT pin to become active. The INTRPT pin is reset low upon the appropriate interrupt service or a master reset operation. The INTRPT pin operation is enabled by setting the OUT2 bit (D3) in the Modem Control Register. When the OUT2 bit (D3) is reset to zero, the INTRPT pin is forced into a high impedance state.

DATA I/O

NAME	73M1450	73M2450	TYPE	DESCRIPTION
SIN	9	9	I	Serial Input: Input for serial data from the communications link (peripheral device, modem or data set).
SOUT	10	10	O	Serial Output: Output for serial data to the communications link (peripheral device,modem or data set). This signal is set high upon a Master Reset.

MODEM CONTROL

NAME	73M1450	73M2450	TYPE	DESCRIPTION
$\overline{RTS}$	22	22	O	Request To Send: This output is programmed by RTS bit (D1) of the Modem Control Register and represents the compliment of that bit. It is used in modem handshaking to signify that the UART has data to transmit. This signal is set high upon Master Reset or during loop mode operation.
$\overline{CTS}$	25	25	I	Clear To Send: A modem status input whose condition is complimented and reflected in the CTS bit (D4) of the Modem Status Register. When $\overline{CTS}$ is low, it indicates that communications have been established and that data may be transmitted.
$\overline{DTR}$	23	23	O	Data Terminal Ready: This output is programmed by DTR bit (D0) of the Modem Control Register, and represents the compliment of that bit. It is used in modem handshaking to signify that the UART is available to communicate. This signal is set high upon Master Reset or during loop mode operation.
$\overline{DSR}$	26	26	I	Data Set Ready: A modem status input whose condition is complimented and reflected in the DSR bit (D5) of the Modem Status Register. When $\overline{DSR}$ is low, it indicates that the modem is ready to establish communications.
$\overline{DCD}$	27	27	I	Data Carrier Detect: A modem status input whose condition is complimented and reflected in the DCD bit (D7) of the Modem Status Register. When $\overline{DCD}$ is low, it indicates that the modem is receiving a carrier.
$\overline{RI}$	17	16	I	Ring Indicator: A modem status input whose condition is complimented and reflected in the RI bit (D6) of the Modem Status Register. When $\overline{RI}$ is low, it indicates that a telephone ringing signal is being received.

GENERAL & CLOCKS

NAME	73M1450	73M2450	TYPE	DESCRIPTION
VCC	28	28	I	+5V Supply, ±10%: Bypass with 0.1 µF capacitor to GND.
VSS	15	14	I	System Ground.
MR	24	24	I	Master Reset: When high, this input clears all UART control logic and registers, except for the Receiver Buffer, Transmitter Holding and Divisor Latches; also, the state of output signals SOUT, INTRPT, $\overline{RTS}$ and $\overline{DTR}$ are affected by an active MR input. This input is buffered with a TTL-compatible Schmitt Trigger.
XIN XOUT	12 13	12 N/A	I/O I/O	External System Clock I/O: These two pins connect the main timing reference (crystal or signal clock) to the UART. Additionally, XIN may be driven by an external clock source. The XOUT pin is not abailable on the 73M2450 which requires an external clock connected to the XIN pin.
µPRST	N/A	17	O	Microprocessor Reset: This output signal is used to provide a hardware reset to a local controller. This pin becomes active high when the MR pin is pulled high or OUT1 bit (D2) of the modem control register is set. The µPRST function is available with the 73M2450 device only.

TABLE 1: CONTROL REGISTER ADDRESS TABLE

DLAB	A2	A1	A0	REGISTER
0	0	0	0	Receiver Buffer Register (read), Transmitter Holding Reg. (write)
0	0	0	1	Interrupt Enable Register
X	0	1	0	Interrupt Identification Register (read only)
X	0	1	1	Line Control Register
X	1	0	0	Modem Control Register
X	1	0	1	Line Status Register
X	1	1	0	Modem Status Register
X	1	1	1	Scratch Register
1	0	0	0	Divisor Latch Register (least significant byte)
1	0	0	1	Divisor Latch Register (most significant byte)

TABLE 2: UART RESET FUNCTIONS

REGISTER/SIGNAL	RESET CONTROL	RESET STATE
Interrupt Enable Register	Master Reset	All bits low (0-3 forced and 4-7 permanent)
Interrupt Identification Register	Master Reset	Bit 0 is high; bits 1 & 2 are low; bits 3-7 are permanently low
Line Control Register	Master Reset	All bits low
Modem Control Register	Master Reset	All bits low
Line Status Register	Master Reset	All bits low, except bits 5 & 6 are high
Modem Status Register	Master Reset	Bits 0-3 are low; bits 4-7 = input signal
SOUT	Master Reset	High
INTRPT (RCVR Errs)	Read LSR/MR	Low
INTRPT (RCVR Data Ready)	Read RBR/MR	Low
INTRPT (THRE)	Read IIR/Write THR/MR	Low
INTRPT (Modem Status Changes)	Read MSR/MR	Low
$\overline{RTS}$	Master Reset	High
$\overline{DTR}$	Master Reset	High
µPRST	Master Reset/set OUT1 bit	High during active Master Reset/OUT1 bit; low afterwards

CONTROL REGISTER OVERVIEW

REGISTER		REGISTER ADDRESS (A2-A0) & DLAB	DATA BIT NUMBER D7	D6	D5	D4	D3	D2	D1	D0
RECEIVER BUFFER REGISTER (READ ONLY)	RBR	000 DLAB = 0	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
TRANSMIT HOLDING REGISTER (WRITE ONLY)	THR	000 DLAB = 0	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
INTERRUPT ENABLE REGISTER	IER	001 DLAB = 0	0	0	SSI MODE	0	ENABLE MODEM STATUS INTERRUPT	ENABLE REC. LINE STATUS INTERRUPT	ENABLE THR EMPTY INTERRUPT	ENABLE REC. DATA AVAILABLE INTERRUPT
INTERRUPT ID REGISTER (READ ONLY)	IIR	010 DLAB = X	0	0	0	0	0	INTERRUPT ID BIT 1	INTERRUPT ID BIT 0	"0" IF INTERRUPT PENDING
LINE CONTROL REGISTER	LCR	011 DLAB = X	DIVISOR LATCH ACCESS (DLAB)	SET BREAK	STICK PARITY	EVEN PARITY SELECT (EPS)	PARITY ENABLE (PEN)	NUMBER OF STOP BITS (STB)	WORD LENGTH SELECT 1 (WLS1)	WORD LENGTH SELECT 0 (WLS0)
MODEM CONTROL REGISTER	MCR	100 DLAB = X	OSC OFF	0	0	LOOP	OUT2 (INTRPT ENABLE)	OUT1 (μPRST CNTRL)	REQUEST TO SEND (RTS)	DATA TERMINAL READY (DTR)
LINE STATUS REGISTER	LSR	101 DLAB = X	0	TRANSMIT-TER EMPTY (TEMT)	TRANSMIT HOLDING REGISTER EMPTY(THRE)	BREAK INTERRUPT (BI)	FRAMING ERROR (FE)	PARITY ERROR (PE)	OVERRUN ERROR (OE)	DATA READY (DR)
MODEM STATUS REGISTER (READ ONLY)	MSR	110 DLAB = X	DATA CARRIER DETECT (DCD)	RING INDICATOR (RI)	DATA SET READY (DSR)	CLEAR TO SEND (CTS)	DELTA DATA CARR. DETECT (DDCD)	TRAILING EDGE RING INDICATOR (TERI)	DELTA DATA SET READY (DDSR)	DELTA CLEAR TO SEND (DCTS)
SCRATCH REGISTER	SCR	111 DLAB = X	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DIVISOR LATCH (LS)	DLL	000 DLAB = 1	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DIVISOR LATCH (MS)	DLM	001 DLAB = 1	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8

REGISTER BIT DESCRIPTIONS

RECEIVER BUFFER REGISTER (RBR) (READ ONLY)
UART ADDRESS: A2 - A0 = 000, DLAB = 0

This read only register contains the parallel received data with start, stop, and parity bits (if any) removed. The high order bits for less than 8 data bits/character will be set to 0.

TRANSMIT HOLDING REGISTER (THR) (WRITE ONLY)
UART ADDRESS: A2 - A0 = 000, DLAB = 0

This write only register contains the parallel data to be transmitted. The data is sent LSB first with start, stop, and parity bits (if any) added to the serial bit stream as the data is transferred.

INTERRUPT ENABLE REGISTER (IER)
UART ADDRESS: A2 - A0 = 001, DLAB = 0

This 8-bit register enables the four types of interrupts of the UART to separately activate the chip Interrupt (INTRPT) output signal. This register also allows access to the chip's special SSI mode which contains the oscillator disable function. It is possible to totally disable the interrupt system by resetting bits D0 through D3 of the Interrupt Enable Register. Similarly, by setting the appropriate bits of this register to a logic 1, selected interrupts can be enabled. Disabling the interrupt system inhibits the Interrupt Identification Register and the active (high) INTRPT output from the chip. All other system functions operate in their normal manner, including the setting of the Line Status and Modem Status Registers.

The chip's SSI mode can be activated by setting bit D5. Once in the SSI mode, the chip can be placed in a power shut-down state by setting bit D7 in the modem control register.

BIT	NAME	COND.	DESCRIPTION
D0	Received Data	1	This bit enables the Received Data Available Interrupt when set to logic 1.
D1	Transmitter Holding Register Empty	1	This bit enables the Transmitter Holding Register Empty Interrupt when set to logic 1.
D2	Receiver Line Status Interrupt	1	This bit enables the Receiver Line Status Interrupt when set to logic 1.
D3	Modem Status	1	This bit enables the Modem Status Interrupt when set to logic 1.
D4	Not used	0	Always logic 0.
D5	SSI Mode	0	Disables chip's SSI Mode; normal operation.
		1	Enables chip's SSI mode. In this mode, chip can be placed into power shut-down by setting bit D7 in modem control register.
D6-D7	Not used	0	Always logic 0.

INTERRUPT ID REGISTER (IIR) (READ ONLY)
UART ADDRESS: A2 - A0 = 010

The IIR register gives prioritized information as to the status of interrupt conditions. When accessed, the IIR freezes the highest priority interrupt pending and no other interrupts are acknowledged until the particular interrupt is serviced by the CPU. The order of interrupt priorities is shown in the table below.

BIT	NAME	COND.	DESCRIPTION
D0	Interrupt Pending	0	This bit can be used in either a hardwired prioritized or polled environment to indicate whether an interrupt is pending. When bit D0 is a logic 0, an interrupt is pending and the IIR contents may be used as a pointer to the appropriate interrupt service routine.
		1	When bit D0 is a logic 1, no interrupt is pending.
D1, D2	Interrupt ID bits 0, 1	Table below	These two bits of the IIR are used to identify the highest priority interrupt pending as indicated in the following table.
D3 - D7	Not Used	0	These five bits of the IIR are always logic 0.

INTERRUPT PRIORITY TABLE

D2	D1	D0	PRIORITY	TYPE	SOURCE	RESET
0	0	1	-	None	None	N/A
1	1	0	Highest	Receiver Line Status	Overrun Error, Parity Error, Framing Error or Break Interrupt	Reading the Line Status Register
1	0	0	Second	Receive Data Available	Receive Data Available	Reading the Rcvr. Buffer Register
0	1	0	Third	Transmit Holding Register Empty	Transmit Holding Register Empty	Reading IIR Register (if source of interrupt) or Writing to Transmit Holding Register
0	0	0	Fourth	Modem Status	Clear to Send or Data Set Ready or Ring Indicator or Data Carrier Det.	Reading the Modem Status Register

LINE CONTROL REGISTER (LCR)
UART ADDRESS: A2 - A0 = 011

The user specifies the format of the asynchronous data communications exchange via the Line Control Register. In addition to controlling the format, the user may retrieve the contents of the Line Control Register for inspection. This feature simplifies system programming and eliminates the need for separate storage in system memory of the line characteristics.

BIT	NAME	COND.		DESCRIPTION
D0	Word Length Select 0 (WLS0)			Bits D0 and D1 select the number of data bits per character as shown:
D1	Word Length Select 1 (WLS1)	D1	D0	Word Length
		0	0	5 bits
		0	1	6 bits
		1	0	7 bits
		1	1	8 bits
D2	Number of Stop Bits (STB)	0 or 1		This bit specifies the number of stop bits in each transmitted character. If bit D2 is a logic 0, one stop bit is generated in the transmitted data. If bit D2 is a logic 1 when a 5-bit word length is selected via bits 0 and 1, one-and-a-half stop bits are generated. If bit D2 is a logic 1 when either a 6, 7, or 8-bit word length is selected, two stop bits are generated. The receiver checks the first stop bit only, regardless of the number of stop bits selected.
D3	Parity Enable (PEN)	1		This is the Parity Enable (PEN) bit. When set to a logic 1, a parity bit is generated (transmit data) or checked (receive data) between the last data word bit and stop bit of the serial data. (The parity bit is used to produce an even or odd number of 1's when the data word bits and the parity bit are summed).
D4	Even Parity Select (EPS)	1 or 0		This is the Even Parity Select (EPS) bit. When bit D3 is a logic 1 and bit D4 is a logic 0, an odd number of logic 1's is transmitted or checked in the data word bits and parity bit. When bit D3 is a logic 1 and bit D4 is a logic 1, an even number of logic 1's is transmitted or checked.

LINE CONTROL REGISTER (LCR) (Continued)

BIT	NAME	COND.		DESCRIPTION
D5	Stick Parity	1 or 0		This is the Stick Parity bit. When bit D3 is a logic 1 and bit D5 is a logic 1, the parity bit is transmitted and checked by the receiver as a logic 0 if bit D4 is a logic 1 or as a logic 1 if bit D4 is a logic 0.
		D5	D4	Parity
		0	0	ODD Parity
		0	1	EVEN Parity
		1	0	MARK Parity
		1	1	SPACE Parity
D6	Set Break	1		This is the Break Control bit. When set to a logic 1, the serial out (SOUT) is forced to a logic 0 state. The break is disabled by setting bit D6 to a logic 0. This bit acts only on SOUT and has no effect on the transmitter logic. See note below.
D7	Divisor Latch Access Bit (DLAB)	1		The Divisor Latch Access Bit (DLAB) must be set high (logic 1) to access the Divisor Latches of the baud generator during a Read or Write operation. It must be set low (logic 0) to access the Receiver Buffer, the Transmitter Holding Register, or the Interrupt Enable Register.

NOTE: This feature enables the CPU to alert a terminal in a computer communications system. If the following sequence is followed, no erroneous or extraneous characters will be transmitted because of the break.

1. Load an all 0's pad character in response to THRE.
2. Set break in response to the next THRE.
3. Wait for the Transmitter to be idle. (TEMT = 1), and clear break when normal transmission has to be restored.

During the break, the Transmitter can be used as a character timer to accurately establish the break duration.

MODEM CONTROL REGISTER (MCR)
UART ADDRESS: A2 - A0 = 100

The Modem Control Register controls the interface with the modem, data set or peripheral device. Bits D1 and D0 are also available as read only bits in the UART Control Register in the Modem Registers.

BIT	NAME	COND.	DESCRIPTION
D0	DTR	0/1	This bit controls the Data Terminal Ready ($\overline{DTR}$) output. When bit D0 is set to a logic 1, the $\overline{DTR}$ output is forced to a logic 0. When bit D0 is reset to a logic 0, the $\overline{DTR}$ output is forced to a logic 1.
D1	RTS	0/1	This bit controls the Request to Send ($\overline{RTS}$) output. When bit D1 is set to a logic 1, the $\overline{RTS}$ output is forced to a logic 0. When bit D1 is reset to a logic 0, the $\overline{RTS}$ output is forced to a logic 1.
D2	OUT1 (µPRST control)	0/1	This bit controls the µPRST output. When bit D2 is set to a logic 1, the µPRST output is forced to a logic 1. When bit D2 is reset to logic 0, the µPRST is forced to logic 0.
D3	OUT2 (INTRPT enable)	0/1	This bit controls the INTRPT output. When bit D3 is set to logic 1, the INTRPT output is enabled. When bit D3 is reset to logic 0, the INTRPT output is forced into a high impedance state.
D4	LOOP	0/1	This bit provides a local loopback feature for diagnostic testing of the UART. When bit D4 is set to logic 1, the following occurs: the transmitter Serial Output (SOUT) is set to the logic 1 state; the receiver Serial Input (SIN) is disconnected; the output of the Transmitter Shift Register is "looped back" into the Receiver Shift Register input; the four Modem Control inputs ($\overline{CTS}$, $\overline{DSR}$, $\overline{DCD}$ and $\overline{RI}$) are disconnected; the three modem control output pins ($\overline{DTR}$, $\overline{RTS}$ and µPRST) are forced to their inactive state; the four modem control register bits DTR, RTS, OUT1 and OUT2 are mapped to the modem status register bits CTS, DSR, RI and DCD, respectively. In the diagnostic mode, data that is transmitted is immediately received. This feature allows the processor to verify the transmit and received-data paths of the UART. In the diagnostic mode, the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational, but the interrupts' sources are now the lower four bits of the Modem Control Register instead of the four Modem Control inputs. The interrupts are still controlled by the Interrupt Enable Register.
D5-D6		0	These bits are permanently set to logic 0.
D7	OSC OFF	0/1	This bit is available only in the SSI mode. Resetting this bit allows normal operation. Setting this bit places the chip in a power shut-down mode.

LINE STATUS REGISTER (LSR)
UART ADDRESS: A2 - A0 = 101

This register provides status information to the CPU concerning the data transfer. Bits 1-4 are the error conditions that produce a Receiver Line Status interrupt whenever any of the corresponding conditions are detected. The Line Status Register is intended for read operation only. Writing to this register is not recommended as this operation is used for factory testing.

BIT	NAME	COND.	DESCRIPTION
D0	DR	1	The Data Ready (DR) bit is set to a 1 whenever a complete incoming character has been received and transferred into the Receiver Buffer Register. DR is reset to 0 by reading the data in the Receiver Buffer Register.
D1	OE	1	The Overrun Error (OE) bit indicates that the data in the Receiver Buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer Register, thereby destroying the previous character. OE is reset to 0 whenever the CPU reads the contents of the Line Status Register.
D2	PE	1	The Parity Error (PE) bit indicates that the received character did not have the correct parity. PE is reset to 0 whenever the CPU reads the Line Status Register.
D3	FE	1	The Framing Error (FE) bit indicates that the received character did not have a valid stop bit. FE is reset to 0 whenever the CPU reads the contents of the Line Status Register.
D4	BI	1	The Break Interrupt (BI) bit indicates that a break has been received. A break occurs whenever the received data is held to 0 for a full data word (start + data + stop). BI is reset to 0 whenever the CPU reads the Line Status Register.
D5	THRE	1	The Transmit Holding Register Empty (THRE) is set to a logic 1 when a character is transferred from the Transmit Holding Regsiter into the Transmit Shift Register, indicating that the UART is ready to accept a new character for transmission. In addition, this bit causes the UART to issue an interrupt to the CPU when the THRE Interrupt enable is set high. THRE is reset to 0 when the CPU loads a character into the Transmit Holding Register.
D6	TEMT	1	The Transmit Empty (TEMT) indicates that both the Transmit Holding Register and the Transmit Shift Registers are empty. TEMT is reset to 0 whenever the TSR or THR contains a data character.
D7	-	0	Always zero.

MODEM STATUS REGISTER (MSR) (READ ONLY)
UART ADDRESS: A2 - A0 = 110

This register provides the current state of the control signals from the modem or peripheral device. In addition, four bits provide change information. Whenever bit 0, 1, 2 or 3 is set to logic 1, a Modem Status Interrupt is generated; reset to logic 0 occurs whenever they are read. In Loop Mode CTS, DSR, RI and DCD are taken from RTS, DTR, OUT1, and OUT2 in the Modem Control Register respectively.

BIT	NAME	COND.	DESCRIPTION
D0	DCTS	1	The Delta Clear to Send (DCTS) bit indicates that the $\overline{CTS}$ input to the chip has changed state since the last time it was read by the CPU.
D1	DDSR	1	The Delta Data Set Ready (DDSR) bit indicates that the $\overline{DSR}$ input to the chip has changed state since the last time it was read by the CPU.
D2	TERI	1	The Trailing Edge of the Ring Indicator (TERI) detect bit indicates that the $\overline{RI}$ input to the chip has changed from an Off (logic 0) to an On (logic 1) condition.
D3	DDCD	1	The Delta Data Carrier Detect (DDCD) bit indicates that the $\overline{DCD}$ input to the chip has changed state.
D4	CTS	1	This bit is the complement of the Clear To Send ($\overline{CTS}$) input. If bit D4 (loop) of the MCR is set to a 1, this bit is equivalent to RTS in the MCR.
D5	DSR	1	This bit is the complement of the Data Set Ready ($\overline{DSR}$) input. If bit D4 of the MCR is set to a 1, this bit is the equivalent of DTR in the MCR.
D6	RI	1	This bit is the complement of the Ring Indicator ($\overline{RI}$) input. If bit D4 of the MCR is set to a 1, this bit is equivalent to OUT1 in the MCR.
D7	DCD	1	This bit is the complement of the Data Carrier Detect ($\overline{DCD}$) input. If bit D4 of the MCR is set to a 1, this bit is equivalent to OUT2 in the MCR.

SCRATCH REGISTER (SCR)
ADDRESS: A2 - A0 = 111

This 8-bit Read/Write Register does not control the UART in any way. It is intended as a scratchpad register to be used by the programmer to hold data temporarily.

DIVISOR LATCH (LS) (DLL)
ADDRESS: A2 - A0 = 000, DLAB = 1

This write-only register contains the least significant byte of the divisor which is used to control the rate of the programmable baud generator.

DIVISOR LATCH (MS) (DLM)
ADDRESS: A2 - A0 = 001, DLAB = 1

This write-only register contains the most significant byte of the divisor which is used to control the rate of the programmable baud generator.

PROGRAMMABLE BAUD GENERATOR

The UART contains a programmable Baud Generator that is capable of taking any clock input (DC to 4 MHz) and dividing it by any divisor from 1 to 2^{16}-1. The output frequency of the Baud Generator is 16 x the Baud [divisor # = (frequency input)÷(baud rate x 16)]. Two 8-bit latches store the divisor in a 16-bit binary format. These Divisor Latches must be loaded during initialization in order to ensure desired operation of the Baud Generator. Upon loading either of the Divisor Latches, a 16-bit Baud counter is immediately loaded. This prevents long counts on initial load.

Tables 3 and 4 illustrate the use of the Baud Generator with crystal frequencies of 1.8432 MHz and 3.072 MHz respectively. For baud rates of 38400 and below, the error obtained is minimal. The accuracy of the desired baud rate is dependent on the crystal frequency chosen.

TABLE 3: BAUD RATES USING 1.8432 MHZ CRYSTAL

DESIRED BAUD RATE	DIVISOR USED TO GENERATE 16 X CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	2304	-
75	1536	-
110	1047	0.026
134.5	857	0.058
150	768	-
300	384	-
600	192	-
1200	96	-
1800	64	-
2000	58	0.69
2400	48	-
3600	32	-
4800	24	-
7200	16	-
9600	12	-
19200	6	-
38400	3	-
56000	2	2.86

TABLE 4: BAUD RATES USING 3.072 MHZ CRYSTAL

DESIRED BAUD RATE	DIVISOR USED TO GENERATE 16 X CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	3840	-
75	2560	-
110	1745	0.026
134.5	1428	0.034
150	1280	-
300	640	-
600	320	-
1200	160	-
1800	107	0.312
2000	96	-
2400	80	-
3600	53	0.628
4800	40	-
7200	27	1.23
9600	20	-
19200	10	-
38400	5	-

ABSOLUTE MAXIMUM RATINGS

(TA = -40°C to +85°C, VCC = 5V ± 10%, unless otherwise noted. Operation above absolute maximum ratings may permanently damage the device.)

PARAMETER	CONDITIONS	RATING
VCC Supply Voltage		+14V
Storage Temperature		–65°C to 150°C
Lead Temperature	Soldering, 10 sec.	260°C
Applied Voltage		–0.3 to V_{DD} + 0.3

DC CHARACTERISTICS

(TA = –40°C to +85°C, VCC = 5V ± 10%, unless otherwise noted.)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
VILX	Clock input Low voltage		–0.5		0.8	V
VIHX	Clock input High Voltage		2.0		V_{CC}	V
VIL	Input Low Voltage		–0.5		0.8	V
VIH	Input High Voltage		2.0		V_{DD}	V
VOL	Output Low Voltage	IOL = 4.0 mA (except XOUT)			0.4	V
VOH	Output High Voltage	IOH = 5.0 mA on all outputs except XOUT	2.4			V
IDD	Power Supply Current	See Note 1		5	10	mA
IDD	Power Supply Current	See Note 2			50	µA
IIL	Input Leakage	VCC=5.25V, GND=0V. All other pins floating.			±10	µA
ICL	Clock Leakage	VIN=0V, 5.25V			±10	µA
IOZ	3-State Leakage	VCC=5.25V, VSS=0V, VOUT=0V, 5.25V 1) Chip deselected 2) Chip & write mode selected			±20	µA
VILMR	MR Schmitt VIL				0.8	V
VIHMR	MR Schmitt VIH		2.0			V

Note 1: VCC = 5.25V, TA = 25°C; No loads on outputs. SIN, $\overline{DSR}$, $\overline{DCD}$, $\overline{CTS}$, $\overline{RI}$ = 2.4V. All other inputs = 0.4V. Baud Rate Gen. = 4 MHz; Baud Rate = 50 KHz.

Note 2: VCC = 5.5V, TA = -45°C; No output load; CMOS level inputs; Oscillator disabled or XIN = VCC

CAPACITANCE
(TA = 25°C, VCC = VSS = 0V, fc = 1 MHz, unmeasured pins returned to VSS)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
CXTAL2 Clock Input Capacitance			15	20	pF
CXTAL1 Clock Output Capacitance			20	30	pF
CI Input Capacitance			6	10	pF
CO Output Capacitance			10	20	pF

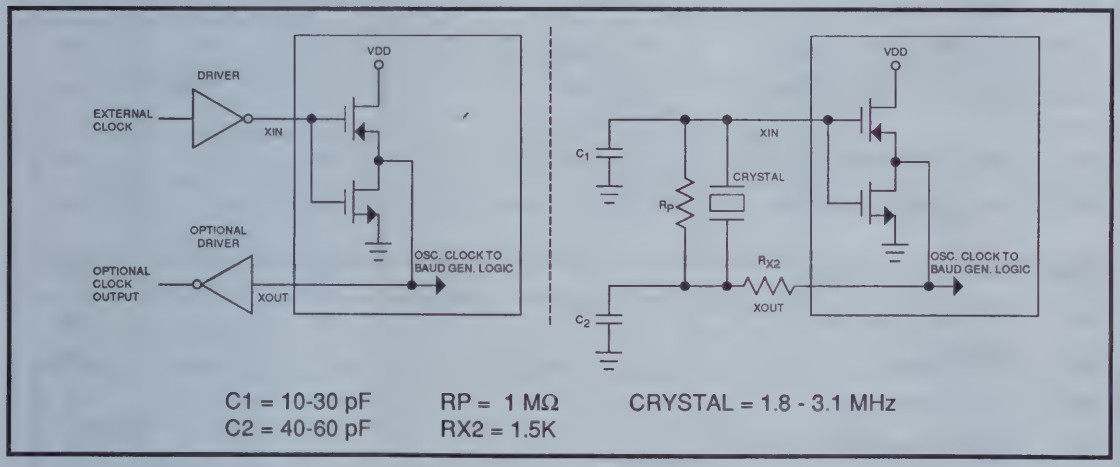


FIGURE 1: Typical Clock Circuits

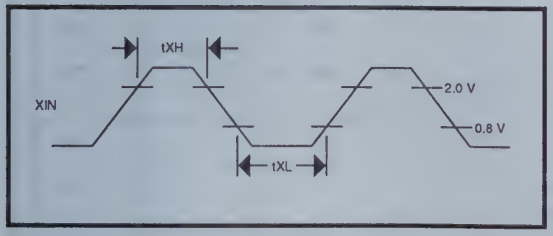


FIGURE 2: External Clock Input*
(4 MHz Maximum)

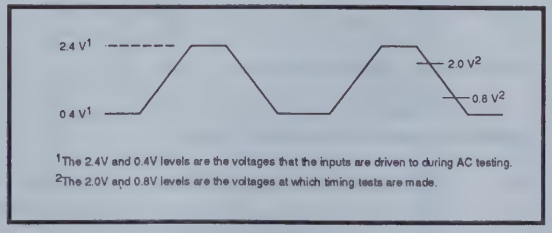

2.4 V1
0.4 V1
2.0 V2
0.8 V2
1The 2.4V and 0.4V levels are the voltages that the inputs are driven to during AC testing.
2The 2.0V and 0.8V levels are the voltages at which timing tests are made.

FIGURE 3: AC Test Points*

*All timings are referenced to valid 0 and valid 1.

AC CHARACTERISTICS (TA = -40°C to +85°C, VCC = 5V ± 10%, unless otherwise noted.)

READ & WRITE CYCLE (Refer to Figures 4 & 5.)

PARAMETER		CONDITIONS	MIN	MAX	UNITS
tCSR	$\overline{RD}$ Delay from Chip Select		50		ns
tAR	$\overline{RD}$ Delay from Address		60		ns
tRD	$\overline{RD}$ Strobe Width		125		ns
tRC	Read Cycle Delay		175		ns
RC	Read Cycle	See Note 1	360		ns
tRVD	Delay from $\overline{RD}$ to Data	100 pF load		125	ns
tHZ	$\overline{RD}$ to Floating Data Delay	100 pF load See Note 2	0	100	ns
tRA	Address Hold Time from $\overline{RD}$		20		ns
tRCS	Chip Select Hold Time from $\overline{RD}$		20		ns
tCSW	$\overline{WR}$ Delay from Select		50		ns
tAW	$\overline{WR}$ Delay from Address		60		ns
tWR	$\overline{WR}$ Strobe Width		100		ns
tWC	Write Cycle Delay		200		ns
WC	Write Cycle=tAW+tWR+tWC		360		ns
tDS	Data Setup Time		40		ns
tDH	Data Hold Time		40		ns
tWA	Address Hold Time from $\overline{WR}$		20		ns
tWCS	Chip Select Hold time from $\overline{WR}$		20		ns
tMRW	Master Reset Pulse Width		5		µs
tXH	Duration of Clock High Pulse	External Clock (4 MHz max.)	100		ns
tXL	Duration of Clock Low Pulse	External Clock (4 MHz max.)	100		ns

Note 1: RC = tAR + tRD + tRC
Note 2: Charge and discharge time is determined by VOL, VOH and the external loading.

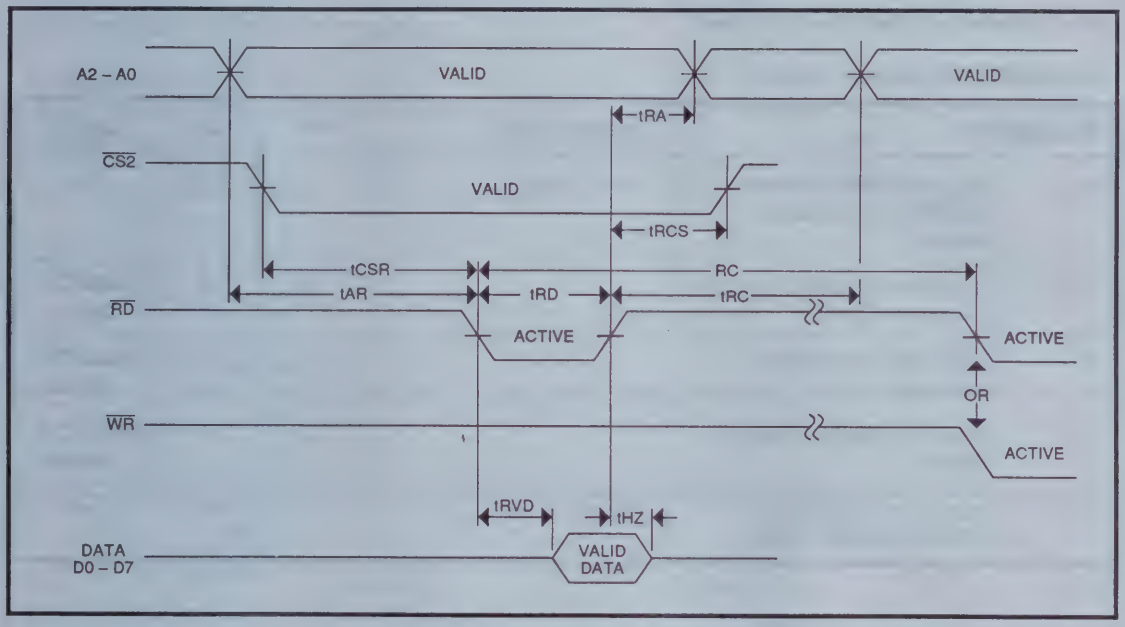


FIGURE 4: Read Cycle Timing

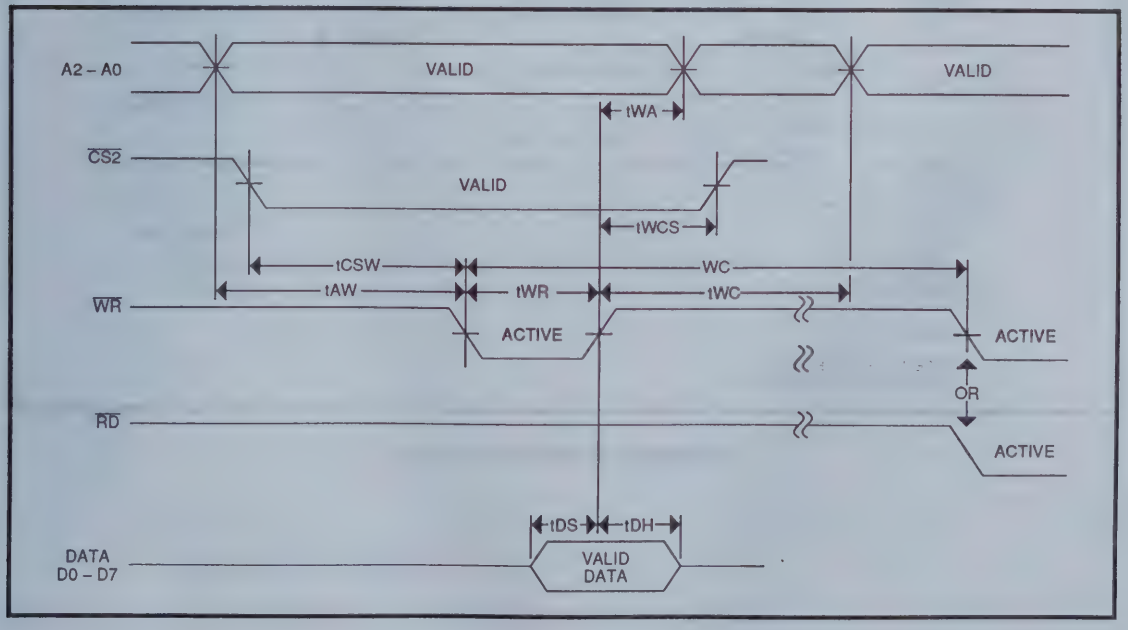


FIGURE 5: Write Cycle Timing

AC CHARACTERISTICS (Continued)

TRANSMITTER (Refer to Figure 6.)

PARAMETER		CONDITIONS	MIN	MAX	UNITS
tHR	Delay from falling edge of $\overline{WR}$ (WR THR)to Reset Interrupt	100 pF load		175	ns
tIRS	Delay form Initial INTR Reset to Transmit Start		24	40	BAUD CLK cycles
tSI	Delay from Initial Write to Interrupt		16	32	BAUD CLK cycles
tSTI	Delay from Stop to Interrupt (THRE)		8	8	BAUD CLK cycles
tIR	Delay from $\overline{RD}$ (RD IIR) to Reset Interrupt (THRE)	100 pF load		250	ns

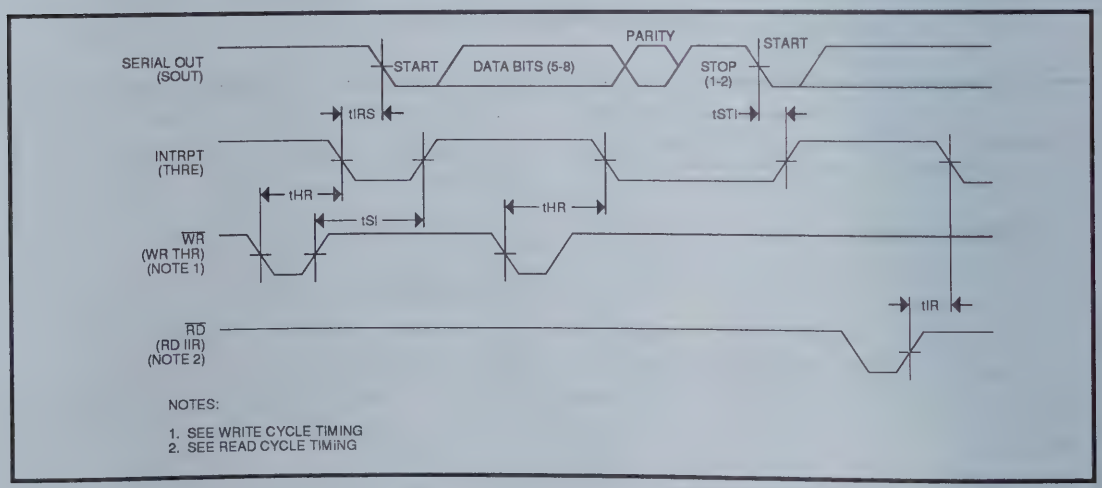


FIGURE 6: Transmitter Timing

AC CHARACTERISTICS (Continued)

MODEM CONTROL (Refer to Figure 7.)

PARAMETER		CONDITIONS	MIN	MAX	UNITS
tMDO	Delay from $\overline{WR}$ (WR MCR) to Output	100 pF load		200	ns
tSIM	Delay to Set Interrupt from Modem Input	100 pF load		250	ns
tRIM	Delay to Reset Interrupt from $\overline{RD}$ (RS MSR)	100 pF load		250	ns

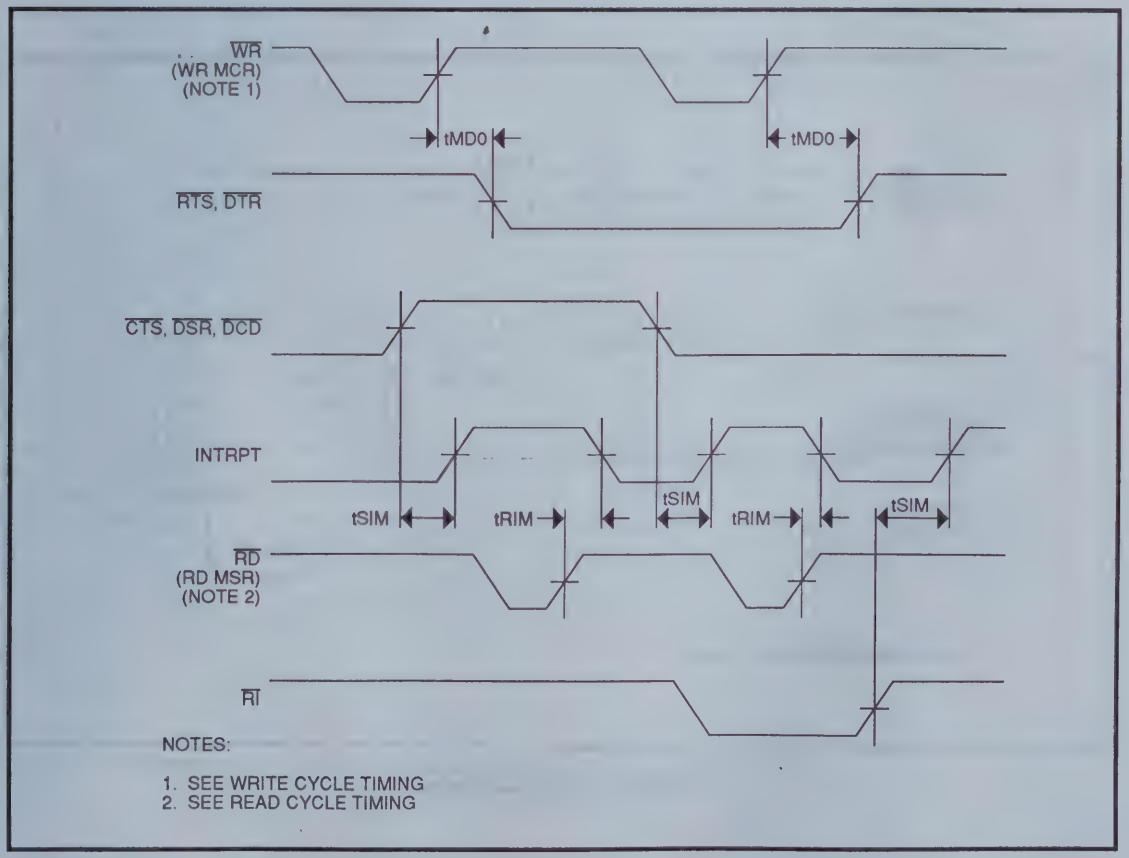


FIGURE 7: Modem Controls Timing

AC CHARACTERISTICS (Continued)

RECEIVER (Refer to Figure 8.)

PARAMETER		CONDITIONS	MIN	MAX	UNITS
tSCD	Delay from RCLK to Sample Time			2	µs
tSINT	Delay from Stop to Set Interrupt			1	BAUD CLK cycles
tRINT	Delay from $\overline{RD}$ (RD RBR/RDLSR) to Reset Interrupt	100 pF load		1	µs

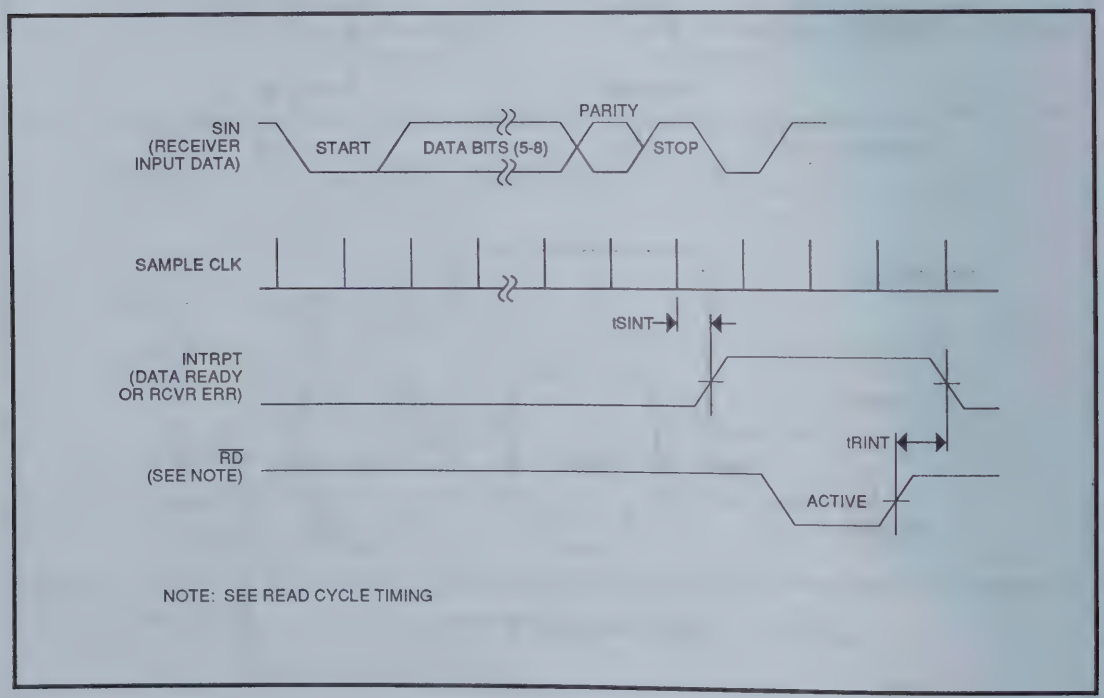


FIGURE 8: Receiver Timing

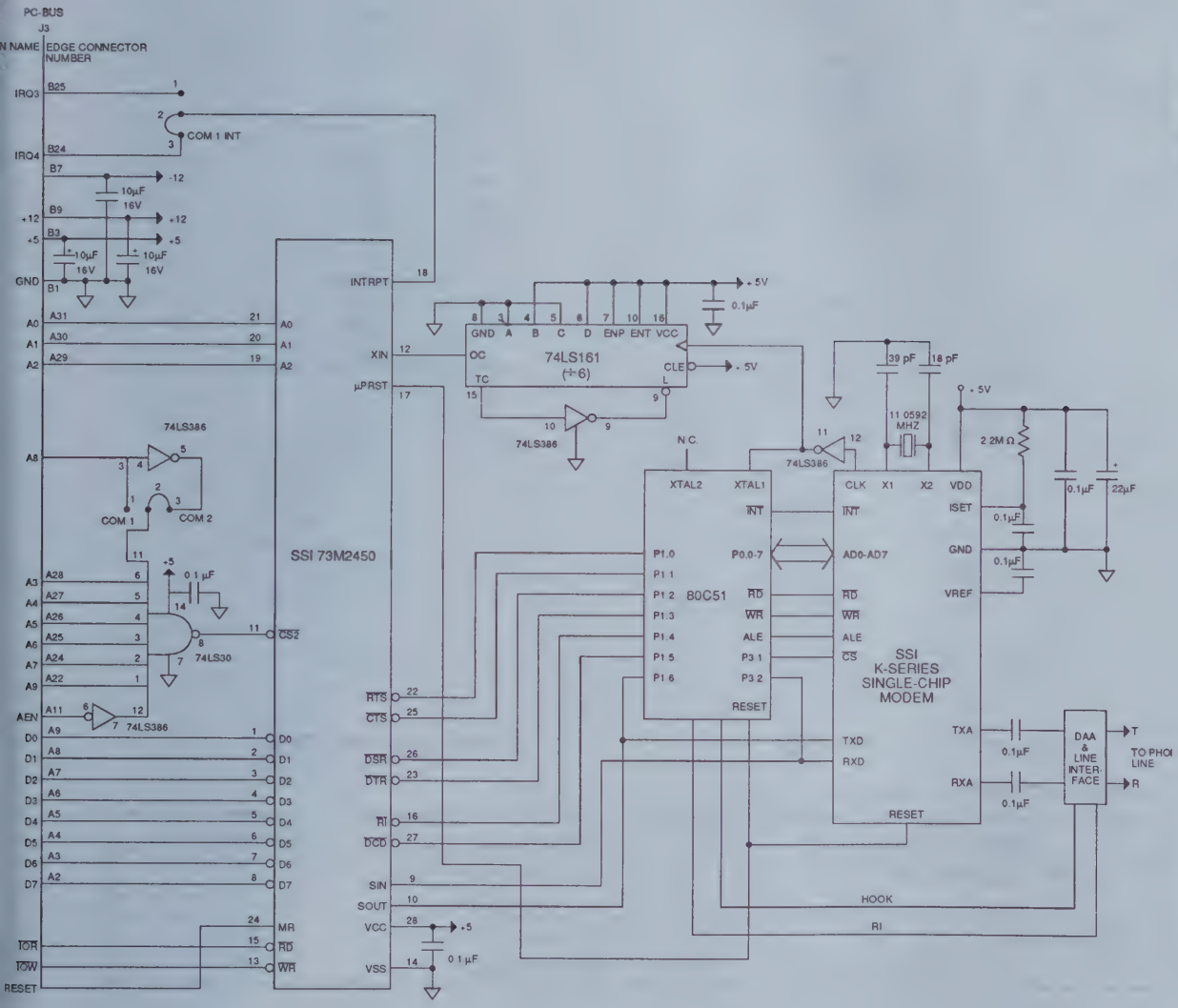
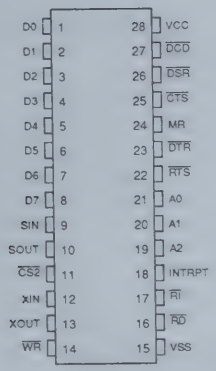


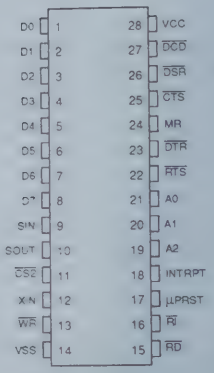
FIGURE 9: Typical Application Showing Modem Interface to PC-Bus via SSI 73M2450 UART

SSI 73M1450/2450
Universal Asynchronous Receiver/Transmitter

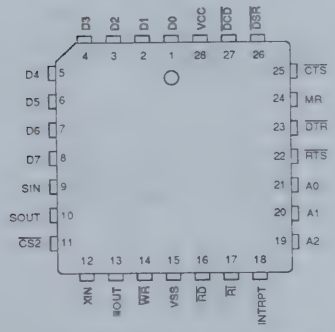
PACKAGE PIN DESIGNATIONS
(TOP VIEW)



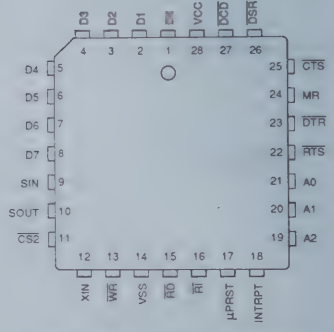
SSI 73M1450 28 - Pin DIP



SSI 73M2450 28 - Pin DIP



SSI 73M1450 28 - Pin PLCC



SSI 73M2450 28 - Pin PLCC

ORDERING INFORMATION

PART DESCRIPTION		ORDER NO.	PKG. MARK
SSI 73M1450	28-pin PDIP	SSI 73M1450-IP	73M1450-IP
	28-pin PLCC	SSI 73M1450-IH	73M1450-IH
SSI 73M2450	28-pin PDIP	SSI 73M2450-IP	73M2450-IP
	28-pin PLCC	SSI 73M2450-IH	73M2450-IH

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Section 3

MODEM/ MODEM SUPPORT

SSI 73M214
Modem
Analog Front End

July, 1989

DESCRIPTION

The SSI 73M214 is a complete analog front end IC for digital signal processor based V.22 bis, V.22, Bell 212A, V.21, and Bell 103 compatible modems.

The 73M214 provides bandsplit filters, compromise equalization, and digitally controlled receive gain and transmit attenuation. An 8-bit A/D convertor is available for receive signal processing, and on-chip modulators provide the QAM, PSK, and FSK transmit signals, making it unnecessary for the DSP to perform the transmit functions. A tone generator is used to produce DTMF, answer, and guard tones while an analog loopback mode allows system testing. Carrier, answer, and call progress tone detection is provided.

The SSI 73M214 uses two busses to transfer data and control information. A 4-bit address/data multiplexed bus is used for connection to a control microprocessor (8031 typical) which performs the scrambler/descrambler, buffer/debuffer, system control, data, and user interface functions. A serial data bus transfers received digitized data as well as receiver status information to a standard DSP (7720 typical). The DSP also sends the 73M214 receive timing and gain control information over the serial bus.

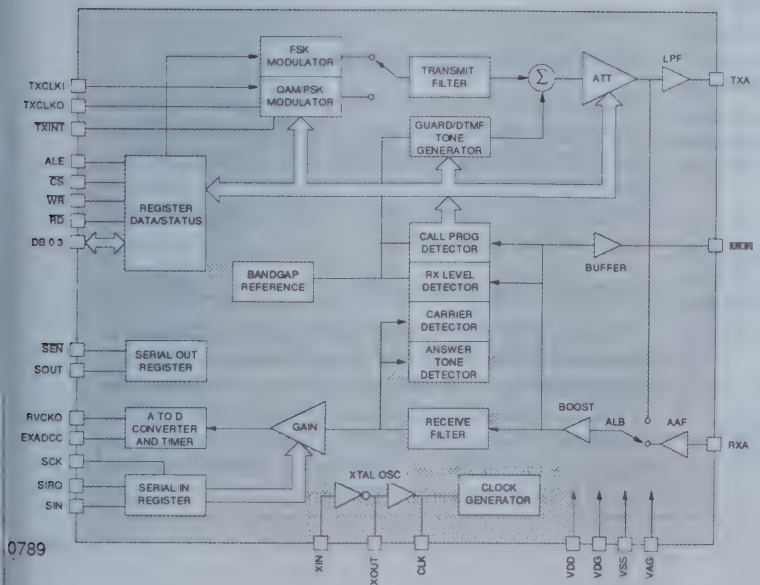
(Continued)

FEATURES

- Analog front end for DSP-based V.22 bis modems
- Complete modulators for QAM/DPSK (V.22bis, V.22, Bell 212) and FSK (Bell 103 and V.21)
- Programmable receive gain/transmit attenuation
- 8-bit ADC with reference, sample, and hold
- Band split filters with compromise equalization
- Analog loopback test mode
- Serial interface for receive processing
- Parallel interface for transmitter and control
- Timer for transmit synchronization
- Programmable timer for receiver data clock recovery
- Carrier, call progress, and answer tone detectors
- Audio monitor for audible call status
- DTMF, guard tone, and answer tone generation
- Crystal oscillator with echo
- Low power CMOS (± 5V at < 300 mW)
- 28-pin plastic DIP or PLCC surface mount package

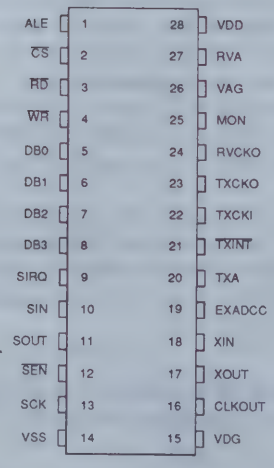
3

BLOCK DIAGRAM



0789

PIN DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component

SSI 73M214
Modem
Analog Front End

DESCRIPTION (Continued)

The SSI 73M214 is ideal for use in self-contained or integral intelligent modem products requiring the benefits of 2400 bit/s full duplex operation while maintaining compatibility with existing standards at speeds down to 300 bit/s. By integrating the majority of the analog functions needed on a single CMOS IC, system complexity and cost is reduced without compromising performance or features.

OPERATION

The SSI 73M214 provides the analog front end processing for a V.22 bis 2400 bit/s modem. The SSI 73M214 includes band-split filters, fixed U.S. compromise line equalizer, programmable gain/attenuator for receive and transmit functions, FSK/QAM modulators, differential encoder, and an analog to digital converter. The 73M214 interfaces to an external digital signal processor and inexpensive control microprocessor to complete the modem function.

FUNCTIONAL DESCRIPTION

The 73M214 allows selection of 600 bit/s, 1200 bit/s, or 2400 bit/s transmission modes. The 73M214 generates the bit rate clocks RVCKO (receive) and TXCKO (transmit) and a baud rate clock $\overline{\text{TXINT}}$. In the synchronous modes, there is a fixed phase relationship between TXCKO and $\overline{\text{TXINT}}$. Each case here assumes that the receive timer is in internal timing mode, otherwise RVCKO is high. Register CR0 selects a mode (there are three synchronous modes and one asynchronous mode). In internal synchronous mode, the 73M214 generates an accurate bit rate clock, TXCKO.This may be used for data transfers from the DTE to the microprocessor. The microprocessor sends the latest quadbit (or dibit), which is latched into the modulator on the falling edge of $\overline{\text{TXINT}}$. Pin TXCKI is ignored in internal synchronous mode.

In external synchronous mode the data rate clock from the DTE should be connected to the TXCKI pin. TXCKI is used to generate phase locked clocks TXCKO and $\overline{\text{TXINT}}$ (TXCKI's falling edge synchronously resets an internal counter).

Please consult Silicon Systems headquarters for more detailed data sheet. (714) 731-7110.

RECEIVE SIDE PROCESSING

The received signal from the line passes through an anti-alias filter with adjustable gain, then through a band-split filter with selectable compromise line equalization, after which it is amplified by a programmable gain stage. The analog signal is converted to an 8-bit, 2's complement number for the digital signal processor.The ADC output and AGC gain word are transferred serially between the DSP and SSI 73M214. A programmable timer is included for use in the data clock recovery loop. Answer tone, carrier, and imprecise call progress detectors are included for modem smart dialing capability.

TRANSMIT SIDE PROCESSING

In QAM (DPSK) mode, the quadbit (dibit) is transferred to the SSI 73M214 where it is differentially encoded and then passed through a baseband filter. The baseband information is modulated up to 1200 Hz or 2400 Hz. A band-split filter shapes the modulator output and provides compromise line equalization. The transmitted spectrum has the recommended square root of 75% raised cosine shaping. Guard tone is added to the signal after the filter, and the pro-grammable attenuator sets the transmit amplitude. Finally, a smoothing filter eliminates out-of-band energy generated by the switched-capacitor filters.

In FSK mode, a programmable tone generator acts as the modulator. The modulator output passes through the band-split and smoothing filters as in the QAM mode.

MICROPROCESSOR INTERFACE

The SSI 73M214 acts as a peripheral to the microprocessor (e.g. Intel 8051, Zilog Z8601, Motorola 6801) on a 4-bit multiplexed address/data bus. Control and status information are stored in registers on the 73M214. Transmit data is also sent from the microprocessor over the bus in 4 bit nibbles.

RECEIVE DSP INTERFACE

The SSI 73M214 interfaces to a digital signal processor over two serial ports.The serial interface is directly compatible with the NEC/OKI 7720 or 77C20. The 73M214 can also be interfaced with parallel bus signal processors using standard TTL 7400 series shift registers. The digital sample from the A/D convertor is sent to the DSP on the serial output port, and the AGC gain

RECEIVE DSP INTERFACE (Continued)

value is sent from the DSP to the 73M214 on the serial input port. Both serial ports transfer 16 bits simultaneously under timing control generated by the 73M214.

In slave mode TXCKO and $\overline{\text{TXINT}}$ are phase locked internally to RVCKO (RVCKO's falling edge synchronously resets an internal counter). Pin TXCKI is ignored in slave mode. If the internal receive timer is not being used, slave mode can be implemented by putting the 73M214 in external synchronous mode and externally connecting the recovered receiver bit rate clock to TXCKI.

Asynchronous mode operation is the same as internal synchronous mode, except TXCKO and RVCKO are high.

SERIAL DSP INTERFACE

The serial DSP Interface provides for communication between the DSP and the 73M214. A programmable receive timer block which provides for adjustment of the ADC sampling rate is included on the 73M214. It may be used as part of the data clock recovery loop. The receive timer control bits RvT1 and RvT0 (TR0) select one of four possible ADC modes: off, external timing, internal timing 7200 Hz, or internal timing 9600 Hz. The DSP, through serial port SIN (bits 8-9) provides for adjustment to the internal sampling clock rates either 7200 Hz ± 1 µsec or 9600 Hz ± 1 µsec. The falling edge of SEN corresponds to the following events:

1) The signal on RvA is sampled and an 8-bit analog-to-digital conversion begins.

2) The previous 8-bit ADC sample and the status bits are loaded into a register for serial shifting out of port SOUT to the DSP. See Table 1.

3) The previous gain & timer bits from the DSP are latched into the 73M214 register and the current DSP serial word is shifted into port SIN. See Table 2.

SERIAL DSP TIMING

For the serial receive processor interface, signal SIRQ is generated by the NEC/OKI 77C20 and must be high to send SIN data. If it is low during a serial transmission, SOUT remains active but SIN becomes inactive and the 73M214 will continue to use the last gain/timer value. SCK from the 73M214 is the serial shift clock.

QAM/DPSK ENCODER/MODULATOR

The quadbits sent to the 73M214 are differentially encoded according to the CCITT V.22bis specification. The encoded quadbits are then passed through an FIR baseband filter. The baseband signal thus generated is modulated by the carrier at either 1.2 KHz or 2.4 KHz. The FSK modulator frequency modulates the data in a continuous phase manner. FSK operation is asynchronous and is determined by the appropriate control bits.

TABLE 1: Serial Output, 16-bit word, bit 0 (LSB) is shifted out first

BIT NO.	15-12	11	10	9	8	7-0
Output Data	FAST C.D.	SLOW C.D.	A.T.	CPD	RCV LEVEL	ADC Output

TABLE 2: Serial Input, 10-bits, bit 0 (LSB) is shifted first

BIT NO.	15-10	9-8	7	6-0
Input Data	X	RCV TIMER CONTROL	X	Gain Word (Log) MSB-LSB

TONE GENERATOR

The tone generator will output a dual-tone (DTMF) or a single tone (FSK, answer tone, or guard tone) on the TxA line if the appropriate control bits are enabled. The control bits are found in register TR0 and TR1. The tone is specified by register TR1. Sixteen dual-tone combinations and 7 single tones are possible. DTMF has priority over single tones. The tone generator macro cell consists of 4 blocks: tone selection and control, two programmable down counters, two three-level six-step square wave generators, and a 3-pole ladder filter with programmable gain and pole setting.

BAND SPLIT FILTERS

The band-split filters provide attenuation for out-of-band noise components and near-end cross talk. The filters also provide some of the square root 75% raised cosine shaping for minimum inter-symbol interference. Receive delay equalization can be bypassed by using the RvF1 bits. The receive filter can be bypassed for direct access to the ADC with the RvF0 bit.

PROGRAMMABLE GAIN STAGE

The programmable gain stage is part of an AGC loop which is controlled by the receive digital signal processor. The gain increases monotonically with increasing gain word. The 7-bit gain setting covers a 48 dB range with 0.375 dB steps. Minimum gain of 0 dB corresponds to 0000000, maximum gain of 48 dB is 1111111.

ADC

The 8-bit analog to digital converter provides a 2's complement representation of the sampled analog voltage. The sample and hold function is incorporated in this switched-capacitor ADC.

TRANSMIT ATTENUATOR

The programmable transmit attenuator allows the control processor to set the transmit power level. If the attenuator control bits are set to 0000, the attenuator acts as a unity gain stage. The attenuation increments by 1 dB per LSB.

In addition to the user programmable attenuator, there is an internally controlled attenuator for the QAM/DPSK modulated signal. The attenuation value is determined by the guard tone selected and assures that modulated data plus guard tone gives 0 dBm prior to the transmit attenuator regardless of the guard tone setting.

DETECTORS

The special detect circuitry checks the received analog signal for special conditions. The conditions checked for are the presence of a carrier (ie. energy in the receive band), the presence of an answer tone (2100 or 2225 Hz), and the presence of a call progress signal.

IMPRECISE CALL PROGRESS DETECTOR

The call progress detector monitors activity on the line. This detector is an imprecise call progress detector - the on/off envelope of the signal is replicated as a 1/0 in the CPD bit of the SR register. The detector consists of a bandpass filter followed by a peak detector. The 3 dB points of the bandpass filter are 350 Hz and 620 Hz. Dial-tone, busy-signal, ringback and reorder are composed of at least one tone in this band.

PRECISE ANSWER TONE DETECTOR

The receive filter output is fed to a highly selective frequency discriminator controlled by the ABT1 and ABT0 bits of the DCR register to detect 2100 and 2225 Hz answer back tones. The frequency discriminator is gated by the output of the carrier detector to provide amplitude discrimination.

CARRIER DETECTOR

The carrier detector detects the presence of a signal in the receive band. When energy is detected, the CAR bit of the SR register is set to "1." The detector uses a peak-to-peak amplitude detecting scheme which requires knowledge of the Peak/Rms ratio of the waveform to be detected. This information is obtained from the data rate control register (CR0) bits DR1 and DR0. The fast carrier detect is an imprecise carrier detector that is derived from the short term peak-to-peak amplitude in the carrier detector. The detector output will be erratic for small signals with high peak-to-rms values. The fast carrier is output on the FCAR bit of the serial output port.

RECEIVE LEVEL DETECTOR

The receive level detector indicates whether the signal present at RvA is too large to permit the use of the receive gain (RvGE) of 12 dB prior to the band-split filters. When the RvL bit of the SR register is a "1," the signal is too large to use the gain. A fixed, switchable 12 dB gain is provided ahead of the band-split filters to be used when the total received signal (received signal + near-end signal) is more than 12 dB below the maximum allowed input voltage.

PIN DESCRIPTION

POWER

NAME	PIN NO.	I/O	DESCRIPTION
VDD	28	I	Positive voltage supply (+5V)
VSS	14	I	Negative voltage supply (-5V)
VAG	26	I	Analog Ground
VDG	15	I	Digital Ground

ANALOG INTERFACE

NAME	PIN NO.	I/O	DESCRIPTION
RVA	27	I	Receive side analog input from line.
TXA	20	O	Transmit side analog output to line. Modulator output as well as DTMF output uses this pin.
XIN	18	I	Crystal connection, 7.3728 MHz crystal, or externally generated 7.3728 MHz oscillator input.
XOUT	17	I	Crystal connection, 7.3728 MHz crystal.
CLKOUT	16	O	Crystal oscillator output echoed for system use.
MONITOR	25	O	Analog output for call progress tone monitoring. Can be muted (see Control Bits)

MICROPROCESSOR INTERFACE

NAME	PIN NO.	I/O	DESCRIPTION
DB0-DB3	5,6,7,8	I/O	(Bidirectional, 3 state) Address/Data Bus.
$\overline{CS}$	2	I	Chip Select. A low allows a read or write cycle to occur. DB0-DB3 can not be written to or read from if $\overline{CS}$ (latched) is not low. $\overline{CS}$ is latched on the falling edge of ALE.
$\overline{RD}$	3	I	Read. A low requests a read of the 214 registers. Data cannot be ouput on DB0-DB3 unless both $\overline{RD}$ and the latched $\overline{CS}$ are low.

MICROPROCESSOR INTERFACE (Continued)

NAME	PIN NO.	I/O	DESCRIPTION
$\overline{WR}$	4	I	Write. A low informs the 214 that data is available on DB0-DB3 for writing into an internal register. Data is latched on the rising edge of $\overline{WR}$. No data is written unless both $\overline{WR}$ and $\overline{CS}$ are low.
ALE	1	I	Address strobe line for multiplexed addressed/data bus. The falling edge of ALE latches the address on DB0-DB3 and the chip select $\overline{CS}$.

TRANSMIT INTERFACE

NAME	PIN NO.	I/O	DESCRIPTION
TXCKI	22	I	Transmit clock input, used for the external synchronous mode. In external synchronous mode, all clocks for the modulator are synchronized to this bit rate clock.
TXCKO	23	O	Bit rate transmit clock output, provided when the modulator is in a synchronous mode. In FSK, or modulator off modes, this pin is pulled high.
$\overline{TXINT}$	21	O	Transmit interrupt, active low. Baud rate clock which requests a new quadbit for the modulator. Active in the 1200 or 2400 bit/s modes only. Forced high otherwise.

RECEIVE INTERFACE

NAME	PIN NO.	I/O	DESCRIPTION
RVCKO	24	O	Bit rate receive clock output from receive timer. Output is active in 2400 bps or 1200 bit/s transmission when the internal timer is used and the modulator is operating in a synchronous mode. Otherwise the output is forced high.
SOUT	11	O	Output serial port - sends ADC/status bits to DSP.
SIN	10	I	Input serial port receive gain and timer bits from DSP.
SIRQ	9	I	Serial input request. SIRQ high signifies that data is available to shift into SIN port - SIRQ low causes SIN port to retain past data and not shift. SIRQ is latched by $\overline{SEN}$ falling edge. SIRQ does not affect the shifting of the SOUT port.
$\overline{SEN}$	12	O	Serial enable pin. Enables serial shifting on SOUT and SIN ports. Signal is low for 16 cycles of SCK.
SCK	13	O	Shift clock generated on 214 for serial ports SIN and SOUT. Clock rate is 184 KHz and is resychronized to receive timer every $\overline{SEN}$ falling edge.
EXADCC	19	I	External ADC convert clock input which is required if the internal receive timer is not being used. The rising edge of EXADCC is aligned to an internal 922 KHz clock; it starts an ADC conversion and serial shifting over the SIN and SOUT ports.

REGISTER SUMMARY

CR0 (00H) Control Register 0

BIT	NAME	DESCRIPTION	
3	DR1	Data Rate	00 = Off 01 = FSK (FBK=0 →Bell 103; FBK=1 →V. 21)
2	DR0		10 = PSK (FBK=0 →1200 bit/s; FBK=1 →600 bit/s) 11 = QAM
1	TxM1	Transmit Mode	00 = Asynchronous 01 = Internal Synchronous
0	TxM0		10 = External Synchronous 11 = Slave Synchronous

CR1 (01H) Control Register 1

BIT	NAME	DESCRIPTION
3	FBK	Fall Back
2	RvF1	Bypass receive Equalizer
1	RvF0	Bypass receive Filter
0	TxSQB	Transmitter Squelch

CR2 (02H) Control Register 2

BIT	NAME	DESCRIPTION
3	ATT3	Transmit Attenuator
2	ATT2	
1	ATT1	
0	ATT0	

REGISTER SUMMARY (Continued)

CR3 (03H) Control Register 3

BIT	NAME	DESCRIPTION	
3	TST	Test	1 = Test mode
2	ALBK	Analog Loopback	1 = Loopback
1	RvGE	12 dB Receive Gain	1 = 12 dB 0 = 0 dB
0	ORIG	Originate/Answer	1 = Originate 0 = Answer

DR (04H) Detect Register

BIT	NAME	DESCRIPTION	
3	ABT1		10 detect 2100 only
2	ABT0	Answer Tone Detector Control	00/11 detect 2100 or 2225 01 detect 2225 only
1	MONEN	Speaker Enable	1 = Speaker on 0 = Speaker off
0	RST	Reset	1 = Reset

SR (05H) Status Register (Read only)

BIT	NAME	DESCRIPTION
3	CAR	Carrier Detect
2	ADT	Answer Tone Detect
1	CPD	Call Progress Detect
0	RvL	Receive Level Large

REGISTER SUMMARY (Continued)

TR0 (06H) Tone Register 0

BIT	NAME	DESCRIPTION	
3	RvT1	ADC Control	00 = ADC stopped 01 = External control (use EXADCC)
2	RvT0		10 = Internal 7200 Hz 11 = Internal 9600 Hz
1	ST	Single Tones	
0	DTMF	Dual Tones	

TR1 (07H) Tone Register 1

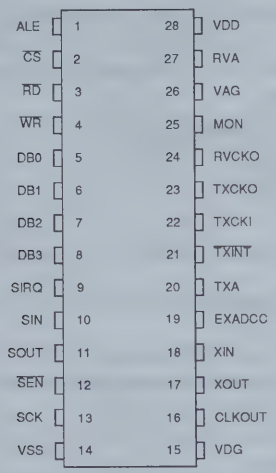
BIT	NAME	DESCRIPTION			
		Single Tone		Dual Tone	
3	TRB3	00H=2025 01H=2225	08H=2225 09H=2100	00H=941, 1633 01H=697, 1209	08H=852, 1336 09H=852, 1477
2	TRB2	02H=1070 03H=1270	0AH=N/A 0BH=N/A	02H=697, 1336 03H=697, 1477	0AH=941, 1336 0BH=941, 1209
1	TRB1	04H=1800 05H=550	0CH=1850 0DH=1650	04H=770, 1209 05H=770, 1336	0CH=941, 1477 0DH=697, 1633
0	TRB0	06H=N/A 07H=N/A	0EH=1180 0FH=980	06H=770, 1477 07H=852, 1209	0EH=770, 1633 0FH=852, 1633

QBR (08H) Quadbit Register

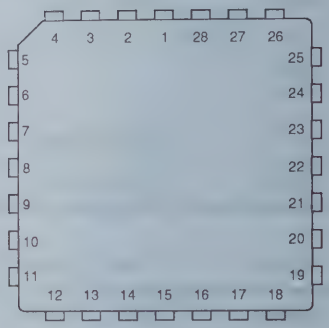
BIT	NAME	DESCRIPTION	
3	QBR3	Quadrant	00 = i +90 01 = ii 0
2	QBR2	Quadrant	10 = iii +180 11 = iv +270
1	QBR1	Point In Quadrant i	00 = (1,1) 01 = (3,1) (DPSK Points)
0	QBR0		10 = (1,3) 11 = (3,3)

SSI 73M214
Modem
Analog Front End

PACKAGE PIN DESIGNATIONS
(TOP VIEW)



28-pin DIP



28-pin PLCC*

*PLCC Pinout is the Same as the 28-Pin DIP

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 73M214		
28-pin Plastic DIP	SSI 73M214-IP	73M214-IP
28-pin Ceramic DIP	SSI 73M214-IC	73M214-IC
28-pin Plastic Leaded Chip Carrier	SSI 73M214-IH	73M214-IH

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SSI 73M223
1200 Baud FSK Modem

July, 1989

DESCRIPTION

The SSI 73M223 modem device receives and transmits serial and binary data over existing telephone networks using Frequency Shift Keying (FSK). It provides the filtering, modulation, and demodulation to implement a serial, asynchronous data communication channel. The SSI 73M223 employs the CCITT V.23 signaling frequencies of 1302 and 2097 Hz, operating at 1200 baud, and is intended for half duplex operation over a two-line system.

The SSI 73M223 provides a cost-effective alternative to existing modem solutions. It is ideally suited for R.F. data links, credit verification systems, point-of-sale terminals, and remote process control.

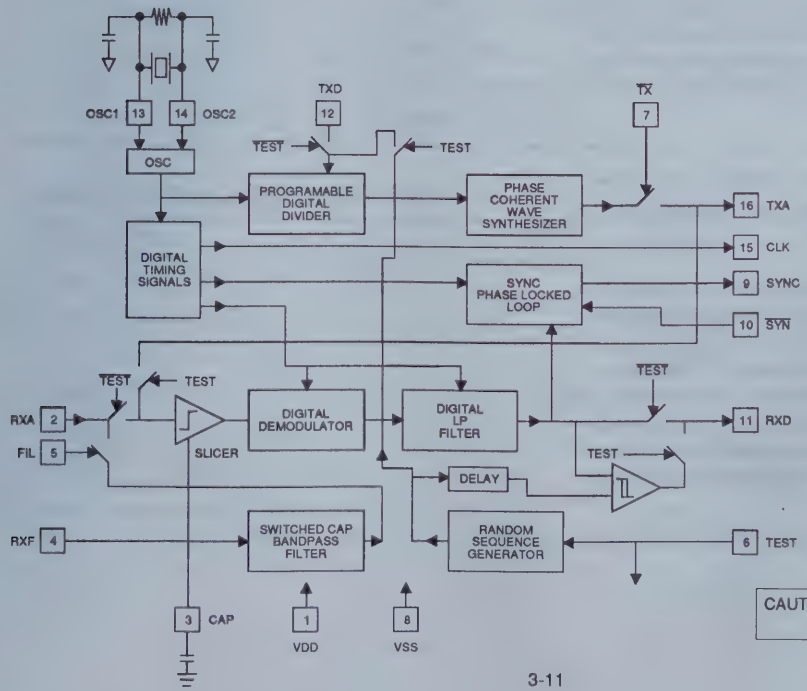
CMOS technology ensures small size, low-power consumption and enhanced reliability.

FEATURES

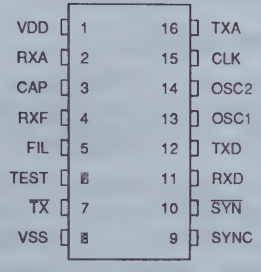
- Low cost FSK Modem
- 1200 baud operation
- CMOS switched capacitor technology
- Built-in self-test feature
- On-chip filtering, and Modulation/Demodulation
- Uses CCITT V.23 frequencies
- On chip crystal oscillator
- Low power/High reliability
- 16-pin plastic package

3

BLOCK DIAGRAM



PIN DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

FUNCTIONAL DESCRIPTION

The SSI 73M223 has four main functional sections: timing, transmit, receive, and test. Each section of the chip will be individually described below.

TIMING

The timing section contains the oscillator (OSC) and random logic which generates digital timing signals used throughout the chip. The time base can be derived from 3.18MHz crystal or an external digital input. The digital timing logic divides the oscillator frequency to give a 1200Hz output than can be used for system timing. The signaling frequencies are 1302Hz for logic "1" and 2097Hz for logic "0". The modem will operate with clock inputs from 330KHz to 3.3MHz. However, the signaling frequencies and the system timing will be different.

TRANSMITTER

The SSI 73M223 transmitter consists of a programmable divider that drives a coherent phase frequency synthesizer. The programmable divider is digitally controlled via the Data Input pin (TXD). The output of the divider clocks a 16 segment phase coherent frequency synthesizer. A sine wave is constructed by eight weighted capacitors which are the inputs to a high pass filter. The synthesized signal is output directly to the transmit pin TXA. The transmit signal can be disabled by using the digital control pin TX.

RECEIVER

The SSI 73M223's receiver is comprised of three sections: the input bandpass filter, the synchronization loop, and the demodulator.

The input bandpass filter is a four pole Butterworth filter, implemented using switched capacitor technology. This filter reduces wideband noise which significantly improves data error rates. The SSI 73M223 can be configured with the bandpass filter in series with the receiver by setting FIL = 1 and inserting the received signal at RXF. The bandpass filter can be deleted from the system by setting FIL = 0 and inputting the received signal through RXA.

The demodulator is used to detect a received mark or space.

The synchronization for sampling the digital output at RXD is derived from a digital phase locked loop. The phase locked loop is clocked at 16 times the bit rate with a maximum lock period of 8 clocks to lock on the data output signal.

SELF TEST MODE

The SSI 73M223 features an autotest mode which provides easy field test capability of the chip's functionality. The modem is placed in the test mode by taking the test pin high. In the test mode the Data Input pin is disconnected and the programmable divider is driven by a pseudo random PN sequence generator and the transmitter's output is connected to the receiver's input. The input data to the programmable divider is delayed by the system delay time and compared to the digital output on sync transitions. If the detected data matches the delayed input data from the PN sequence counter, the SSI 73M223 is properly functioning as indicated by RXD low. A high on the RXD pin indicates a functional problem on the SSI 73M223.

PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1	VDD	Positive Supply Voltage
2	RXA	Receive Analog Input. Analog input from the telephone network.
3	CAP	Capacitor. Connect a 0.1µF capacitor between Pin 3 and ground (VSS).
4	RXF	Filtered Receive Analog Input
5	FIL	Analog Input Control. A logical 1 selects the filtered input. A logical 0 selects the non-filtered input.
6	TEST	Self-Test Mode Control. Normal operation when a logical 0.A logical 1 places the device into the self-test mode. A low appears at RXD, to indicate a properly functioning device.
7	$\overline{TX}$	Transmitter Control. A logical 0 selects transmit mode. A logical 1 selects a stand-by condition forcing TXA to VDD/2 VDC.
8	VSS	Ground
9	SYNC	Synchronized Output. Digital output synchronized with the received signal and used to sample the received eye pattern.
10	$\overline{SYN}$	Sync Disable. A logical 1 input disables the phase locked signal from the received data and locks it to the 1200Hz reference.
11	RXD	Receiver Digital Output
12	TXD	Transmitter Digital Input
13	OSC_1	Crystal Input (3.1872MHz) or External Clock Input
14	OSC_2	Crystal Return
15	CLK	1200Hz Squarewave Output. Can drive up to 10 CMOS loads.
16	TXA	Transmitter Analog Output

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Power Supply Voltage (VDD-VSS)	14	V
Analog Input Voltage at RXA	- 0.3 to VDD	V
Analog Input Voltage at RXF	- 3 to VDD	V
Digital Input Voltage	VSS - 0.3 to VDD + 0.3	V
Storage Temperature Range	- 65 to + 150	°C
Operating Temperature Range	- 25 to + 70	°C
Lead Temperature (10 secs soldering)	260	°C

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, 4.5 <VDD <13 VDC, VSS = 0 VDC, -25° C <TA

POWER SUPPLY

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
VDD Voltage Supply Range		4.5		13	V
Supply Current	VDD = 5V 25° C		2.0		mA
	VDD = 12V 25° C		5.0		mA
Digital Inputs					
Input Low Voltage VIL		VSS - 0.3		VSS + 1.5	V
Input High Voltage VIH		VDD - 1.5		VDD + 0.3	V
Input Low Current IIL		-1			µA
Input High Current IIH				1	µA
Digital Outputs					
Output Low Voltage VOL	IOL < 1µA			0.05	V
Output High Voltage VOH	IOL < -1µA VDD = 5V	4.95			V
Output Low Current IOL	VOL = 0.4V VDD = 5V	0.5			mA
Output High Current IOH	VOH = 4.5V VDD = 5V	-0.2			mA
Analog Input Level @ RXA	Centered at VDD/2 + 0.5V	0.2		VDD/4	Vpp
Analog Input Level @ RXF	*DC Level between VDD & VSS	0.2		VDD/2	VDC
Error Rate	S/N = 8dB Input @ RXF			5×10^{-3}	
Analog Output Level @ TXA	RL ≥ 10K $\overline{TX}$ = 0		VDD/4		Vpp
	$\overline{TX}$ = 1		VDD/2		VDC
Output Frequency @ TXA	XTAL = 3.1872MHz TXD=1		1302		Hz
	TXD=0		2097		Hz
Output Harmonics	2nd to 14th Harmonics		-60	-50	dB
	15th Harmonic			-20	dB
Input Filter (RFX)	*Input = 200 m Vpp to VDD/2 Vpp				
Lower 3dB Corner			760		Hz
Upper 3dB Corner			2625		Hz

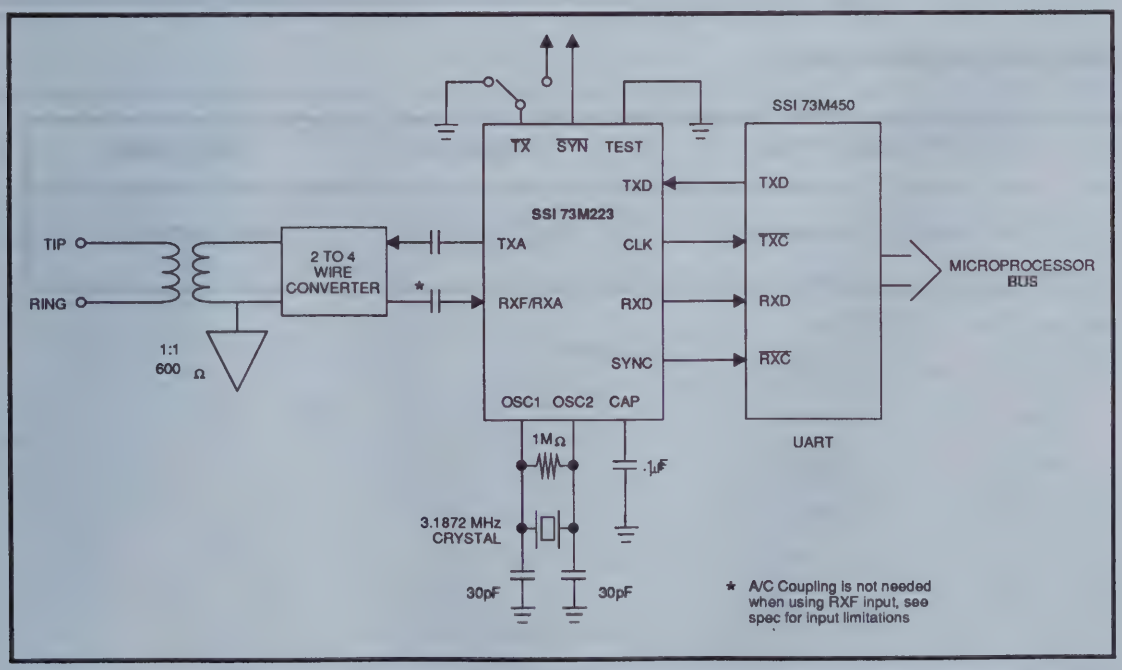
* Note: The SSI 73M223 RXF input is AC coupled internally but the DC value of the input must be between the two supplies VDD & VSS.

APPLICATION INFORMATION

The SSI 73M223 modem chip allows low cost communications in a private network, utilizing twisted pair telephone wires. This chip is the prime choice of those designers who require an efficient, high performance modem solution for dedicated private networks, HDX dial-up and other specialized applications. Such applications include credit verification systems, point-of-sale terminals, remote process control, private data links and acoustic modem designs.

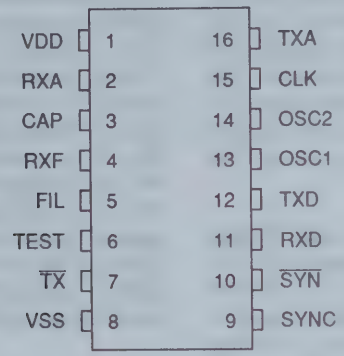
Utilizing a crystal input of 3.1872MHz, the SSI 73M223 is a 1200 Baud, FSK modem. The signaling frequencies generated are 1302Hz for a logic "1" and 2097Hz for a logic "0". Crystals with frequencies varying between 330KHz to 3.3MHz can be used. The baud rate and signaling frequencies vary linearly with variation in crystal frequency.

A typical implementation on the SSI 73M223 is shown in the figure below. An SSI 73M450 UART receives data to be transmitted from a microprocessor bus. The UART sends the data in a serial format to the SSI 73M223 modem after inserting the necessary start and stop bits. The modem transmits this data to the far end via the TXA pin. The figure depicts a half-duplex operation. Full-duplex operation can be implemented by utilizing separate transmit and receive circuits. A USART can be used instead of a UART if synchronous operation is desired. With synchronous operation, the USART uses the modem's SYNC signal to sample the received data, and the modem's CLK signal to send data to be transmitted.



SSI 73M223 TYPICAL APPLICATION

PACKAGE PIN DESIGNATIONS
(TOP VIEW)



16-PIN DIP

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 73M223 16 Pin Plastic DIP	SSI 73M223 - CP	SSI 73M223 - CP

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SSI 73M3522
Bell 212A/V.22 Modem Filter

July, 1989

3

DESCRIPTION

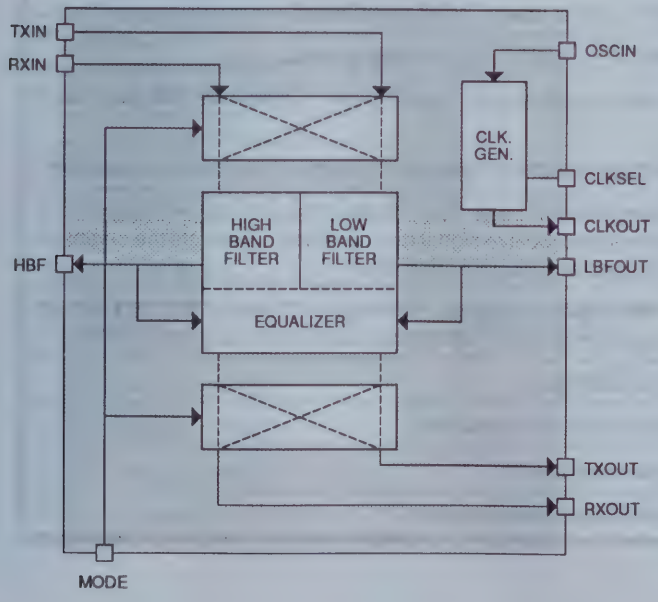
The SSI 73M3522 is a 16 pin CMOS integrated circuit that provides the channel filtering and equalization functions required for Bell 212A and CCITT V.22 modem applications. Employing switched capacitor filter techniques, the 73M3522 includes channel separation filters optimized for 1200 and 2400 Hz operation, while maintaining the bandshape necessary to reject 550 and 1800 Hz guard tones typical for V.22 standard modems. Fixed compromise equalization and group delay correction is distributed between the two channels as prescribed by V.22 recommendations. Dual multiplexers provide channel steering action for answer/originate control using a single pin.

The 73M3522 is designed to provide the front end for a Bell 212A or V.22 modem design. Optimized for PSTN lines, the 73M3522 offers an economical solution to the filter requirements of medium speed modem designs.

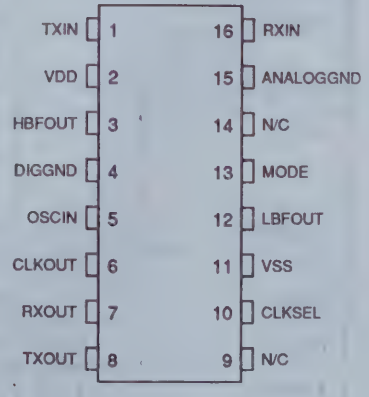
FEATURES

- Performs Bell 212A/V.22 channel filter functions
- High performance/low cost filter for medium speed modems
- Compromise equalization
- Single pin originate/answer steering logic
- Selectable clock divider-2.304 MHz or 3.5795 MHz color burst frequency
- ± 5V operation at 50 mW typical power consumption
- CMOS technology and I/O compatibility
- 16 pin DIP configuration
- CMOS latch-up protected

BLOCK DIAGRAM



PIN DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

SSI 73M3522
Bell 212A/V.22
Modem Filter

FUNCTIONAL DESCRIPTION

GENERAL

The SSI 73M3522 is designed to act as a low cost filter for use in Bell 212A or V.22 modem designs. The device consists of high and low band filters, split compromise equalizers for the two channels, and dual multiplexer logic for originate/answer channel steering. The unbuffered filter outputs are brought out to pins LBF and HBF before the signals have been processed by the equalizer section, and may be used for test purposes or in applications where the equalizer must be bypassed. Output impedance of these pins is 100 KΩ, requiring buffering if significant loads are to be driven. A clock generator provides the switched capacitor clock sampling frequency of 52.36 KHz from a 2.304 MHz buffered input signal. Tying pins 10 and 11 together changes the internal scaling rate to allow use of a 3.5795 MHz input, which can be generated from a standard color burst crystal. Filter response is essentially flat for a passband centered around the 1200 and 2300 Hz center frequencies, while notch filters located at 550 and 1800 Hz insure excellent rejection of CCITT guard tones.

DESIGN CONSIDERATIONS

The SSI 73M3522 uses SCF sampled data techniques. To avoid signal aliasing problems the input signal should not contain significant energy within 3 KHz of any multiple of the 52.36 KHz sampling clock. An anti-aliasing filter may be needed to meet this requirement.

When the alternate clock input is selected, a rate multiplier is inserted in the normal clock divider circuit. This shifts the SCF clock frequency to 52.30 KHz and the CLKOUT pin output to 104.6 KHz. In addition, a low level modulation tone at approximately 23 KHz will be generated with a typical amplitude of less than 600 µV RMS. Normal applications will not be affected by these changes.

PIN DESCRIPTIONS

NAME	I/O	DESCRIPTION
ANALOGGND	I	Analog ground pin - separate from digital ground.
CLKOUT	O	104.5 KHz SCF clock output, CMOS compatible.
DIGGND	I	Digital ground pin - separate from analog ground.
HBFOUT	O	High band filter output before equalization. Limited to 100 KΩ drive capability.
LBFOUT	O	Low band filter output before equalizer. Limited to 100 KΩ drive capability.
MODE	I	Channel steering control. Logic 1 selects the answer mode, with high-band transmit and low-band receive signal routing. A logic 0 selects the originate mode with the opposite channel orientation.
OSCIN	I	Accepts a CMOS level frequency reference at 2.304 or 3.5795 MHz as selected to generate the SCF 52.36 KHz clock used internally.
RXIN	I	Receive signal filter input.
RXOUT	O	Receive signal output from equalizer.
TXIN	I	Transmit signal filter input.
TXOUT	O	Transmit signal output from equalizer.

PIN DESCRIPTIONS (Continued)

NAME	I/O	DESCRIPTION
VDD	I	+5V -5%, +25% power input.
VSS	I	-5V +5%, -25% power input.
CLKSEL	I	Clock select pin. Connecting pins 10 and 11 changes the internal divider ratio to allow use of a standard 3.5795 MHz color burst crystal reference to generate the 52.36 KHz SCF clock. The 2.304 MHz clock input is selected when pin 10 is left open (has internal pull-up).

ELECTRICAL SPECIFICATIONS

DIGITAL SIGNALS (pins 5,6,10,13)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
VIH	High level input voltage		3.75			V
IIH	High level input current				10	µA
VIL	Low level input voltage				0.8	V
IIL	Low level input current				-10	µA

CLOCK INPUT (pin 5)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
	Input clock frequency	See note				
	Input clock duty cycle		20		80	%

Note: 2.304 MHz or 3.5795 MHz ±0.01%

ANALOG SIGNALS (pins 1,2,3,4,7,8,11,12,15,16)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
VDD	Supply voltage		4.75		6.25	V
VSS	Supply voltage		-4.75		-6.25	V
IDD	Supply current	VDD = 5.0V			10	mA
ISS	Supply current	VSS = -5.0V			-10	mA

ANALOG SIGNALS (Continued)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
Zin	Input impedance		10			KΩ
Zout	Output impedance	pins 3, 12		100		KΩ
Zout	Output impedance	pins 7, 8			1	KΩ
	Output noise	C-message			950	µV RMS
	Channel separation		50			dB
	Input signal level				VDD -2.0	V P-P
	Supply imbalance	VDD + VSS			0.5	V
	Operating temperature range		0		70	°C
	Storage temperature range		-55		125	°C

TYPICAL PERFORMANCE

(TA = 25°C, VDD = 5.0V, VSS = -5.0V)

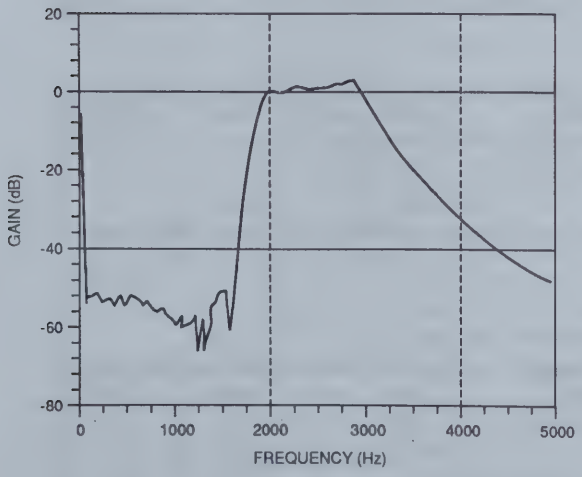


FIGURE 1: High Band Amplitude Response (dB)

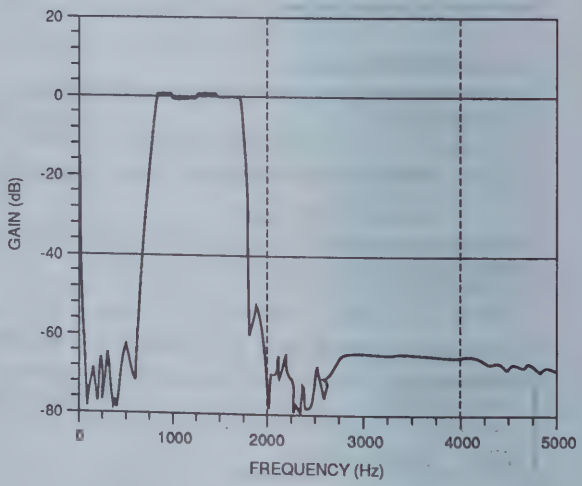


FIGURE 2: Low Band Amplitude Response (dB)

TYPICAL FREQUENCY RESPONSE

(TA = 25°C, VDD = 5.0V, VSS = -5.0V)

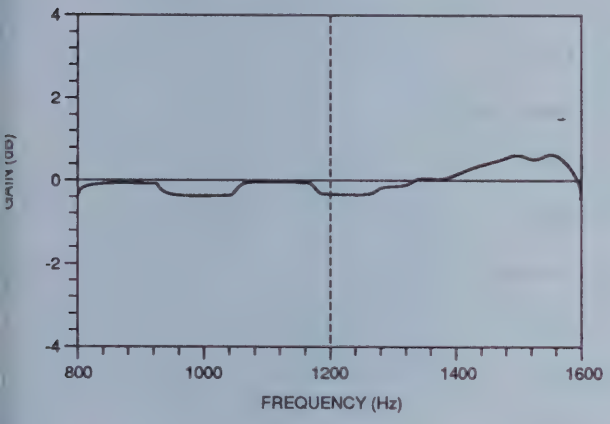


FIGURE 3: Low Band Amplitude Response (dB)

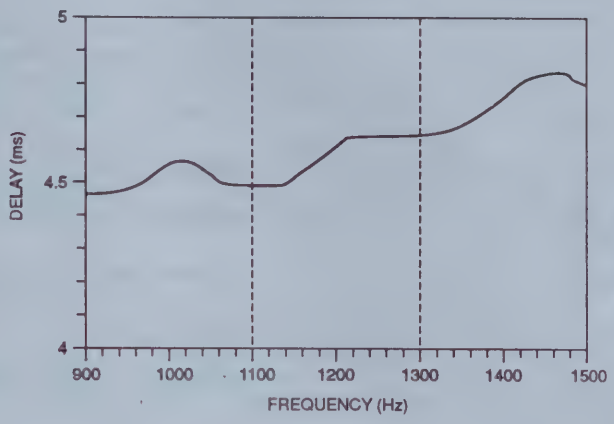


FIGURE 4: Low Band Group Delay (ms)

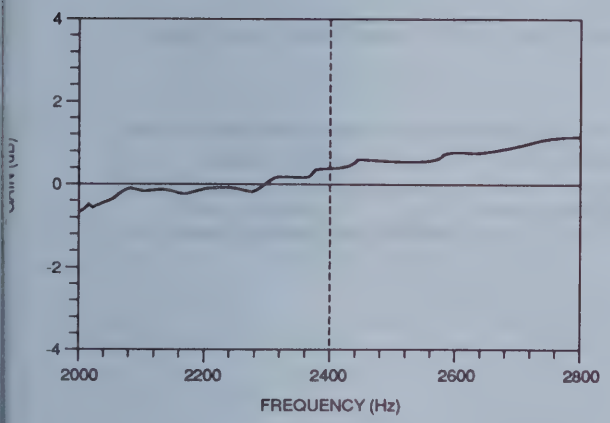


FIGURE 5: High Band Amplitude Response (dB)

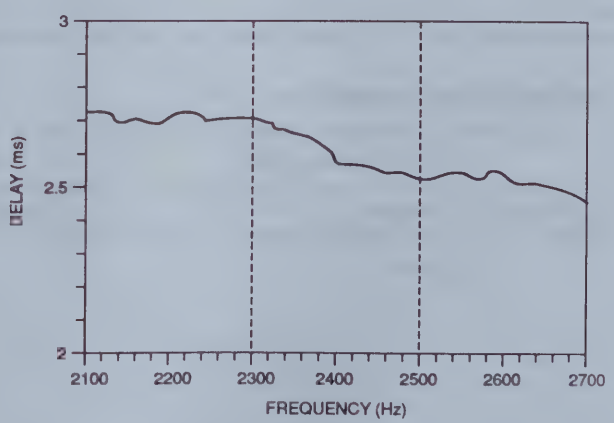
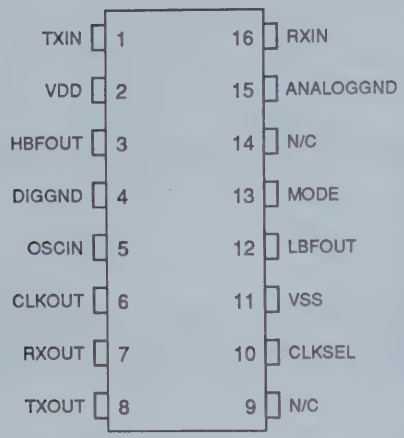


FIGURE 6: High Band Group Delay (ms)

SSI 73M3522
Bell 212A/V.22
Modem Filter

PACKAGE PIN DESIGNATIONS
(TOP VIEW)



16-pin DIP

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 73M3522 16-pin DIP	SSI 73M3522-CP	73M3522-CP

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Section 4

TONE SIGNALLING PRODUCTS

TELEPHONY INTEGRATED CIRCUITS SELECTOR GUIDE

TELEPHONY IC SELECTION CHART

APPLICATIONS	PRODUCTS	CENTRAL OFFICE		CUSTOMER PREMISES		PRODUCT DESCRIPTION
MARKETS SERVED	SSI DEVICE NUMBER	SUBSCRIBER NETWORK	C.O. INTERCONNECT EQUIPMENT	PUBLIC NETWORK	PRIVATE NETWORK	
T1/ISDN PRIMARY RATE APPLICATIONS • Channel Banks • Digital Cross-connects • Channel Service Units	78P233					T1/Primary Rate Line Interface
CEPT/ISDN PRIMARY RATE APPLICATIONS • PBX's • Multiplexers	78P234					CEPT/ Primary Rate Line Interface
ANALOG TONE SIGNALING APPLICATIONS • Central Office Switches • PBX's • Auto-Dialers • Test Equipment	75T201					12V DTMF Receiver
	75T202					5V DTMF Receiver
	75T203					DTMF Receiver with Early Detect
	75T981 & 2					Precise Call Progress Detect
• Toll Call Signaling	78A207					MFR1 Receiver
• Maintenance Terminating Units	78A400					2713 Hz Detect, 4-Wire Loopback
•Leased Line Diagnostics	78A420					Loopback with Gain Block
CONSUMER APPLICATIONS • Telephone Answering Machines • Pay Telephones • Modems • Security Systems	75T204					Low-Cost DTMFReceiver
	75T957					DTMF Rcvr. with Dial Tone Reject
	75T2089					DTMF Transceiver
	75T2090					DTMF Xcvr. with Call Progress
	75T2091					DTMF Xcvr. w/CPD Early Detect
• Business Phone Systems • Analog Matrix Switching	75T980					Call Progress Detect
	78A093					12 x 8 Analog Crosspoint Switch

SSI 75T201
Integrated DTMF Receiver

May, 1989

DESCRIPTION

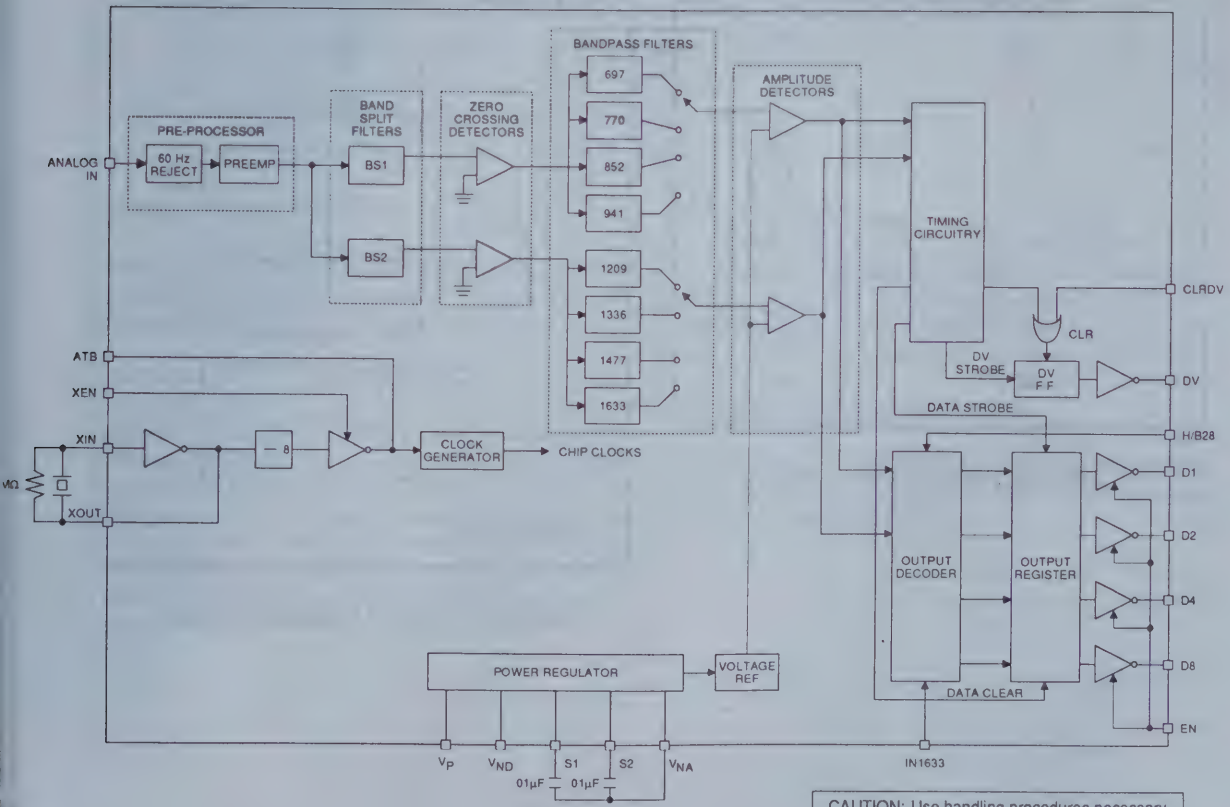
The SSI 75T201 is a complete Dual-Tone Multifrequency (DTMF) receiver detecting a selectable group of 12 or 16 standard digits. No front-end prefiltering is needed. The only external components required are an inexpensive 3.58MHz television "colorburst" crystal (for frequency reference) and two low-tolerance bypass capacitors. Extremely high system density is made possible by using the clock output of a crystal connected SSI 75T201 receiver to drive the time bases of additional receivers. The SSI 75T201 is a monolithic integrated circuit fabricated with low-power, complementary symmetry MOS (CMOS) processing. It requires only a single low tolerance voltage supply and is packaged in a standard 22-pin DIP. (Continued)

FEATURES

- Central office quality
- NO front-end band-splitting filters required
- Single, low-tolerance, 12-volt supply
- Detects either 12 or 16 standard DTMF digits
- Uses inexpensive 3.579545MHz crystal for reference
- Excellent speech immunity
- Output in either 4-bit hexadecimal code or binary coded 2-of-8
- 22-pin DIP package for high system density
- Synchronous or handshake interface
- Three-state outputs

4

BLOCK DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

DESCRIPTION (Continued)

The SSI 75T201 employs state-of-the-art circuit technology to combine digital and analog functions on the same CMOS chip using a standard digital semicondutor process. The analog input is preprocessed by 60Hz reject and band splitting filters and then hard-limited to provide AGC. Eight bandpass filters detect the individual tones. The digital post-processor times the tone durations and provides the correctly coded digital outputs. Outputs interface directly to standard CMOS circuitry, and are three-state enabled to facilitate bus-oriented architectures.

ANALOG IN

This pin accepts the analog input. It is internally biased so that the input signal may be AC coupled. The input may be DC coupled as long as it does not exceed the positive supply. Proper input coupling is illustrated in Figure 1.

CRYSTAL OSCILLATOR

The SSI 75T201 contains an onboard inverter with sufficient gain to provide oscillation when connected to a low-cost television "colorburst" crystal. The crystal oscillator is enabled by tying XEN high. The crystal is connected between XIN and XOUT. A 1MΩ 10% resistor is also connected between these pins. In this mode, ATB is a clock frequency output. Other SSI 75T201's may use the same frequency reference by tying their ATB pins to the ATB of a crystal connected device. XIN and XEN of the auxiliary devices must then be tied high and low respectively. Twenty-five devices may run off a single crystal-connected SSI 75T201 as shown in Figure 2.

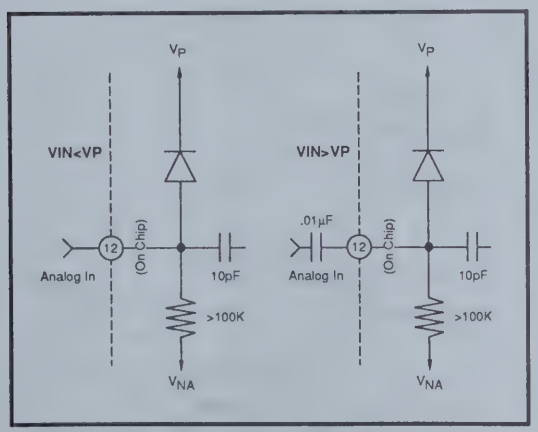


FIGURE 1: INPUT COUPLING

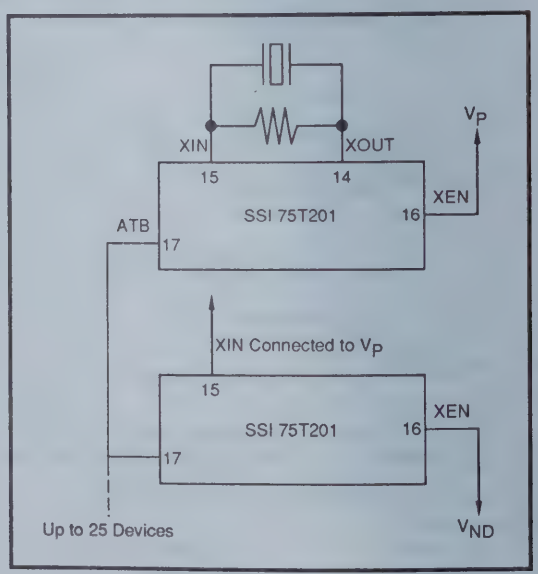


FIGURE 2: CRYSTAL CONNECTIONS

H/B28

This pin selects the format of the digital output code. When H/B28 is tied high, the output is hexadecimal. When tied low, the output is binary coded 2-of-8. The table below describes the two output codes.

Hexadecimal					Binary Coded 2-of-8				
Digit	D8	D4	D2	D1	Digit	D8	D4	D2	D1
1	0	0	0	1	1	0	0	0	0
2	0	0	1	0	2	0	0	0	1
3	0	0	1	1	3	0	0	1	0
4	0	1	0	0	4	0	1	0	0
5	0	1	0	1	5	0	1	0	1
6	0	1	1	0	6	0	1	1	0
7	0	1	1	1	7	1	0	0	0
8	1	0	0	0	8	1	0	0	1
9	1	0	0	1	9	1	0	1	0
0	1	0	1	0	0	1	1	0	1
*	1	0	1	1	*	1	1	0	0
#	1	1	0	0	#	1	1	1	0
A	1	1	0	1	A	0	0	1	1
B	1	1	1	0	B	0	1	1	1
C	1	1	1	1	C	1	0	1	1
D	0	0	0	0	D	1	1	1	1

TABLE 1: OUTPUT CODES

IN1633

When tied high, this pin inhibits detection of tone pairs containing the 1633Hz component. For detection of all 16 standard digits, IN1633 must be tied low.

OUTPUTS D1, D2, D4, D8 and EN

Outputs D1, D2, D4, and D8 are CMOS push-pull when enabled (EN high) and open circuited (high impedance) when disabled by pulling EN low. These digital outputs provide the code corresponding to the detected digit in the format programmed by the H/B28 pin. The digital outputs become valid after a tone pair has been detected and they are then cleared when a valid pause is timed.

DV and CLRDV

DV signals a detection by going high after a valid tone pair is sensed and decoded at the output pins D1, D2, D4, and D8. DV remains high until a valid pause occurs or the CLRDV is raised high, whichever comes first.

INTERNAL BYPASS PINS, S1, S2

In order for the SSI 75T201 DTMF Receiver to function properly, these pins must be bypassed to V_{NA} with 0.01µF ±20% capacitors.

POWER SUPPLY PINS, V_P, V_{NA}, V_{ND}

The analog (V_{NA}) and digital (V_{ND}) supplies are brought out separately to enhance analog noise immunity on the chip. V_{NA} and V_{ND} should be connected externally as shown in Figure 3.

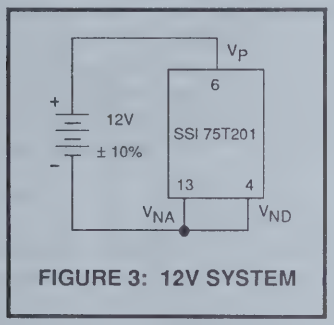


FIGURE 3: 12V SYSTEM

N/C PINS

These pins have no internal connection and may be left floating.

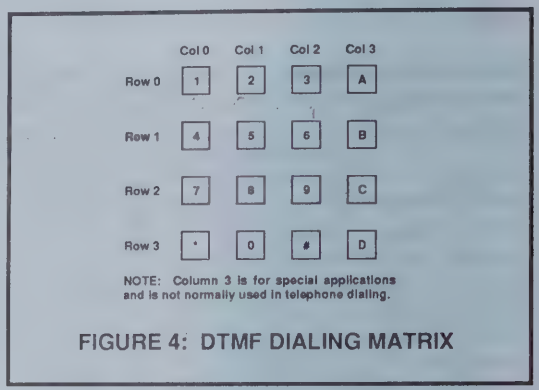


FIGURE 4: DTMF DIALING MATRIX

DETECTION FREQUENCY

Low Group f_0	High Group f_0
Row 0 = 697Hz	Column 0 = 1209Hz
Row 1 = 770Hz	Column 1 = 1336Hz
Row 2 = 852Hz	Column 2 = 1477Hz
Row 3 = 941Hz	Column 3 = 1633Hz

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Operation above absolute maximum ratings may damage the device. All SSI 75T201 unused inputs must be connected to V_P or V_{ND}, as appropriate.

PARAMETER	RATING	UNIT
DC Supply Voltage - V_P	Referenced to V_{NA}, V_{ND}	+16V
Operating Temperature		-40°C to +85°C Ambient
Storage Temperature		-65°C to +150°C
Power Dissipation (25°C)		1W
Input Voltage	All inputs except ANALOG IN	(V_P+ .5V) to (V_{ND} -.5V)
ANALOG IN Voltage		(V_P + .5V) to (V_P - 22V)
DC Current into any Input		±1.0mA
Lead Temperature	Soldering, 10 sec.	300°C

ELECTRICAL CHARACTERISTICS

($-40°C \le T_A \le +85°C$, $V_P - V_{ND} = V_P - V_{NA} = 12V \pm 10\%$)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Frequency Detect Bandwidth		± (1.5+2Hz)	±2.3	±3.0	% of fo
Amplitude for Detection	each tone	-24		+6	dBm ref. to 600Ω
Minimum Acceptable Twist	$\text{Twist} = \frac{\text{High Tone}}{\text{Low Tone}}$	-8		+4	dB
60Hz Tolerance				2	Vrms
Dial Tone Tolerance	"precise" dial tone			0dB	dB*
Talk Off	MITEL tape #CM 7290		2		hits
Digital Outputs	"0" level, 750µA load	V_{ND}		$V_{ND}+0.5$	V
(except XOUT)	"1" level, 750µA load	$V_P-0.5$		V_P	V
Digital Inputs	"0" level	V_{ND}		**	V
(except H/B28, XEN)	"1" level	***		V_P	V
Digital Inputs	"0" level	V_{ND}		$V_{ND}+1$	V
H/B28, XEN	"1" level	V_P-1		V_P	V
Power Supply Noise	wide band			25	mV p-p
Supply Current	TA = 25°C $V_P - V_{NA} = V_P - V_{ND} = 12V \pm 10\%$		29	50	mA
Noise Tolerance	MITEL tape #CM 7290			-12	dB*
Input Impedance	$V_P \ge V_{IN} \ge V_P - 22$	100KΩ||5pF			

* dB referenced to lowest amplitude tone
** $V_{ND} + .3(V_P - V_{ND})$
*** $V_P - .3(V_P - V_{ND})$

TIMING CHARACTERISTICS

($-40°C \le T_A \le +85°C$, $V_P - V_{ND} = V_P - V_{NA} = 12V \pm 10\%$)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_v	Tone Detection Time		20	25	40	ms
t_{slh}	Data Overlap of DV Rising Edge	CLRDV = V_{ND}, EN = V_P	7			µs
t_p	Pause Detection Time		25	32	40	ms
t_{dv}	Time between end of Tone and Fall of DV		40	45	50	ms

TIMING CHARACTERISTICS (Continued)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{shl}	Data overlap of DV Falling Edge		4	4.56	4.8	ms
t_{phl}	Prop. Delay: Rise of CLRDV to fall of DV	Cl = 300pF Measured at 50% points			1	µs
	Output Enable Time	Cl = 300pF, Rl = 10K Measured from 50% point of Rising Edge of EN to the 50% point of the data output with Rl to opposite rail.			1	µs
	Output Disable Time	Cl = 300pF, Rl = 1K , V = 1V Measured from 50% point of Falling Edge of EN to time at which output has changed 1V with Rl to opposite rail.			1	µs
	Output 10-90% Transition Time	Cl = 300pF			1	µs

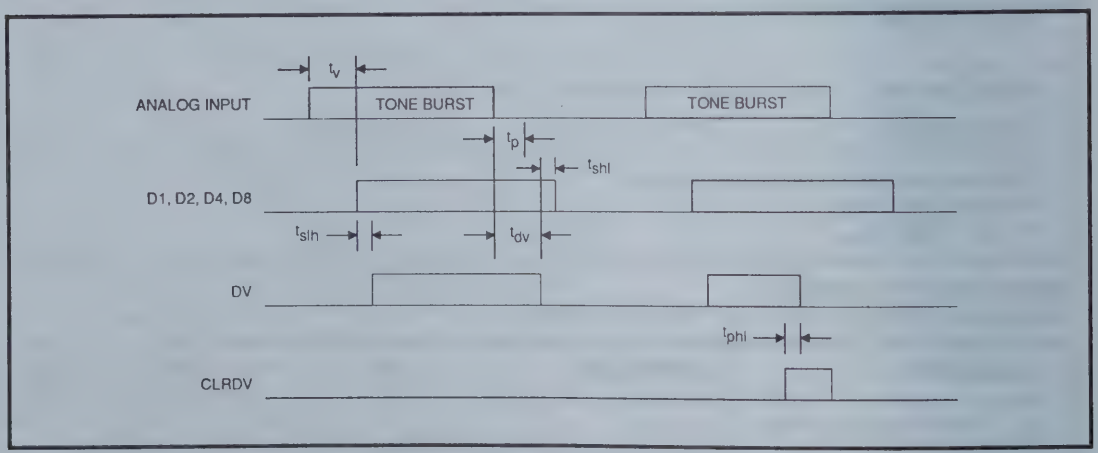


FIGURE 5: TIMING DIAGRAM

APPLICATION INFORMATION

TELEPHONE LINE INTERFACE

In applications that use the SSI 75T201 to decode DTMF signals from a phone line, a DAA (Direct Access Arrangement) must be implemented. Equipment intended for connection to the public telephone network must comply with and be registered in accordance with FCC Part 68. For PBX applications refer to EIA Standard RS-464.

Some of the basic guidelines are:

1) Maximum voltage and current ratings of the SSI 75T201 must not be exceeded; this calls for protection from ringing voltage, if applicable, which ranges from 80 to 120 volts RMS over a 20 to 80Hz frequency range.

2) The interface equipment must not breakdown with high-voltage transient tests (including a 2500 volt peak surge) as defined in the applicable document.

3) Phone line termination must be less than 200Ω DC and approximately 600Ω AC (200-3200Hz).

4) Termination must be capable of sustaining phone line loop current (off-hook condition) which is typically 18 to 120mA DC.

5) The phone line termination must be electrically balanced with respect to ground.

6) Public phone line termination equipment must be registered in accordance to FCC Part 68 or connected through registered protection circuitry. Registration typically takes about six months.

Figure 6 shows a simplified phone line interface using a 600Ω 1:1 line transformer. Transformers specially designed for phone line coupling are available from many transformer manufacturers.

Figure 7 shows a more featured version of Figure 6. These added options include:

1) A 150 volt surge protector to eliminate high voltage spikes.

2) A Texas Instruments TCM1520A ring detector, optically isolated from the supervisory circuitry.

3) Back-to-back Zener diodes to protect the DTMF (and optional multiplexer Op-Amp) from ringer voltage.

4) Audio multiplexer which allows voice or other audio to be placed on the line (a recorded message, for example) and not interfere with incoming DTMF tone detection.

An integrated voice circuit may also be implemented for line coupling, such as the Texas Instruments TCM1705A, however, this approach is typically more expensive than using a transformer as shown above.

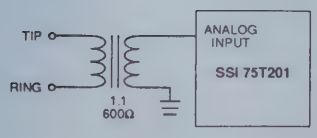


FIGURE 6: SIMPLIFIED INTERFACE

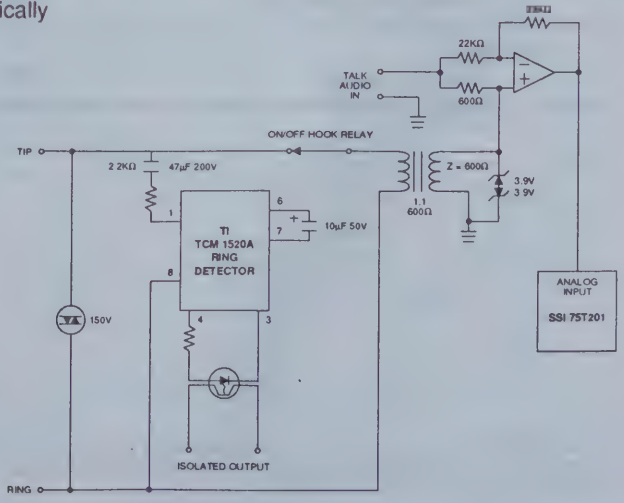
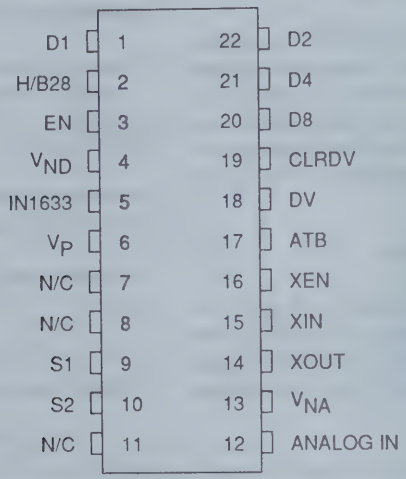


FIGURE 7: FULL FEATURED INTERFACE

SSI 75T201
Integrated
DTMF Receiver

PACKAGE PIN DESIGNATIONS
(TOP VIEW)



22-Pin DIP

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 75T201 22-Pin Plastic DIP	SSI 75T201 - IP	75T201 - IP

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SSI 75T202/203
5V Low-Power DTMF Receiver

May, 1988

DESCRIPTION

The SSI 75T202 and 75T203 are complete Dual-Tone Multifrequency (DTMF) receivers detecting a selectable group of 12 or 16 standard digits. No front-end pre-filtering is needed. The only externally required components are an inexpensive 3.58-MHz television "colorburst" crystal (for frequency reference) and a bias resistor. Extremely high system density is made possible by using the clock output of a crystal-connected SSI 75T202 or 75T203 receiver to drive the time bases of additional receivers. Both are monolithic integrated circuits fabricated with low-power, complementary symmetry MOS (CMOS) processing. They require only a single low tolerance voltage supply and are packaged in a standard 18-pin plastic DIP.

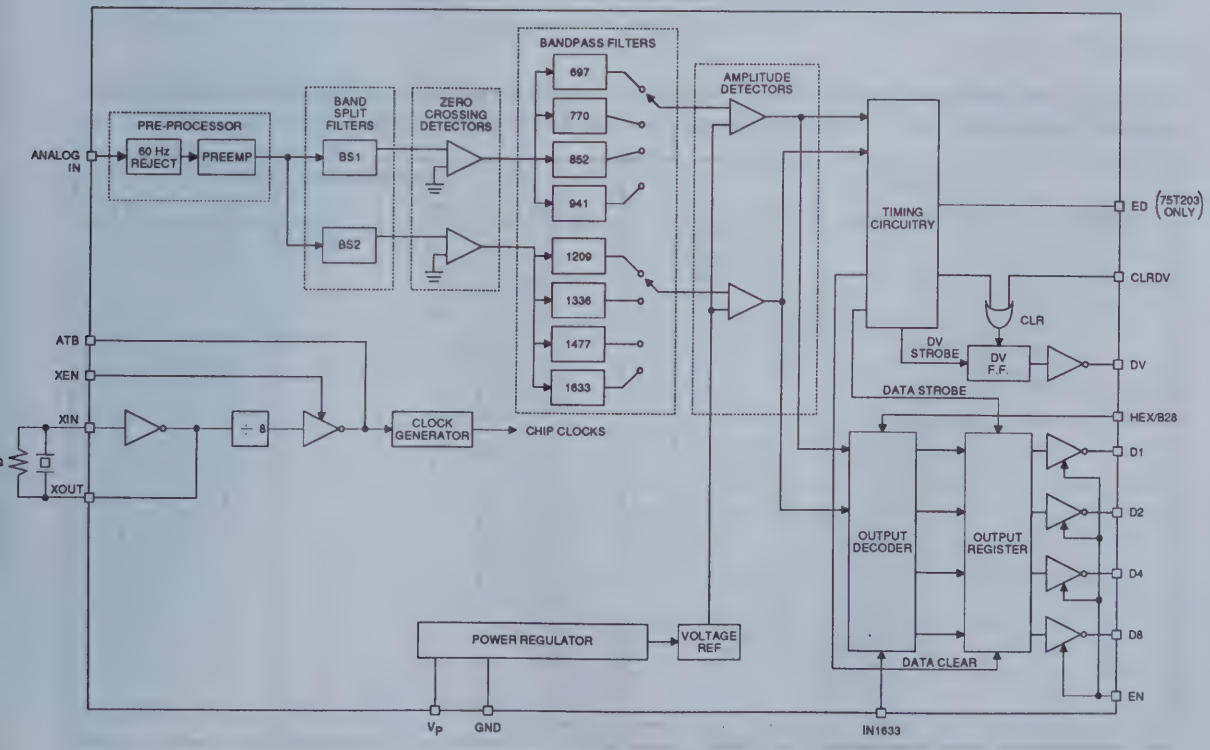
(Continued)

FEATURES

- Central office quality
- NO front-end band-splitting filters required
- Single, low-tolerance, 5-volt supply
- Detects either 12 or 16 standard DTMF digits
- Uses inexpensive 3.579545-MHz crystal for reference
- Excellent speech immunity
- Output in either 4-bit hexadecimal code or binary coded 2-of-8
- 18-pin DIP package for high system density
- Synchronous or handshake interface
- Three-state outputs
- Early detect output (SSI 75T203 only)

4

BLOCK DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

DESCRIPTION (Continued)

The SSI 75T202 and 75T203 employ state-of-the-art circuit technology to combine digital and analog functions on the same CMOS chip using a standard digital semicondutor process. The analog input is pre-processed by 60-Hz reject and band splitting filters and then hard-limited to provide AGC. Eight bandpass filters detect the individual tones. The digital post-processor times the tone durations and provides the correctly coded digital outputs. Outputs interface directly to standard CMOS circuitry, and are three-state enabled to facilitate bus-oriented architectures.

ANALOG IN

This pin accepts the analog input. It is internally biased so that the input signal may be AC coupled. The input may be DC coupled as long as it does not exceed the positive supply. Proper input coupling is illustrated in Figure 1.

The SSI 75T202 is designed to accept sinusoidal input wave forms but will operate satisfactorily with any input that has the correct fundamental frequency with harmonics less then -20 dB below the fundamental.

CRYSTAL OSCILLATOR

The SSI 75T202 and 75T203 contain an onboard inverter with sufficient gain to provide oscillation when connected to a low-cost television "colorburst" crystal. The crystal oscillator is enabled by tying XEN high. The crystal is connected between XIN and XOUT. A 1 MΩ 10% resistor is also connected between these pins. In this mode, ATB is a clock frequency output. Other SSI 75T202's (or 75T203's) may use the same frequency reference by tying their ATB pins to the ATB of a crystal connected device. XIN and XEN of the auxiliary devices must then be tied high and low respectively. Ten devices may run off a single crystal-connected SSI 75T202 or 75T203 as shown in Figure 2.

HEX/B28

This pin selects the format of the digital output code. When HEX/B28 is tied high, the output is hexadecimal. When tied low, the output is binary coded 2-of-8. The table below describes the two output codes.

Hexadecimal					Binary Coded 2-of-8				
Digit	D8	D4	D2	D1	Digit	D8	D4	D2	D1
1	0	0	0	1	1	0	0	0	0
2	0	0	1	0	2	0	0	0	1
3	0	0	1	1	3	0	0	1	0
4	0	1	0	0	4	0	1	0	0
5	0	1	0	1	5	0	1	0	1
6	0	1	1	0	6	0	1	1	0
7	0	1	1	1	7	1	0	0	0
8	1	0	0	0	8	1	0	0	1
9	1	0	0	1	9	1	0	1	0
0	1	0	1	0	0	1	1	0	1
*	1	0	1	1	*	1	1	0	0
#	1	1	0	0	#	1	1	1	0
A	1	1	0	1	A	0	0	1	1
B	1	1	1	0	B	0	1	1	1
C	1	1	1	1	C	1	0	1	1
D	0	0	0	0	D	1	1	1	1

TABLE 1: OUTPUT CODES

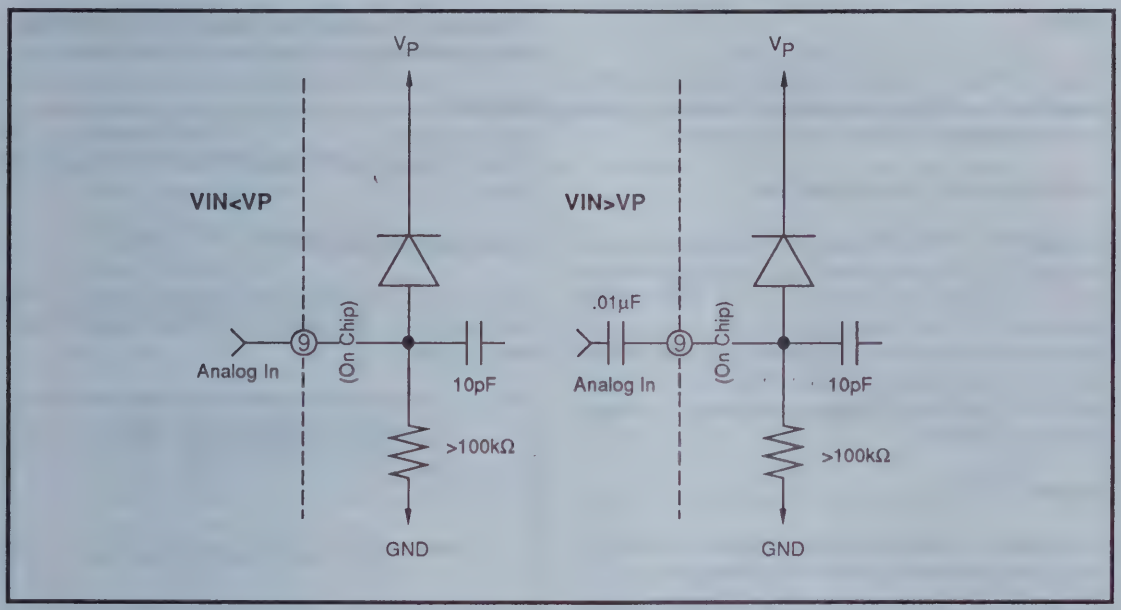


FIGURE 1: INPUT COUPLING

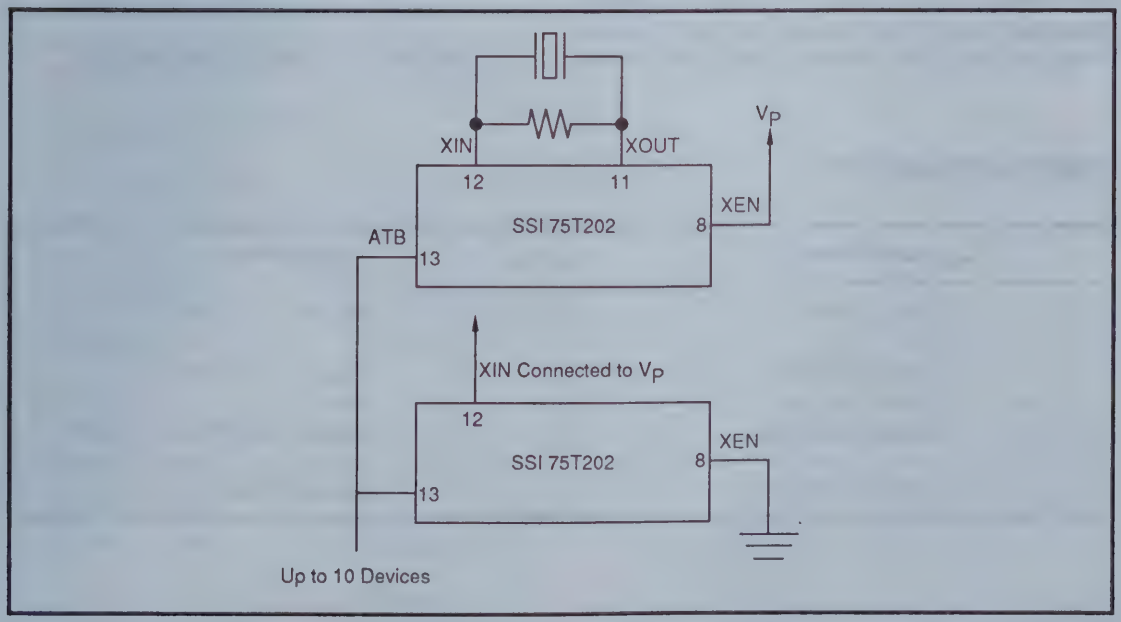


FIGURE 2: CRYSTAL CONNECTIONS

IN1633

When tied high, this pin inhibits detection of tone pairs containing the 1633Hz component. For detection of all 16 standard digits, IN1633 must be tied low.

OUTPUTS D1, D2, D4, D8 and EN

Outputs D1, D2, D4, D8 are CMOS push-pull when enabled (EN high) and open curcuited (high impedance) when disabled by pulling EN low. These digital outputs provide the code corresponding to the detected digit in the format programmed by the HEX/B28 pin. The digital outputs become valid after a tone pair has been detected and they are then cleared when a valid pause is timed.

DV and CLRDV

DV signals a detection by going high after a valid tone pair is sensed and decoded at the output pins D1, D2, D4, and D8. DV remains high until a valid pause occurs or the CLRDV is raised high, whichever is earlier.

ED (SSI 75T203 only)

The ED output goes high as soon as the SSI 75T203 begins to detect a DTMF tone pair and falls when the 75T203 begins to detect a pause. The D1, D2, D4, and D8 outputs are guaranteed to be valid when DV is high, but are not necessarily valid when ED is high.

N/C PINS

These pins have no internal connection and may be left floating.

DTMF DIALING MATRIX

See Figure 3. Please make note that column 3 is for special applications and is not normally used in telephone dialing.

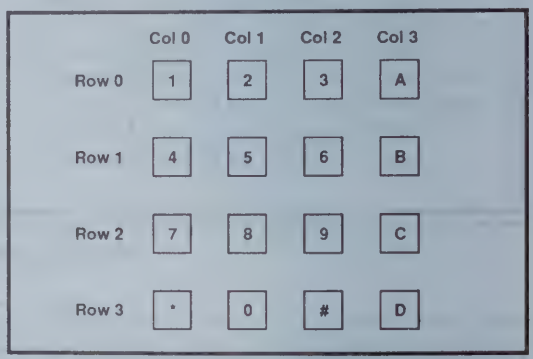


FIGURE 3: DTMF DIALING MATRIX

DETECTION FREQUENCY

Low Group f_0	High Group f_0
Row 0 = 697 Hz	Column 0 = 1209 Hz
Row 1 = 770 Hz	Column 1 = 1336 Hz
Row 2 = 852 Hz	Column 2 = 1477 Hz
Row 3 = 941 Hz	Column 3 = 1633 Hz

ABSOLUTE MAXIMUM RATINGS

(Operation above absolute maximum ratings may damage the device. All SSI 75T202/203 unused inputs must be connected to V_P or GND, as appropriate.)

PARAMETER	CONDITIONS	RATING
DC Supply Voltage - V_P		+7V
Operating Temperature		-40°C to +85°C Ambient
Storage Temperature		-65°C to +150°C
Power Dissipation (25°C)		65mW
Input Voltage	All inputs except ANALOG IN	(V_P + .5V) to -.5V
ANALOG IN Voltage		(V_P + .5V) to (V_P - 10V)
DC Current into any Input		±1.0mA
Lead Temperature	Soldering, 10 sec.	300°C

ELECTRICAL CHARACTERISTICS

(-40°C ≤ T_A ≤ +85°C, V_P = 5V ± 10%)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Frequency Detect Bandwidth		±(1.5+2Hz)	±2.3	±3.5	% of fo
Amplitude for Detection	each tone	-32		-2	dBm ref. to 600Ω
Minimum Acceptable Twist	$\text{Twist} = \frac{\text{High Tone}}{\text{Low Tone}}$	-10		+10	dB
60-Hz Tolerance				0.8	Vrms
Dial Tone Tolerance	"precise" dial tone			0dB	dB*
Talk Off	MITEL tape #CM 7290		2		hits
Digital Outputs	"0" level, 400µA load	0		0.5	V
(except XOUT)	"1" level, 200µA load	V_P-0.5		V_P	V
Digital Inputs	"0" level	0		0.3V_P	V
	"1" level	0.7V_P		V_P	V
Power Supply Noise	wide band			10	mV p-p
Supply Current	T_A = 25°C		10	16	mA
Noise Tolerance	MITEL tape #CM 7290			-12	dB*
Input Impedance	$V_P \geq V_{IN} \geq V_P$-10	100KΩ||15pF			

* dB referenced to lowest amplitude tone

SSI 75T202/203 TIMING

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
t_{ON}	Tone Time	for detection	40	-	-	ms
		for rejection	-	-	20	ms
t_{OFF}	Pause Time	for detection	40	-	-	ms
		for rejection	-	-	20	ms
t_D	Detect Time		25	-	46	ms
t_R	Release Time		35	-	50	ms
t_{SU}	Data Setup Time		7	-	-	µs
t_H	Data Hold Time		4.2	-	5.0	ms
t_{CL}	DV Clear Time		-	160	250	ns
t_{PW}	CLRDV Pulse Width		200	-	-	ns
t_{ED}	ED Detect Time		7	-	22	ms
t_{ER}	ED Release Time		2	-	18	ms
	Output Enable Time	C_L = 50pF, R_L = 1KΩ	-	-	200	ns
	Output Disable Time	C_L = 35pF, R_L = 500Ω	-	-	200	ns
	Output Rise Time	C_L = 50pF	-	-	200	ns
	Output Fall Time	C_L = 50pF	-	160	200	ns

SSI 75T202/203 TIMING (Continued)

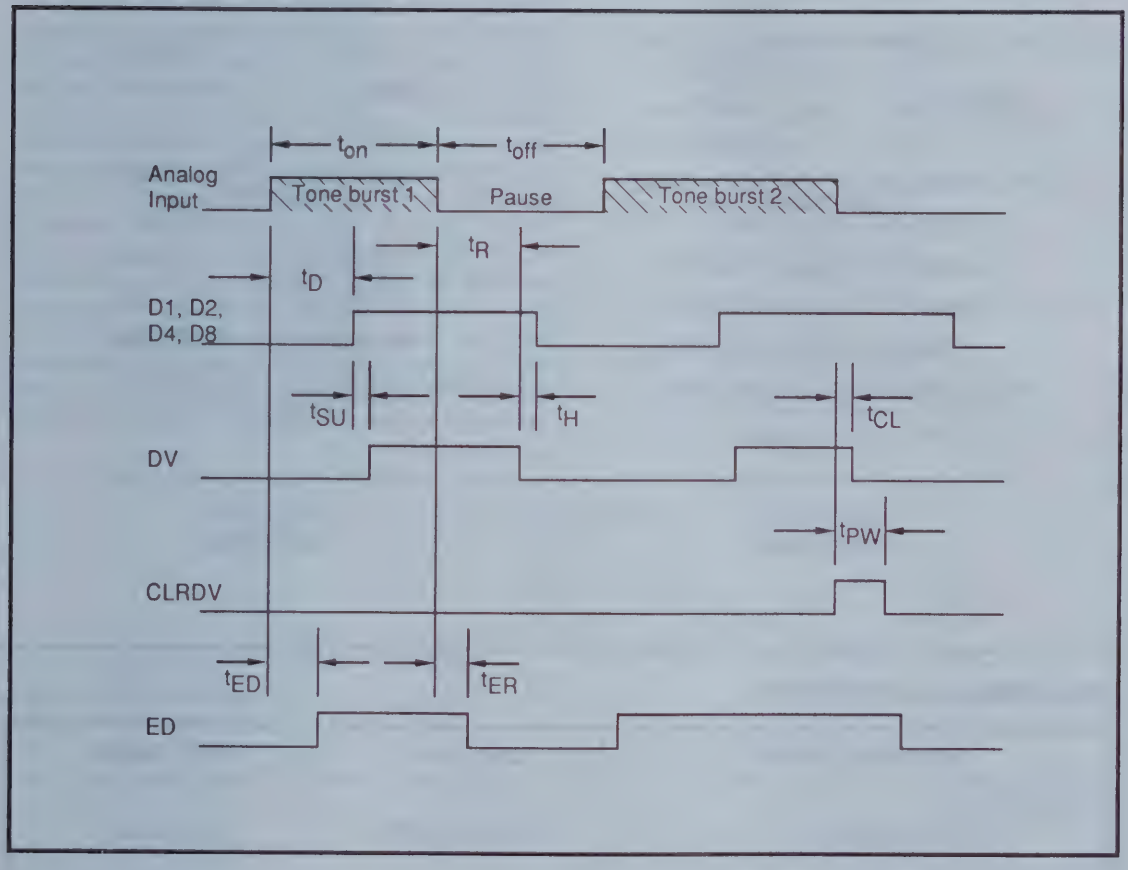
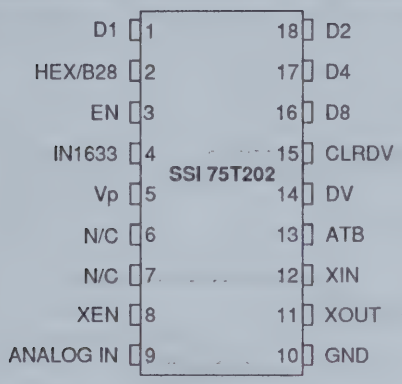


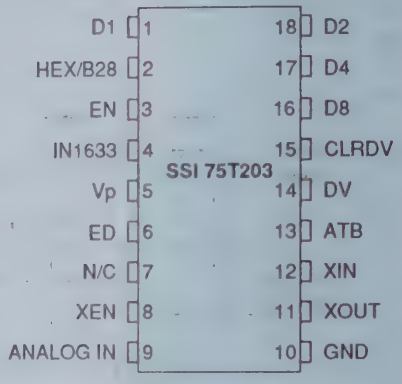
FIGURE 4: TIMING DIAGRAM

SSI 75T202/203
5V Low-Power
DTMF Receiver

PACKAGE PIN DESIGNATIONS
(TOP VIEW)



18 - Pin DIP
SSI 75T202



18 - Pin DIP
SSI 75T203

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 75T202 18-pin Plastic DIP	SSI 75T202-IP	75T202-IP
SSI 75T203 18-pin Plastic DIP	SSI 75T203-IP	75T203-IP

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SSI 75T204
5V Low-Power Subscriber DTMF Receiver

May, 1989

DESCRIPTION

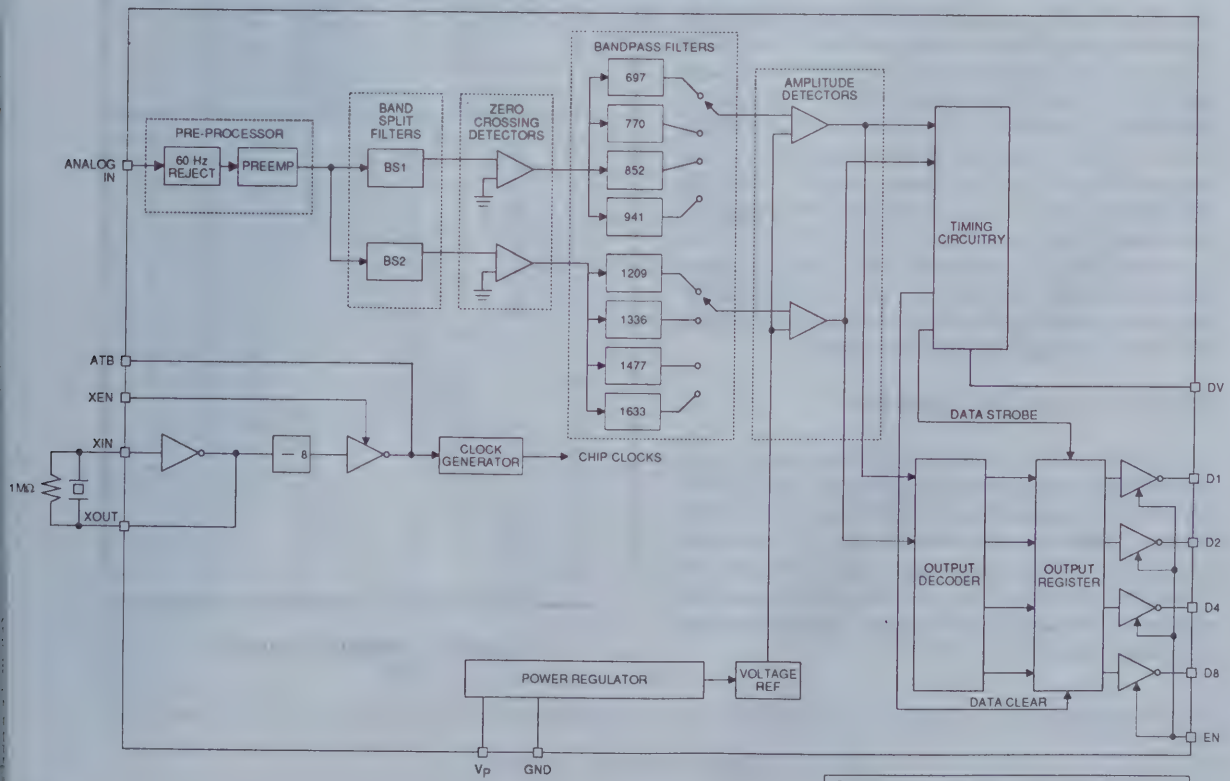
The SSI 75T204 is a complete Dual-Tone Multifrequency (DTMF) receiver that detects 16 standard digits. No front-end pre-filtering is needed. The only external components required are an inexpensive 3.58-MHz television "colorburst" crystal for frequency reference and a bias resistor. An Alternate Time Base (ATB) is provided to permit operation of up to 10 SSI 75T204's from a single crystal. The SSI 75T204 employs state-of-the-art "switched-capacitor" filter technology, resulting in approximately 40 poles of filtering, and digital circuitry on the same CMOS chip. The analog input signal is pre-processed by 60-Hz reject and band split filters and then zero-cross detected to provide AGC. Eight bandpass filters detect the individual tones. Digital processing is used to

(Continued)

FEATURES

- Intended for applications with less requirements than the SSI 75T202
- 14-pin plastic DIP or 16-pin SO package for high system density
- NO front-end band-splitting filters required
- Single low-tolerance 5-volt supply
- Detects all 16 standard DTMF digits.
- Uses an inexpensive 3.579545-MHz crystal
- Excellent speech immunity
- Output in 4-bit hexadecimal code
- Three-state outputs for microprocessor interface

BLOCK DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

DESCRIPTION (Continued)

measure the tone and pause durations and to provide output timing and decoding. The outputs interface directly to standard CMOS circuitry and are three-state enabled to facilitate bus-oriented architectures.

ANALOG IN

This pin accepts the analog input. It is internally biased so that the input signal may be AC coupled. The input may be DC coupled as long as it does not exceed the positive supply. Proper input coupling is illustrated in Figure 1.

The SSI 75T204 is designed to accept sinusoidal input wave forms but will operate satisfactorily with any input that has the correct fundamental frequency with harmonics less then -20 dB below the fundamental.

CRYSTAL OSCILLATOR

The SSI 75T204 contains an onboard inverter with sufficient gain to provide oscillation when connected to a low-cost television "colorburst" crystal. The crystal oscillator is enabled by tying XEN high. The crystal is connected between XIN and XOUT. A 1 MΩ 10% resistor is also connected between these pins. In this mode, ATB is a clock frequency output. Other SSI 75T204's (or 75T202's) may use the same frequency reference by tying their ATB pins to the ATB of a crystal connected device. XIN and XEN of the auxiliary devices must then be tied high and low respectively. Ten devices may run off a single crystal-connected SSI 75T204 (or 75T202) as shown in Figure 2.

OUTPUTS D1, D2, D4, D8 and EN

Outputs D1, D2, D4, D8 are CMOS push-pull when enabled (EN high) and open curcuited (high impedance) when disabled by pulling EN low. These digital outputs provide the hexadecimal code corresponding to the detected digit. The digital outputs become valid after a tone pair has been detected and they are then cleared when a valid pause is timed. The hexadecimal codes are described in Table 1.

DV

DV signals a detection by going high after a valid tone pair is sensed and decoded at the output pins D1, D2, D4, and D8. DV remains high until a valid pause occurs.

N/C PINS

These pins have no internal connection and may be left floating.

	Output Code			
Digit	D8	D4	D2	D1
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
0	1	0	1	0
*	1	0	1	1
#	1	1	0	0
A	1	1	0	1
B	1	1	1	0
C	1	1	1	1
D	0	0	0	0

TABLE 1: OUTPUT CODES

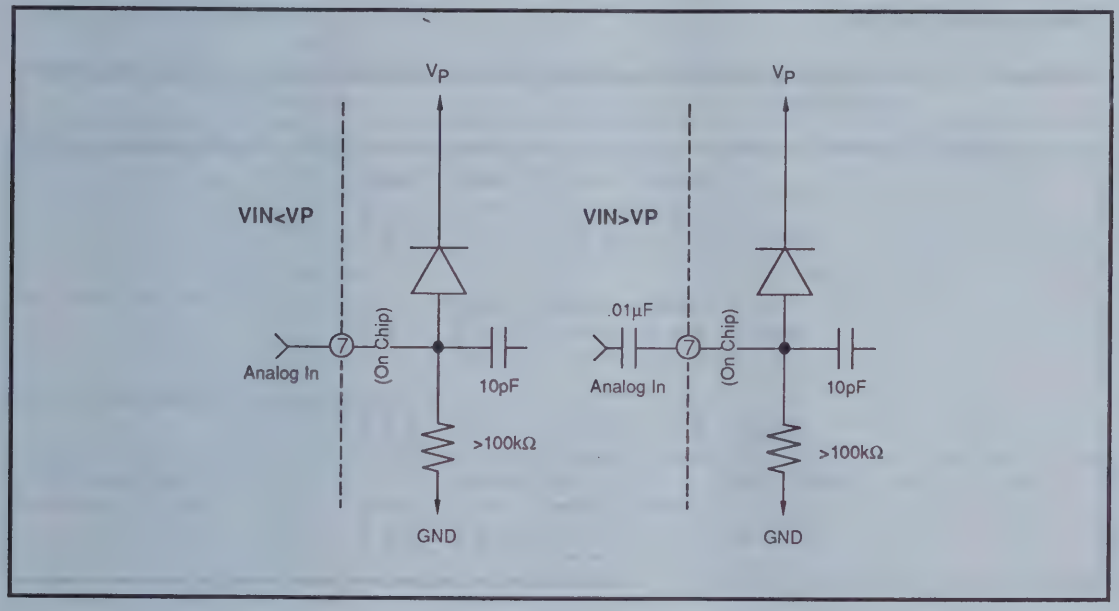


FIGURE 1: INPUT COUPLING

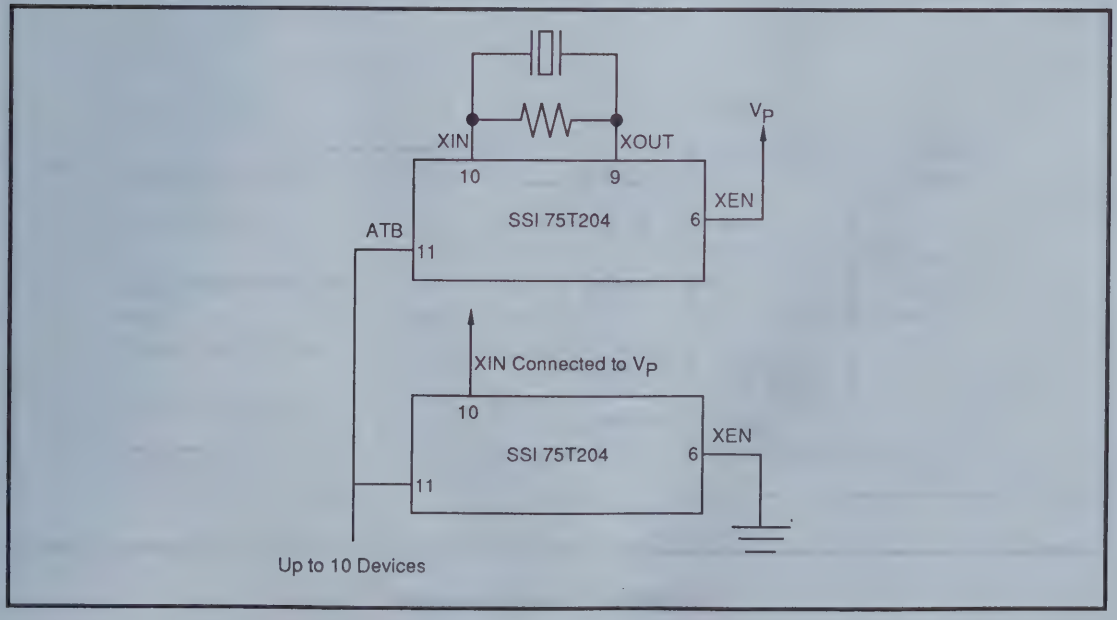


FIGURE 2: CRYSTAL CONNECTIONS

DTMF DIALING MATRIX

See Figure 3. Please note that column 3 is for special applications and is not normally used in telephone dialing.

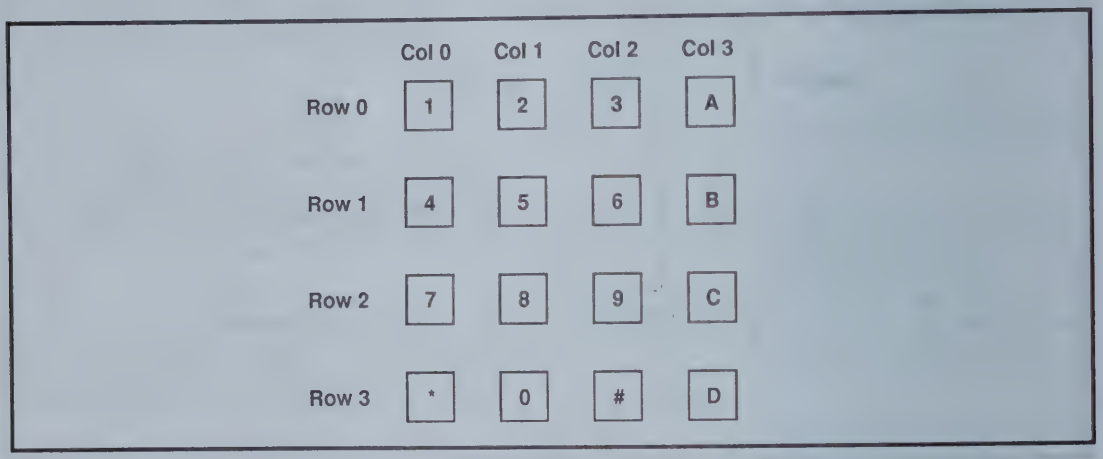


FIGURE 3: DTMF DIALING MATRIX

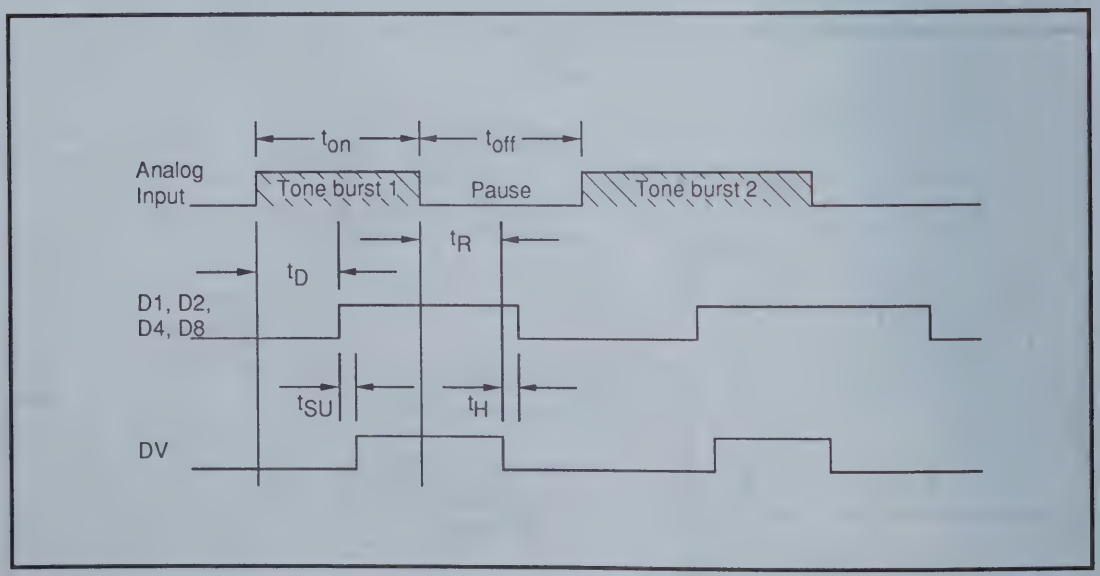


FIGURE 4: TIMING DIAGRAM

DETECTION FREQUENCY

Low Group f_0	High Group f_0
Row 0 = 697 Hz	Column 0 = 1209 Hz
Row 1 = 770 Hz	Column 1 = 1336 Hz
Row 2 = 852 Hz	Column 2 = 1477 Hz
Row 3 = 941 Hz	Column 3 = 1633 Hz

SSI 75T204 TIMING (Refer to Figure 4.)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
t_{ON}	Tone Time	for detection	40	-	-	ms
		for rejection	-	-	20	ms
t_{OFF}	Pause Time	for detection	40	-	-	ms
		for rejection	-	-	20	ms
t_D	Detect Time		25	-	46	ms
t_R	Release Time		35	-	50	ms
t_{SU}	Data Setup Time		7	-	-	µs
t_H	Data Hold Time		4.2	-	5.0	ms
	Output Enable Time	C_L = 50pF, R_L = 1KΩ	-	-	200	ns
	Output Disable Time	C_L = 35pF, R_L = 500Ω	-	-	200	ns
	Output Rise Time	C_L = 50pF	-	-	200	ns
	Output Fall Time	C_L = 50pF	-	-	200	ns

APPLICATION INFORMATION

The SSI 75T204 will tolerate total input RMS noise up to 12dB below the lowest amplitude tone. For most telephone applications, the combination of the high frequency attenuation of the telephone line and internal band-limiting make special circuitry at the input to the SSI 75T204 unnecessary. However, noise near the 56kHz internal sampling frequency will be aliased (folded back) into the audio spectrum, so if excessive noise is present above 28kHz, the simple RC filter shown in Figure 5 may be employed to band limit the incoming signal.

Noise will also be reduced by placing a grounded trace around the XIN and XOUT pins on the circuit board layout when using a crystal. It is important to note that XOUT is not intended to drive an additional device. XIN may be driven externally; in this case leave XOUT floating.

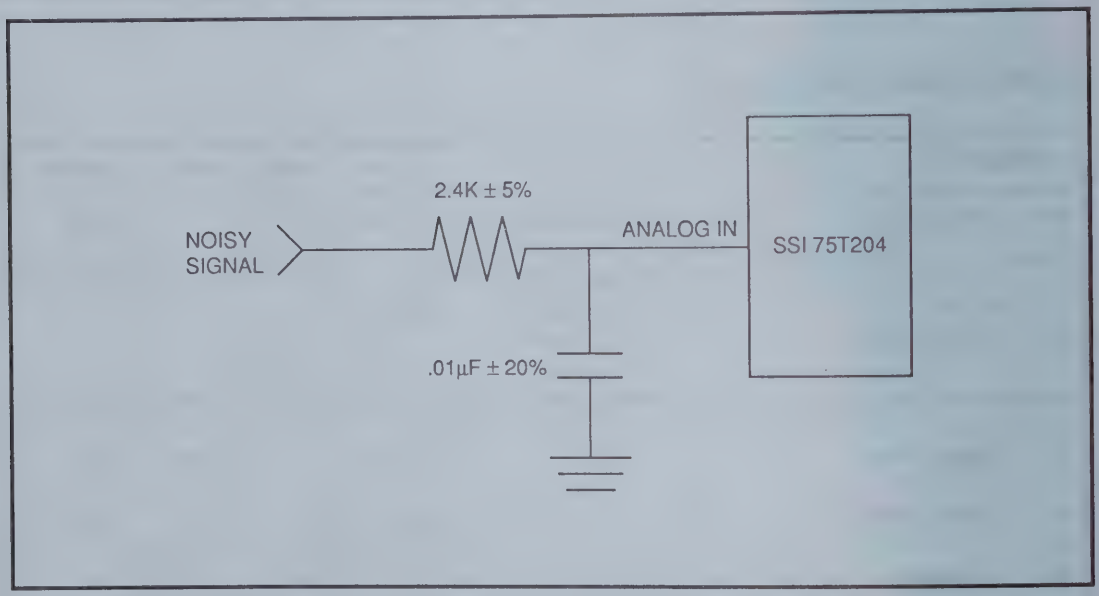


FIGURE 5: RC FILTER

ABSOLUTE MAXIMUM RATINGS

(Operation above absolute maximum ratings may damage the device. All SSI 75T204 unused inputs must be connected to V_P or GND, as appropriate.)

PARAMETER	CONDITIONS	RATING
DC Supply Voltage - V_P		+7V
Operating Temperature		-40°C to +85°C Ambient
Storage Temperature		-65°C to +150°C
Power Dissipation (25°C)		65mW
Input Voltage	All inputs except ANALOG IN	(V_P + 0.5V) to -0.5V
ANALOG IN Voltage		(V_P + .5V) to (V_P - 10V)
DC Current into any Input		±1.0mA
Lead Temperature	Soldering, 10 sec.	300°C

ELECTRICAL CHARACTERISTICS

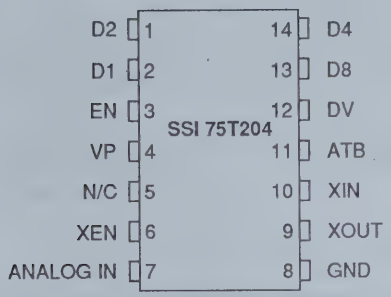
(-40°C ≤ T_A ≤ +85°C, V_P = 5V ± 10%)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Frequency Detect Bandwidth		±(1.5+2Hz)	±2.3	±3.5	% of fo
Amplitude for Detection	each tone	-32		-2	dBm ref. to 600Ω
Minimum Acceptable Twist	$\text{Twist} = \frac{\text{High Tone}}{\text{Low Tone}}$	-10		+10	dB
60-Hz Tolerance				0.8	Vrms
Dial Tone Tolerance	"precise" dial tone			0dB	dB*
Talk Off	MITEL tape #CM 7290		2		hits
Digital Outputs	"0" level, 400µA load	0		0.5	V
(except XOUT)	"1" level, 200µA load	V_P-0.5		V_P	V
Digital Inputs	"0" level	0		0.3V_P	V
	"1" level	0.7V_P		V_P	V
Power Supply Noise	wide band			10	mV p-p
Supply Current	T_A = 25°C		10	16	mA
Noise Tolerance	MITEL tape #CM 7290			-12	dB*
Input Impedance	$V_P \geq V_{IN} \geq V_P$-10	100KΩ||15pF			

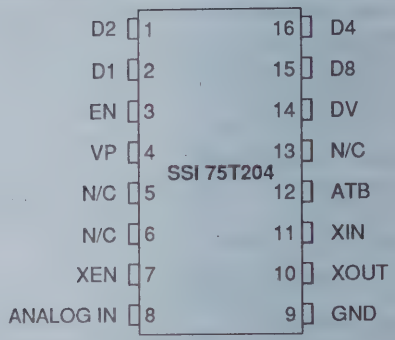
* dB referenced to lowest amplitude tone

SSI 75T204
5V Low-Power
Subscriber DTMF Receiver

PACKAGE PIN DESIGNATIONS
(TOP VIEW)



14 - Pin DIP



16 - Pin SOL

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 75T204 14-pin PDIP	SSI 75T204-IP	75T204-IP
SSI 75T204 16-pin SOL	SSI 75T204-IL	75T204-IL

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SSI 75T2089
DTMF Transceiver

May, 1989

DESCRIPTION

Silicon Systems' SSI 75T2089 is a complete Dual-Tone Multifrequency (DTMF) Transceiver that can both generate and detect all 16 DTMF tone pairs. The SSI 75T2089 circuit integrates the performance proven SSI 75T202 DTMF receiver with a new DTMF generator circuit.

The DTMF receiver electrical characteristics are identical to the standard SSI 75T202 device characteristics. The DTMF generator provides performance similar to the Mostek MK5380, but with an improved (tighter) output amplitude range specification and with the addition of independent latch and reset controls.

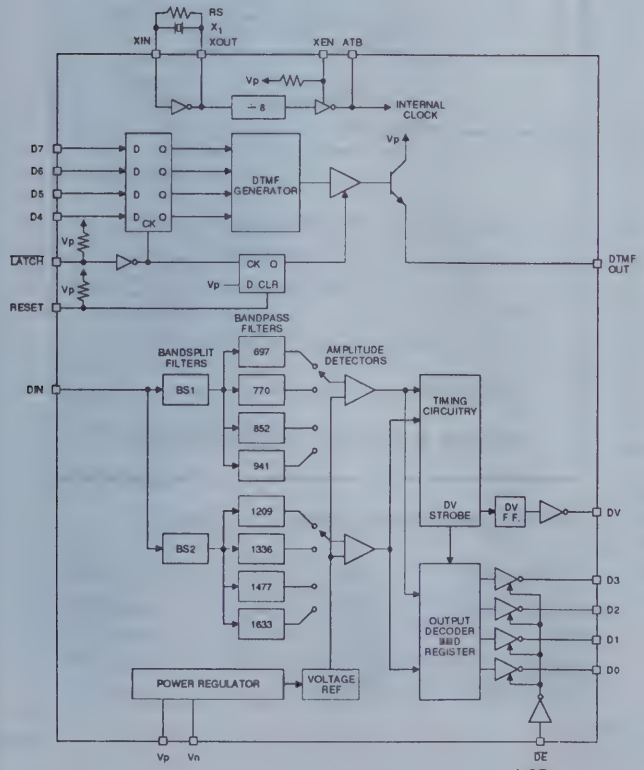
The only external components necessary for the SSI 75T2089 are a 3.58 MHz "colorburst" crystal with a parallel 1MΩ resistor. This provides the time base for digital functions and switched-capacitor filters in the device. No external filtering is required.

FEATURES

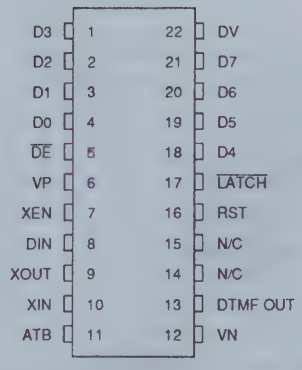
- DTMF Generator and Receiver on one-chip
- 22-pin, 400 mil plastic DIP
- Low-power 5 volt CMOS
- DTMF Receiver exhibits excellent speech immunity
- Three-state outputs (4-bit hexadecimal) from DTMF Receiver
- AC coupled, internally biased analog input
- Latched DTMF Generator inputs
- Analog input range from –32 to –2 dBm (ref 600 Ω)
- DTMF output typ. –8 dBm (Low Band) and –5.5 dBm (High Band)
- Uses inexpensive 3.579545 MHz crystal for reference
- Easy interface for microprocessor dialing

4

BLOCK DIAGRAM



PIN DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

CIRCUIT OPERATION

RECEIVER

The DTMF Receiver in the SSI 75T2089 detects the presence of a valid tone pair (indicating a single dialed digit) on a telephone line or other transmission medium. The analog input is pre-processed by 60 Hz reject and band-splitting filters, then hard-limited to provide Automatic Gain Control. Eight bandpass filters detect the individual tones. The digital post-processor times the tone durations and provides the correctly coded digital outputs. The outputs will drive standard CMOS circuitry, and are three-state enabled to facilitate bus-oriented architectures.

DIN

This pin accepts the analog input. It is internally biased so that the input signal may be AC coupled. The input may be DC coupled as long as it does not exceed the positive supply. Proper input coupling is illustrated in Figure 1.

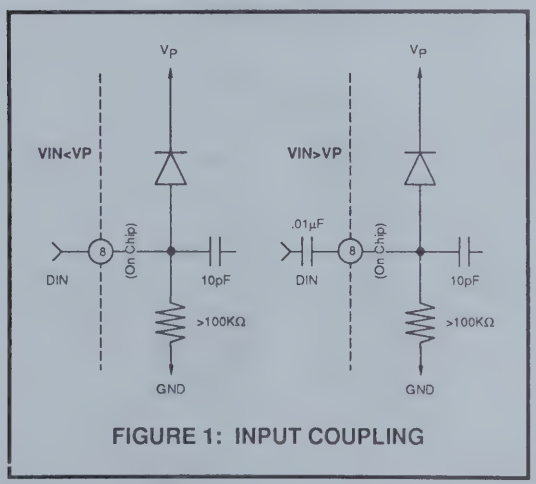


FIGURE 1: INPUT COUPLING

The SSI 75T2089 is designed to accept sinusoidal input waveforms but will operate satisfactorily with any input that has the correct fundamental frequency with harmonics greater than -20 dB below the fundamental.

CRYSTAL OSCILLATOR

The SSI 75T2089 contains an onboard inverter with sufficient gain to provide oscillation when connected to a low-cost television "color-burst" crystal. The crystal is placed between XIN and XOUT in parallel with a 1MΩ resistor, while XEN is tied high. Since the switched-capacitor-filter time base is derived from the crystal oscillator, the frequency accuracy of all portions of the SSI 75T2089 depends on the time base tolerance. The SSI DTMF Receiver frequency response and timing is specified for a time base accuracy of at least ±0.005%. ATB is a clock frequency output. Other devices may use the same frequency reference by tying their ATB pins to the ATB of a crystal connected device. XIN and XEN of the auxiliary devices must then be tied high and low respectively, XOUT is left floating. XOUT is designed to drive a resonant circuit only and is not intended to drive additional devices. Ten devices may run off a single crystal-connected SSI 75T2089 as shown in Figure 2.

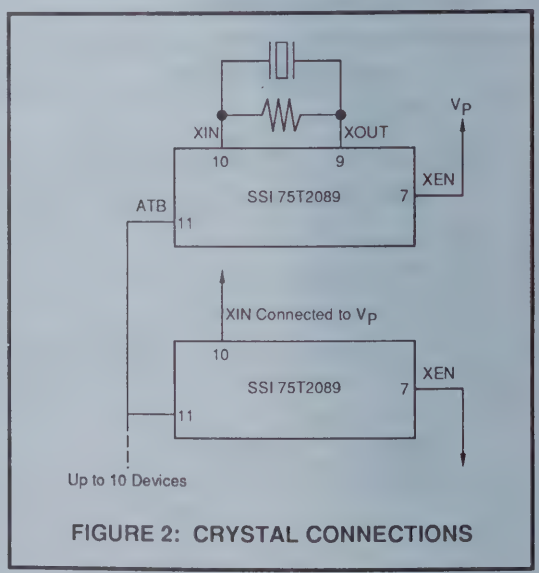


FIGURE 2: CRYSTAL CONNECTIONS

RECEIVER OUTPUTS AND THE $\overline{DE}$ PIN

Outputs D0, D1, D2, D3 are CMOS push-pull when enabled ($\overline{DE}$ low) and open-circuited (high impedance) when disabled ($\overline{DE}$ high). These digital outputs provide the hexadecimal code corresponding to the detected digit. Figure 3 shows that code.

The digital outputs become valid and DV signals a detection after a valid tone pair has been sensed. The outputs and DV are cleared when a valid pause has been timed.

Digit In / Out	Hexadecimal Code D7 / D3	D6 / D2	D5 / D1	D4 / D0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
0	1	0	1	0
*	1	0	1	1
#	1	1	0	0
A	1	1	0	1
B	1	1	1	0
C	1	1	1	1
D	0	0	0	0

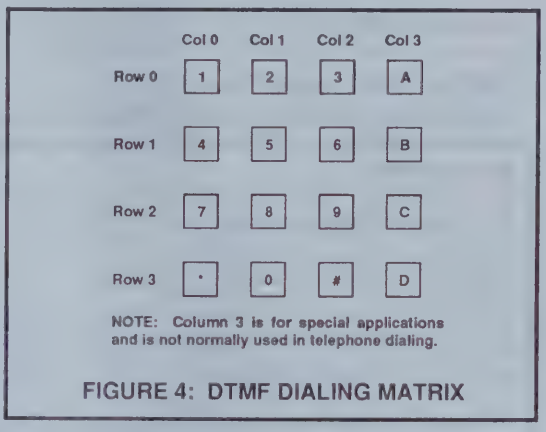
FIGURE 3

GENERATOR

The DTMF generator on the SSI 75T2089 responds to a hexadecimal code input with a valid tone pair. Pins D4-D7 are the data inputs for the generator. A high to low transition on $\overline{\text{LATCH}}$ causes the hexadecimal code to be latched internally and generation of the appropriate DTMF tone pair to begin. The DTMF output is disabled by a high on RESET and will not resume until new data is latched in.

DIGITAL INPUTS

The D4, D5, D6, D7, $\overline{\text{LATCH}}$, RESET inputs to the DTMF generator may be interfaced to open-collector TTL with a pull-up resistor or standard CMOS. These inputs follow the same hexadecimal code format as the DTMF receiver output. Figure 4 shows the code for each digit. The dialing matrix and detection frequency table below list the frequencies of the digits



NOTE: Column 3 is for special applications and is not normally used in telephone dialing.

FIGURE 4: DTMF DIALING MATRIX

DETECTION FREQUENCY

Low Group f_0	High Group f_0
Row 0 = 697Hz	Column 0 = 1209Hz
Row 1 = 770Hz	Column 1 = 1336Hz
Row 2 = 852Hz	Column 2 = 1477Hz
Row 3 = 941Hz	Column 3 = 1633Hz

DTMF OUT

The output amplitude characteristics listed in the specifications are given for a supply voltage of 5.0V. However, the output level is directly proportional to the supply, so variations in it will affect the DTMF output. A recommended line interface for this output is shown in Figure 5.

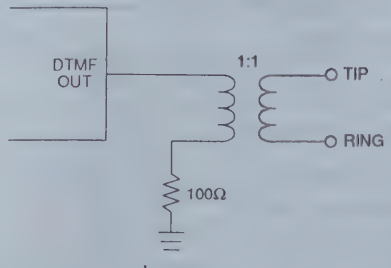


FIGURE 5: DTMF OUTPUT

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operating above absolute maximum ratings may damage the device.

PARAMETER	RATING	UNIT
DC Supply Voltage (Vp - Vn)	+7	V
Voltage at any Pin (Vn = 0)	-0.3 to Vp + 0.3	V
DIN Voltage	Vp + 0.5 to Vp - 10	V
Current through any Protection Device	±20	mA
Operating Temperature Range	-40 to + 85	°C
Storage Temperature	-65 to 150	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Supply Voltage		4.5		5.5	V
Power Supply Noise (wide band)				10	mV pp
Ambient Temperature		-40		+85	°C
Crystal Frequency (F Nominal = 3.579545MHz)		-0.01		+0.01	%
Crystal Shunt Resistor		0.8		1.2	MΩ
DTMF OUT Load Resistance		100			Ω

DIGITAL AND DC REQUIREMENTS

The following electrical specifications apply to the digital input and output signals over the recommended operating range unless otherwise noted. The specifications do not apply to the following pins: DIN, XIN, XOUT, and DTMF OUT. Positive current is defined as entering the circuit. Vn = 0 unless otherwise stated.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Supply Current*			15	30	mA
Power Dissipation				225	mW
Input Voltage High		0.7Vp			V
Input Voltage Low				0.3Vp	V
Input Current High				10	µA
Input Current Low		-10			µA
Output Voltage High	Ioh = -0.2mA	Vp-0.5			V
Output Voltage Low	Iol = +0.4mA			Vn+0.5	V

* with DTMF output disabled

DTMF RECEIVER: Electrical Characteristics

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Frequency Detect Bandwidth		±(1.5+2Hz)	±2.3	±3.5	%Fo
Amplitude for Detection		-32		-2	dBm
Twist Tolerance		-10		+10	dB
60Hz Tolerance				0.8	Vrms
Dial Tone Tolerance	Precise Dial Tone			0	dB*
Speech Immunity	MITEL Tape #CM7290		2		hits
Noise Tolerance	MITEL Tape #CM7290			-12	dB*
Input Impedance		100			KΩ
* Referenced to lowest amplitude tone					

DTMF RECEIVER: Timing Characteristics

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
TON	Tone Time for Detect		40			ms
TON	Tone Time for No Detect				20	ms
TOFF	Pause Time for Redetection		40			ms
TOFF	Pause Time for Bridging				20	ms
TD1	Detect Time		25		46	ms
TR1	Release Time		35		50	ms
TSU1	Data Set Up Time		7			µs
THD1	Data Hold Time		4.2		5.0	ms
	Output Enable Time				200	ns
	Output Disable Time				200	ns

DTMF GENERATOR: Electrical Characteristics

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Frequency Accuracy		-1.0		+1.0	%Fo
Output Amplitude	R1 = 100Ω to Vn, Vp - Vn = 5.0V				
Low Band		-9.2		-7.2	dBm
High Band		-6.6		-4.6	dBm
Output Distortion	DC to 50KHz			-20	dB

DTMF GENERATOR: Timing Characteristics

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
TSTART	Start-Up Time				2.5	µs
TSU2	Data Set-Up Time		100			ns
THD2	Data Hold Time		50			ns
TRP	RESET Pulse Width		100			ns
TPW	$\overline{\text{LATCH}}$ Pulse Width		100			ns

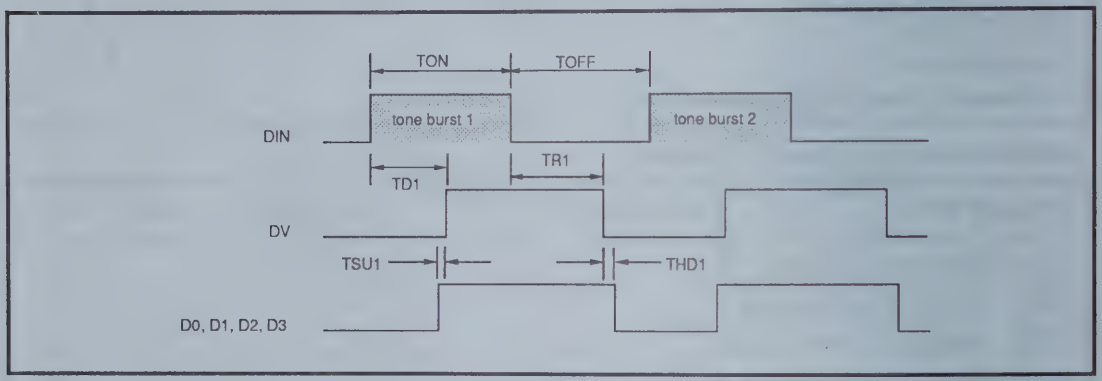


FIGURE 6: DTMF DECODER

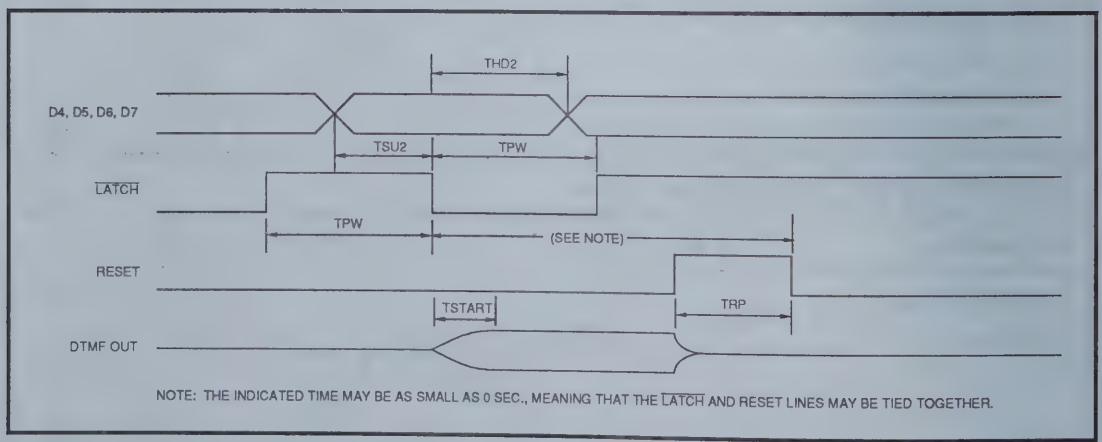
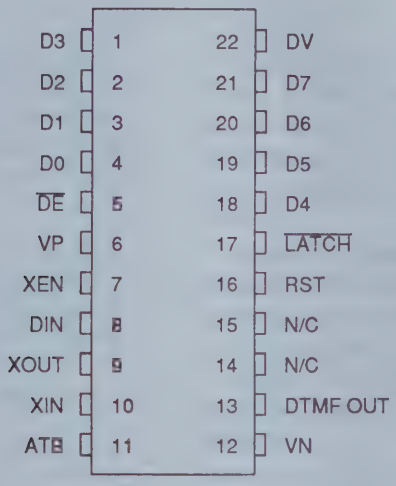


FIGURE 7: DTMF GENERATOR

PACKAGE PIN DESIGNATIONS

(TOP VIEW)



22-Pin DIP

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 75T2089 22-Pin Plastic DIP	SSI 75T2089 - IP	75T2089 - IP

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NOTES:

SSI 75T2090
DTMF Transceiver and Call Progress Detection

May, 1989

DESCRIPTION

Silicon Systems' SSI 75T2090 is a complete Dual-Tone Multifrequency (DTMF) Transceiver that can both generate and detect all 16 standard Touch-Tone digits. The SSI 75T2090 circuit integrates the performance proven SSI 75T202 DTMF Receiver with a new DTMF generator circuit.

The DTMF Receiver electrical characteristics are identical to the standard SSI 75T202 device characteristics. The DTMF generator provides performance similar to the Mostek MK5380, but with an improved (tighter) output amplitude range specification and with the addition of independent latch and reset controls.

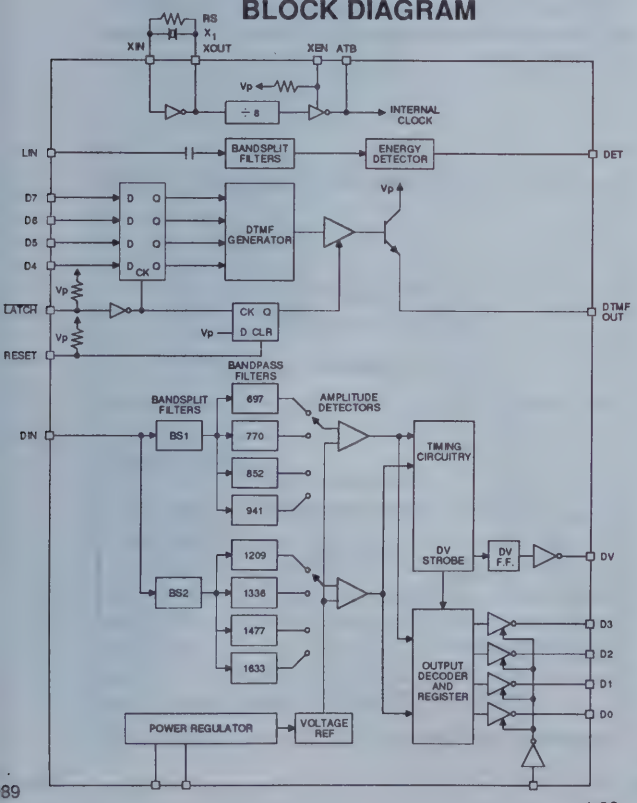
An additional features of the 75T2090 is "imprecise" call progress detector. The detector detects the presence of signals in the 305-640 Hz band. (Continued)

FEATURES

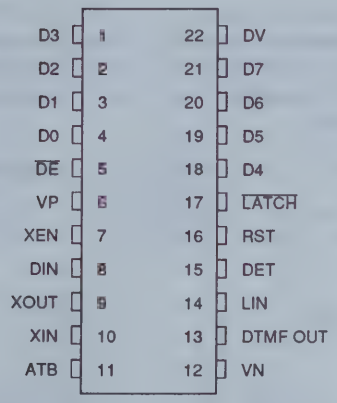
- DTMF Generator and Receiver on one-chip
- 22-pin, 400 mil plastic DIP
- Low-power 5 volt CMOS
- DTMF Receiver exhibits excellent speech immunity
- Three-state outputs (4-bit hexadecimal) from DTMF Receiver
- AC coupled, internally biased analog input
- Latched DTMF Generator inputs
- Analog input range from –32 to –2 dBm (ref 600Ω)
- DTMF output typ. –8 dBm (Low Band) and –5.5 dBm (High Band)
- Uses inexpensive 3.579545 MHz crystal for reference
- Easy interface for microprocessor dialing
- Call progress detection

4

BLOCK DIAGRAM



PIN DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

DESCRIPTION (Continued)

The only external components necessary for the SSI 75T2090 are a 3.58 MHz "colorburst" crystal with a parallel 1MΩ resistor. This provides the time base for digital functions and switched-capacitor filters in the device. No external filtering is required.

CIRCUIT OPERATION

RECEIVER

The DTMF Receiver in the SSI 75T2090 detects the presence of a valid tone pair (indicating a single dialed digit) on a telephone line or other transmission medium. The analog input is pre-processed by 60Hz reject and band-splitting filters, then hard-limited to provide Automatic Gain Control. Eight bandpass filters detect the individual tones. The digital post-processor times the tone durations and provides the correctly coded digital outputs. The outputs will drive standard CMOS circuitry, and are three-state enabled to facilitate bus-oriented architectures.

DIN

This pin accepts the analog input. It is internally biased so that the input signal may be AC coupled. The input may be DC coupled as long as it does not exceed the positive supply. Proper input coupling is illustrated in Figure 1.

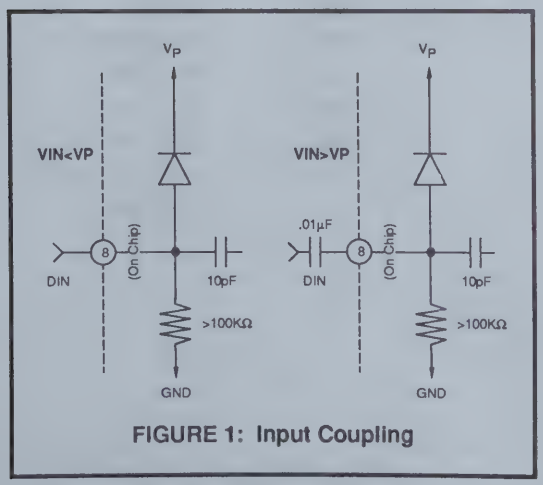


FIGURE 1: Input Coupling

The SSI 75T2090 is designed to accept sinusoidal input waveforms but will operate satisfactorily with any input that has the correct fundamental frequency with harmonics greater than -20 dB below the fundamental.

CRYSTAL OSCILLATOR

The SSI 75T2090 contains an onboard inverter with sufficient gain to provide oscillation when connected to a low-cost television "color-burst" crystal. The crystal is placed between XIN and XOUT in parallel with a 1MΩ resistor, while XEN is tied high. Since the switched-capacitor-filter time base is derived from the crystal oscillator, the frequency accuracy of all portions of the SSI 75T2090 depends on the time base tolerance. The SSI DTMF Receiver frequency response and timing is specified for a time base accuracy of at least ±0.005%. ATB is a clock frequency output. Other devices may use the same frequency reference by tying their ATB pins to the ATB of a crystal connected device. XIN and XEN of the auxiliary devices must then be tied high and low respectively, XOUT is left floating. XOUT is designed to drive a resonant circuit only and is not intended to drive additional devices. Ten devices may run off a single crystal-connected SSI 75T2090 as shown in Figure 2.

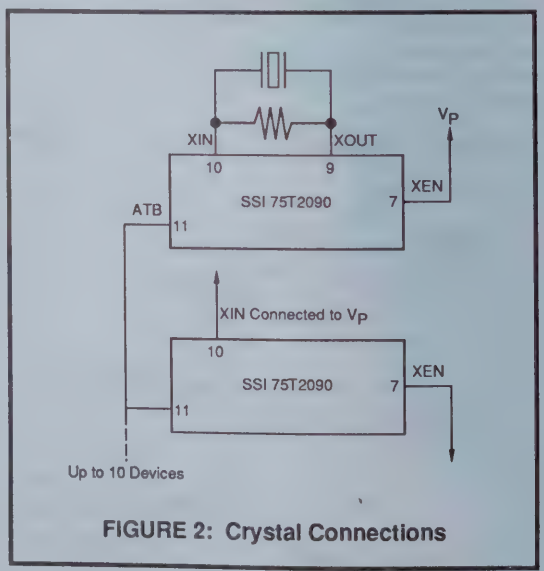


FIGURE 2: Crystal Connections

RECEIVER OUTPUTS AND THE $\overline{DE}$ PIN

Outputs D0, D1, D2, D3 are CMOS push-pull when enabled ($\overline{DE}$ low) and open-circuited (high impedance) when disabled ($\overline{DE}$ high). These digital outputs provide the hexadecimal code corresponding to the detected digit. Figure 3 shows that code.

The digital outputs become valid and DV signals a detection after a valid tone pair has been sensed. The outputs and DV are cleared when a valid pause has been timed.

	Hexadecimal Code			
Digit In / Out	D7 / D3	D6 / D2	D5 / D1	D4 / D0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
0	1	0	1	0
*	1	0	1	1
#	1	1	0	0
A	1	1	0	1
B	1	1	1	0
C	1	1	1	1
D	0	0	0	0

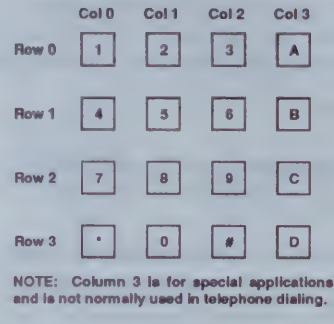
FIGURE 3

GENERATOR

The DTMF generator on the SSI 75T2090 responds to a hexadecimal code input with a valid tone pair. Pins D4-D7 are the data inputs for the generator. A high to low transition on $\overline{LATCH}$ causes the hexadecimal code to be latched internally and generation of the appropriate DTMF tone pair to begin. The DTMF output is disabled by a high on RESET and will not resume until new data is latched in.

DIGITAL INPUTS

The D4, D5, D6, D7, $\overline{LATCH}$, RESET inputs to the DTMF generator may be interfaced to open-collector TTL with a pull-up resistor or standard CMOS. These inputs follow the same hexadecimal code format as the DTMF receiver output. Figure 4 shows the code for each digit. The dialing matrix and detection frequency table below list the frequencies of the digits.



NOTE: Column 3 is for special applications and is not normally used in telephone dialing.

FIGURE 4: DTMF Dialing Matrix

DETECTION FREQUENCY

Low Group f_0	High Group f_0
Row 0 = 697Hz	Column 0 = 1209Hz
Row 1 = 770Hz	Column 1 = 1336Hz
Row 2 = 852Hz	Column 2 = 1477Hz
Row 3 = 941Hz	Column 3 = 1633Hz

DTMF OUT

The output amplitude characteristics listed in the specifications are given for a supply voltage of 5.0V. However, the output level is directly proportional to the supply, so variations in it will affect the DTMF output. A recommended line interface for this output is shown in Figure 5.

CALL PROGRESS DETECTION

The Call Progress Detector consists of a bandpass filter and an energy detector for turning the on/off cadences into a microprocessor compatible signal.

LIN INPUT

This analog input accepts the call progress signal and should be used in the same manner as the receiver input DIN.

DET OUTPUT

This output is TTL compatible and will be of a frequency corresponding to the various cadences of Call Progress signals such as, on 0.5 sec/off 0.5 sec for a busy tone, on 0.25 sec/off 0.25 sec for a reorder tone and on 0.8-1.2 sec/off 2.7-3.3 sec for an audible ring tone.

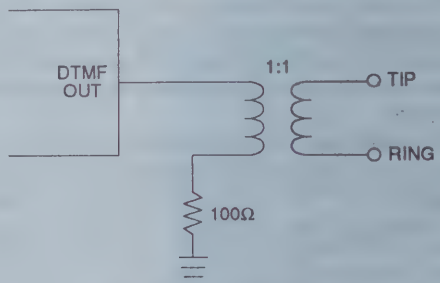


FIGURE 5: DTMF Output

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operating above absolute maximum ratings may damage the device.

PARAMETER	RATING	UNIT
DC Supply Voltage (Vp - Vn)	+7	V
Voltage at any Pin (Vn = 0)	-0.3 to Vp + 0.3	V
DIN Voltage	Vp + 0.5 to Vp - 10	V
Current through any Protection Device	±20	mA
Operating Temperature Range	-40 to + 85	°C
Storage Temperature	-65 to 150	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Supply Voltage		4.5		5.5	V
Power Supply Noise (wide band)				10	mV pp
Ambient Temperature		-40		+85	°C
Crystal Frequency (F Nominal = 3.579545MHz)		-0.01		+0.01	%
Crystal Shunt Resistor		0.8		1.2	MΩ
DTMF OUT Load Resistance		100			Ω

DIGITAL AND DC REQUIREMENTS

The following electrical specifications apply to the digital input and output signals over the recommended operating range unless otherwise noted. The specifications do not apply to the following pins: LIN, DIN, XIN, XOUT, and DTMF OUT. Positive current is defined as entering the circuit. Vn = 0 unless otherwise stated.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Supply Current*			15	30	mA
Power Dissipation				225	mW
Input Voltage High		0.7Vp			V
Input Voltage Low				0.3Vp	V
Input Current High				10	µA
Input Current Low		-10			µA
Output Voltage High	Ioh = -0.2mA	Vp-0.5			V
Output Voltage Low	Iol = +0.4mA			Vn+0.5	V
* with DTMF output disabled					

DTMF RECEIVER: Electrical Characteristics

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Frequency Detect Bandwidth		±(1.5+2Hz)	±2.3	±3.5	%Fo
Amplitude for Detection		-32		-2	dBm
Twist Tolerance		-10		+10	dB
60Hz Tolerance				0.8	Vrms
Dial Tone Tolerance	Precise Dial Tone			0	dB*
Speech Immunity	MITEL Tape #CM7290		2		hits
Noise Tolerance	MITEL Tape #CM7290			-12	dB*
Input Impedance		100			KΩ
* Referenced to lowest amplitude tone					

DTMF RECEIVER: Timing Characteristics

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
TON	Tone Time for Detect		40			ms
TON	Tone Time for No Detect				20	ms
TOFF	Pause Time for Redetection		40			ms
TOFF	Pause Time for Bridging				20	ms
TD1	Detect Time		25		46	ms
TR1	Release Time		35		50	ms

DTMF RECEIVER: Timing Characteristics (continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
TSU1 Data Set Up Time		7			µs
THD1 Data Hold Time		4.2		5.0	ms
Output Enable Time				200	ns
Output Disable Time				200	ns

DTMF GENERATOR: Electrical Characteristics

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Frequency Accuracy		-1.0		+1.0	%Fo
Output Amplitude	R1 = 100Ω to Vn, Vp - Vn = 5.0V				
Low Band		-9.2		-7.2	dBm
High Band		-6.6		-4.6	dBm
Output Distortion	DC to 50KHz			-20	dB

DTMF GENERATOR: Timing Characteristics

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
TSTART Start-Up Time				2.5	µs
TSU2 Data Set-Up Time		100			ns
THD2 Data Hold Time		50			ns
TRP RESET Pulse Width		100			ns
TPW $\overline{\text{LATCH}}$ Pulse Width		100			ns

CALL PROGRESS DETECTOR: Electrical Characteristics

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Amplitude for Detection	305Hz-640Hz	-40		0	dBm
Amplitude for No Detecion	305Hz-640Hz			-50	dBm
	f>2200Hz, <160Hz			-25	dBm
Detect Output	Logic 0			.5	V
	Logic 1	4.5			V
"LIN" Input	Max. Voltage	V_{DD}-10		V_{DD}	V
Input Impedance	500Hz	100			KΩ

CALL PROGRESS DETECTOR: Timing Characteristics

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
TON Signal Time for Detect		40			ms
TON Dignal Time for No Detect				10	ms
TOFF Interval Time for Detect		40			ms
TOFF Interval Time fo No Detect				20	ms
TD2 Detect Time				40	ms
TR2 Release Time				40	ms

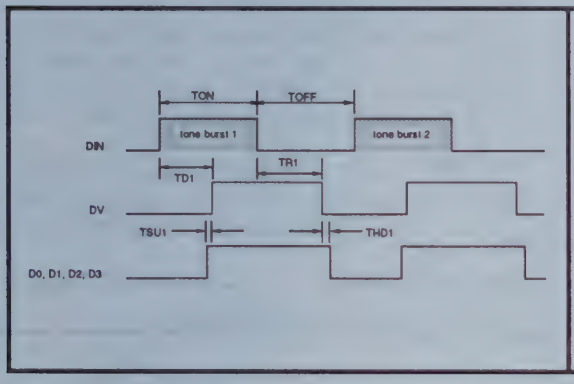


FIGURE 6: DTMF Decoder

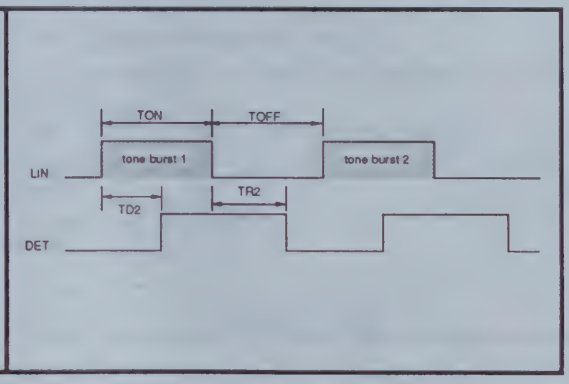


FIGURE 7: Call Progress Detector

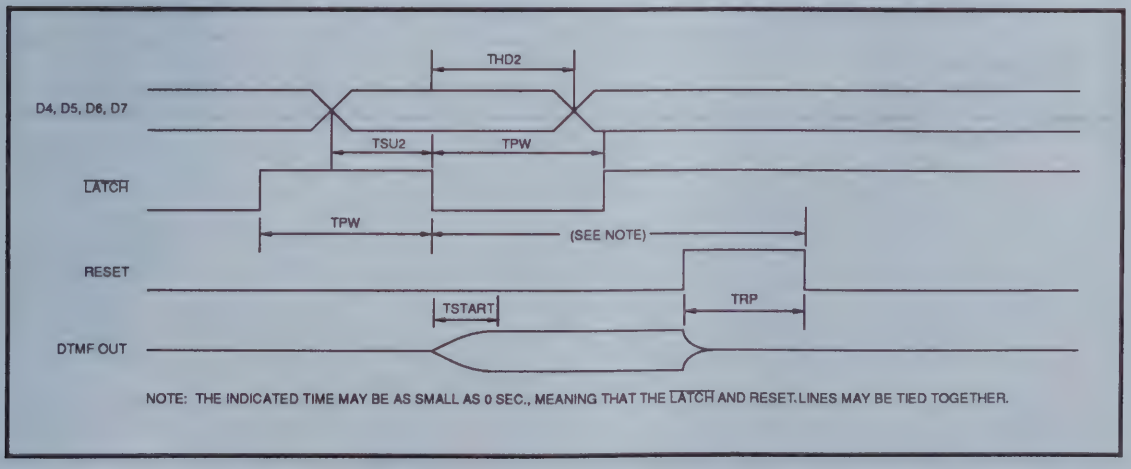
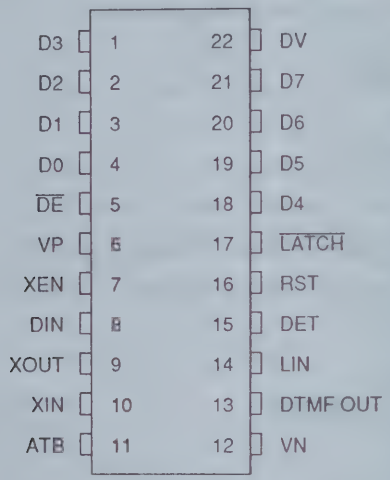


FIGURE 8: DTMF Generator

SSI 75T2090
DTMF Transceiver with Call Progress Detection

PACKAGE PIN DESIGNATIONS
(TOP VIEW)



22-Pin DIP

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 75T2090 22-Pin DIP	SSI 75T2090 - IP	75T2090 - IP

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SSI 75T2091
DTMF Transceiver with Early Detect & Call Progress Detection

May, 1989

DESCRIPTION

Silicon Systems' SSI 75T2091 is a complete Dual-Tone Multifrequency (DTMF) Transceiver that can both generate and detect all 16 DTMF tone-pairs. The SSI 75T2091 circuit integrates the performance proven SSI 75T203 DTMF receiver with a new DTMF generator circuit.

The DTMF receiver electrical characteristics are identical to the standard SSI 75T203 device characteristics. The DTMF generator provides performance similar to the Mostek MK5380, but with an improved (tighter) output amplitude range specification and with the addition of independent latch and reset controls.

An additional feature of the SSI 75T2091 is "imprecise" call progress detector. The detector detects the presence of signals in the 305-640 Hz band.

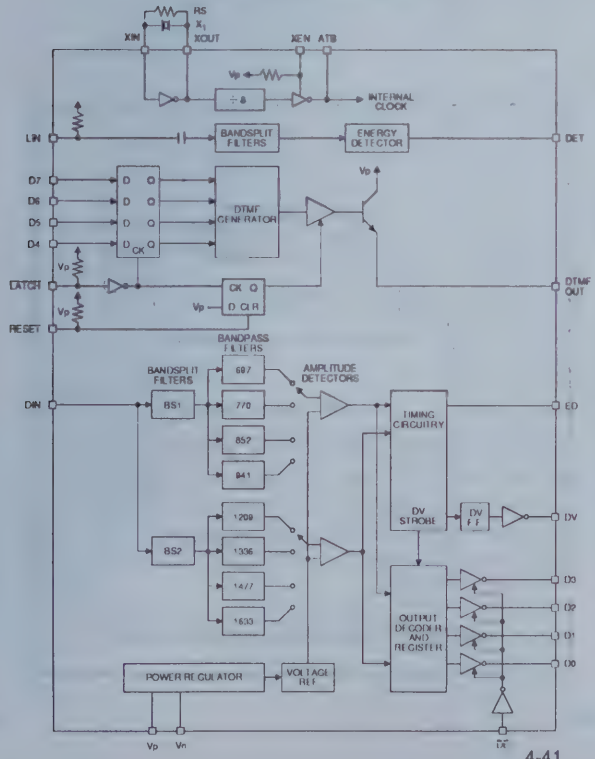
(Continued)

FEATURES

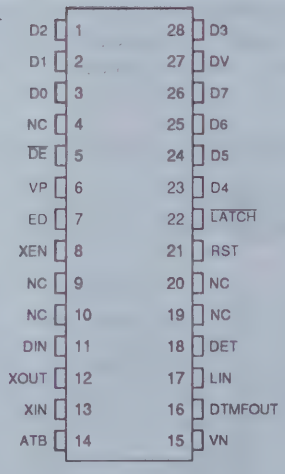
- DTMF Generator and Receiver on one-chip
- Call progress detection
- Early detect output
- DTMF Receiver exhibits excellent speech immunity
- Analog input range from –32 to –2 dBm (ref 600 Ω)
- Three-state outputs (4-bit hexadecimal) from DTMF Receiver
- AC coupled, internally biased analog input
- Latched DTMF Generator inputs
- DTMF output typ. –8 dBm (Low Band) and –5.5 dBm (High Band)
- Easy interface for microprocessor dialing
- Uses inexpensive 3.579545 MHz crystal for reference
- Low-power 5 volt CMOS
- 28-pin DIP or PLCC

4

BLOCK DIAGRAM



PIN DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

DESCRIPTION (Continued)

The only external components necessary for the SSI 75T2091 are a 3.58 MHz "colorburst" crystal with a parallel 1MΩ resistor. This provides the time base for digital functions and switched-capacitor filters in the device. No external filtering is required.

CIRCUIT OPERATION

RECEIVER

The DTMF Receiver in the SSI 75T2091 detects the presence of a valid tone pair (indicating a single dialed digit) on a telephone line or other transmission medium. The analog input is pre-processed by 60 Hz reject and band-splitting filters, then hard-limited to provide Automatic Gain Control. Eight bandpass filters detect the individual tones. The digital post-processor times the tone durations and provides the correctly coded digital outputs. The outputs will drive standard CMOS circuitry, and are three-state enabled to facilitate bus-oriented architectures.

DIN

This pin accepts the analog input. It is internally biased so that the input signal may be AC coupled. The input may be DC coupled as long as it does not exceed the positive supply. Proper input coupling is illustrated in Figure 1.

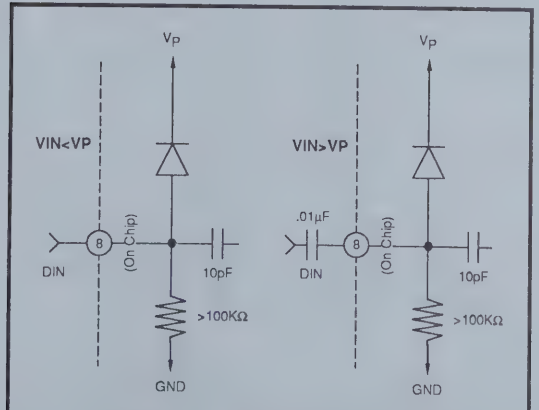


FIGURE 1: INPUT COUPLING

The SSI 75T2091 is designed to accept sinusoidal input waveforms but will operate satisfactorily with any input that has the correct fundamental frequency with harmonics greater than -20 dB below the fundamental.

CRYSTAL OSCILLATOR

The SSI 75T2091 contains an onboard inverter with sufficient gain to provide oscillation when connected to a low-cost television "color-burst" crystal. The crystal is placed between XIN and XOUT in parallel with a 1MΩ resistor, while XEN is tied high. Since the switched-capacitor-filter time base is derived from the crystal oscillator, the frequency accuracy of all portions of the SSI 75T2091 depends on the time base tolerance. The SSI DTMF Receiver frequency response and timing is specified for a time base accuracy of at least ±0.005%. ATB is a clock frequency output. Other devices may use the same frequency reference by tying their ATB pins to the ATB of a crystal connected device. XIN and XEN of the auxiliary devices must then be tied high and low respectively, XOUT is left floating. XOUT is designed to drive a resonant circuit only and is not intended to drive additional devices. Ten devices may run off a single crystal-connected SSI 75T2091 as shown in Figure 2.

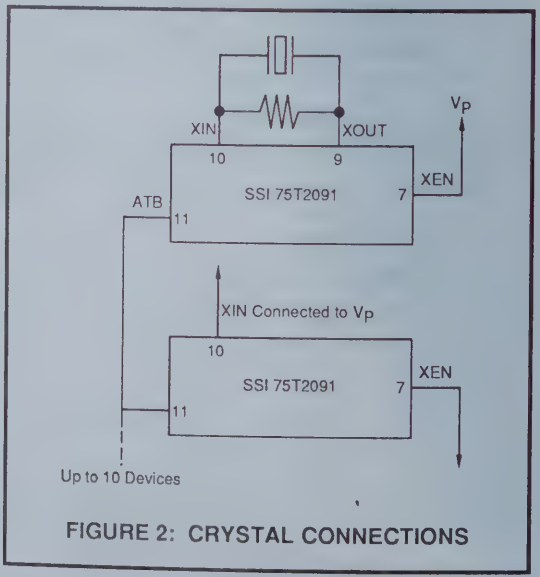


FIGURE 2: CRYSTAL CONNECTIONS

RECEIVER OUTPUTS AND THE $\overline{DE}$ PIN

Outputs D0, D1, D2, D3 are CMOS push-pull when enabled ($\overline{DE}$ low) and open-circuited (high impedance) when disabled ($\overline{DE}$ high). These digital outputs provide the hexadecimal code corresponding to the detected digit. Figure 3 shows that code.

The digital outputs become valid and DV signals a detection after a valid tone pair has been sensed. The outputs and DV are cleared when a valid pause has been timed.

	Hexadecimal Code			
Digit In / Out	D7 / D3	D6 / D2	D5 / D1	D4 / D0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
0	1	0	1	0
*	1	0	1	1
#	1	1	0	0
A	1	1	0	1
B	1	1	1	0
C	1	1	1	1
D	0	0	0	0

FIGURE 3

ED OUTPUT

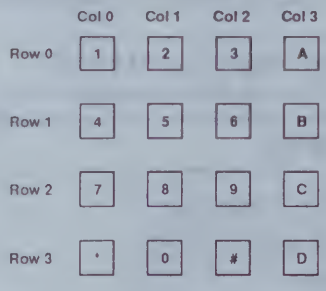
The ED output goes high as soon as the SSI 75T2091 begins to detect a DTMF tone pair and falls when the SSI 75T2091 begins to detect a pause. The D1, D2, D4, and D8 outputs are guaranteed to be valid when DV is high, but are not necessarily valid when ED is high.

GENERATOR

The DTMF generator on the SSI 75T2091 responds to a hexadecimal code input with a valid tone pair. Pins D4-D7 are the data inputs for the generator. A high to low transition on $\overline{LATCH}$ causes the hexadecimal code to be latched internally and generation of the appropriate DTMF tone pair to begin. The DTMF output is disabled by a high on RESET and will not resume until new data is latched in.

DIGITAL INPUTS

The D4, D5, D6, D7, $\overline{LATCH}$, RESET inputs to the DTMF generator may be interfaced to open-collector TTL with a pull-up resistor or standard CMOS. These inputs follow the same hexadecimal code format as the DTMF receiver output. Figure 4 shows the code for each digit. The dialing matrix and detection frequency table below list the frequencies of the digits.



NOTE: Column 3 is for special applications and is not normally used in telephone dialing.

FIGURE 4: DTMF DIALING MATRIX

DETECTION FREQUENCY

Low Group f_0	High Group f_0
Row 0 = 697Hz	Column 0 = 1209Hz
Row 1 = 770Hz	Column 1 = 1336Hz
Row 2 = 852Hz	Column 2 = 1477Hz
Row 3 = 941Hz	Column 3 = 1633Hz

DTMF OUT

The output amplitude characteristics listed in the specifications are given for a supply voltage of 5.0V. However, the output level is directly proportional to the supply, so variations in it will affect the DTMF output. A recommended line interface for this output is shown in Figure 5.

CALL PROGRESS DETECTION

The Call Progress Detector consists of a bandpass filter and an energy detector for turning the on/off cadences into a microprocessor compatible signal.

LIN INPUT

This analog input accepts the call progress signal and should be used in the same manner as the receiver input DIN.

DET OUTPUT

The output is TTL compatible and will be of a frequency corresponding to the various candences of Call Progress signals such as: on 0.5 sec/off 0.5 sec for a busy tone, on 0.25 sec/off 0.25 sec for a reorder tone and on 0.8-1.2 sec/off 2.7-3.3 sec for an audible ring tone.

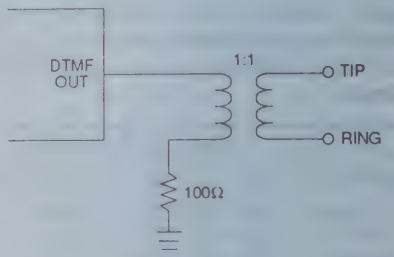


FIGURE 5: DTMF OUTPUT

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operating above absolute maximum ratings may damage the device.

PARAMETER	RATING	UNIT
DC Supply Voltage (Vp - Vn)	+7	V
Voltage at any Pin (Vn = 0)	-0.3 to Vp + 0.3	V
DIN Voltage	Vp + 0.5 to Vp - 10	V
Current through any Protection Device	±20	mA
Operating Temperature Range	-40 to + 85	°C
Storage Temperature	-65 to 150	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Supply Voltage		4.5		5.5	V
Power Supply Noise (wide band)				10	mV pp
Ambient Temperature		-40		+85	°C
Crystal Frequency (F Nominal = 3.579545MHz)		-0.01		+0.01	%
Crystal Shunt Resistor		0.8		1.2	MΩ
DTMF OUT Load Resistance		100			Ω

DIGITAL AND DC REQUIREMENTS

The following electrical specifications apply to the digital input and output signals over the recommended operating range unless otherwise noted. The specifications do not apply to the following pins: LIN, DIN, XIN, XOUT, and DTMF OUT. Positive current is defined as entering the circuit. Vn = 0 unless otherwise stated.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Supply Current*			15	30	mA
Power Dissipation				225	mW
Input Voltage High		0.7Vp			V
Input Voltage Low				0.3Vp	V
Input Current High				10	µA
Input Current Low		-10			µA
Output Voltage High	Ioh = -0.2mA	Vp-0.5			V
Output Voltage Low	Iol = +0.4mA			Vn+0.5	V

* with DTMF output disabled

DTMF RECEIVER: Electrical Characteristics

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Frequency Detect Bandwidth		±(1.5+2Hz)	±2.3	±3.5	%Fo
Amplitude for Detection	Each Tone	-32		-2	dBm/tone
Twist Tolerance		-10		+10	dB
60Hz Tolerance				0.8	Vrms
Dial Tone Tolerance	Precise Dial Tone			0	dB*
Speech Immunity	MITEL Tape #CM7290		2		hits
Noise Tolerance	MITEL Tape #CM7290			-12	dB*
Input Impedance		100			KΩ

* Referenced to lowest amplitude tone

DTMF RECEIVER: Timing Characteristics

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
TON	Tone Time for Detect		40			ms
TON	Tone Time for No Detect				20	ms
TOFF	Pause Time for Redetection		40			ms
TOFF	Pause Time for Bridging				20	ms
TD1	Detect Time		25		46	ms
TR1	Release Time		35		50	ms

DTMF RECEIVER: Timing Characteristics (Continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
TSU1 Data Set Up Time		7			µs
THD1 Data Hold Time		4.2		5.0	ms
TED ED Detect Time		7		22	ms
BER ED Release Time		2		18	ms
Output Enable Time				200	ns
Output Disable Time				200	ns

DTMF GENERATOR: Electrical Characteristics

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Frequency Accuracy		-1.0		+1.0	%Fo
Output Amplitude	R1 = 100Ω to Vn, Vp - Vn = 5.0V				
Low Band		-9.2		-7.2	dBm
High Band		-6.6		-4.6	dBm
Output Distortion	DC to 50KHz			-20	dB

DTMF GENERATOR: Timing Characteristics

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
TSTART Start-Up Time				2.5	µs
TSU2 Data Set-Up Time		100			ns
THD2 Data Hold Time		50			ns
TRP RESET Pulse Width		100			ns
TPW $\overline{\text{LATCH}}$ Pulse Width		100			ns

CALL PROGRESS DETECTOR: Electrical Characteristics

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Amplitude for Detection	305 Hz-640 Hz	-40		0	dBm
Amplitude for No Detection	305 Hz-640 Hz			-50	dBm
	f>2200 Hz, <160 Hz			-25	dBm
Detect Output	Logic 0			.5	V
	Logic 1	4.5			V
"LIN" Input	Max. Voltage	V_{DD}-10		V_{DD}	V
Input Impedance	500 Hz	100			KΩ

CALL PROGRESS DETECTOR: Electrical Characteristics (Continued)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
TON	Signal Time for Detect		40			ms
TON	Signal Time for No Detect				10	ms
TOFF	Interval Time for Detect		40			ms
TOFF	Interval Time for No Detect				20	ms
TD2	Detect Time				40	ms
TR2	Release Time				40	ms

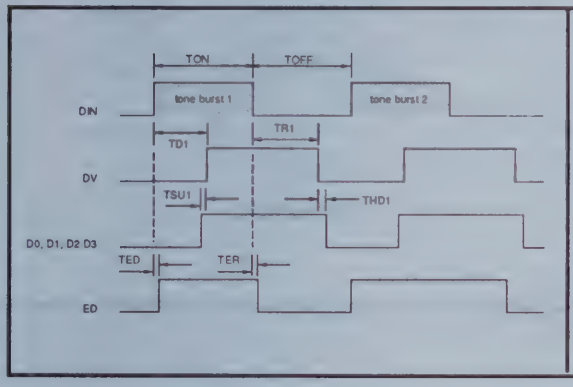


FIGURE 6: DTMF DECODER

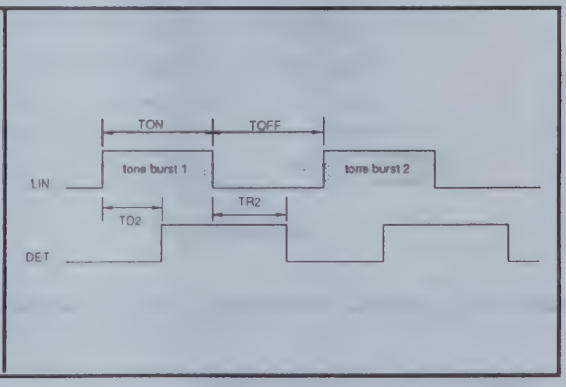


FIGURE 7: CALL PROGRESS DETECTOR

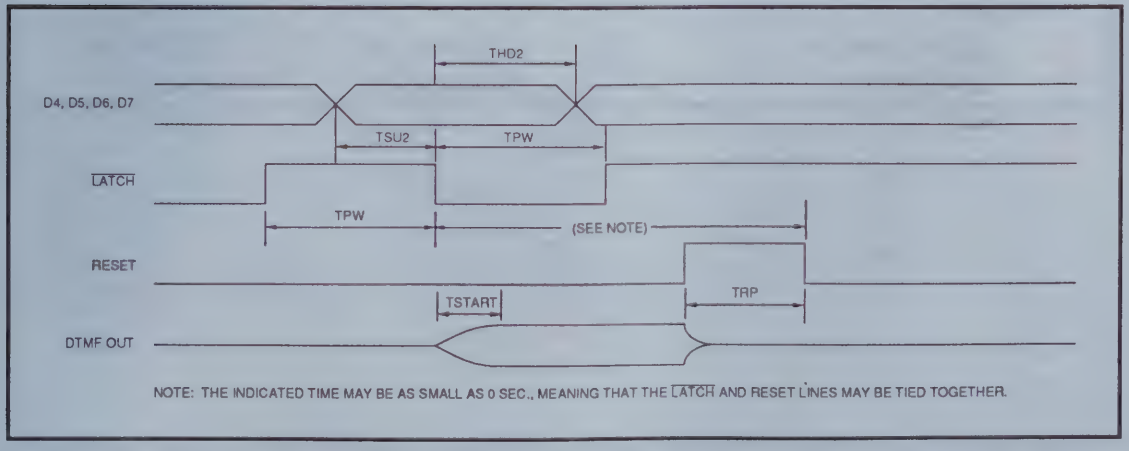
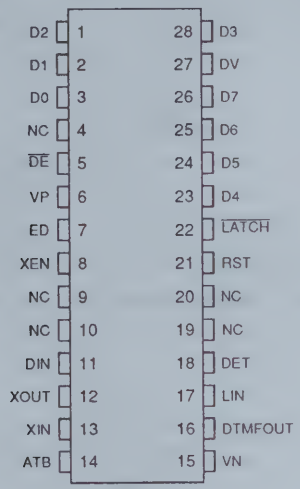


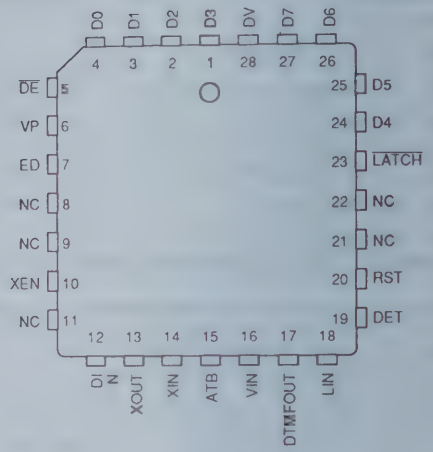
FIGURE 8: DTMF GENERATOR

SSI 75T2091
DTMF Transceiver with Early Detect & Call Progress Detection

PACKAGE PIN DESIGNATIONS
(TOP VIEW)



28-Pin DIP



28-Pin PLCC

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 75T2091		
28-Pin Plastic DIP	SSI 75T2091 - IP	75T2091 - IP
28-Pin PLCC	SSI 75T2091 - IH	75T2091 - IH

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SSI 75T957/957A
DTMF Receiver with Dial Tone Reject Filter

May, 1989

DESCRIPTION

The SSI 75T957/957A combines switched-capacitor and digital frequency measuring techniques to decode Dual-Tone Multifrequency (DTMF) signals to four bit binary data. Dial tone rejection and 60 Hz noise rejection filters are built in. Fabricated as a monolithic integrated circuit using low power CMOS processing, the SSI 75T957/957A is packaged in a 22-pin DIP or 24-pin SO. The SSI 75T957A will operate with a supply range of 5 to 12 volts; the 75T957 is for 5V-only operation. An inexpensive 3.58 MHz television crystal and a resistor are the only external components required. High system density may be achieved by using the clock output of one crystal-connected receiver to drive the time bases of additional receivers.

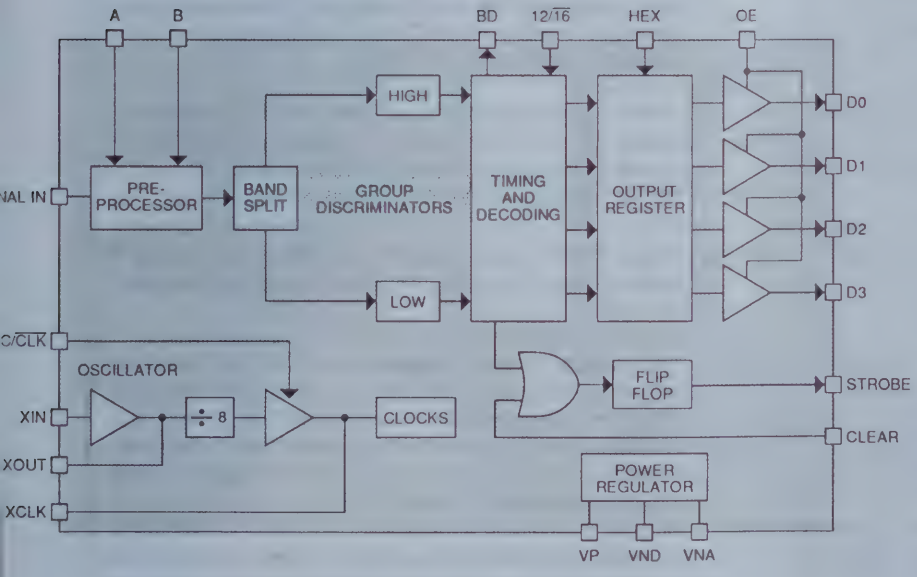
(Continued)

FEATURES

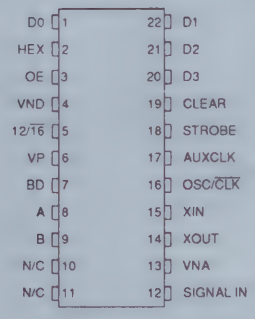
- Complete DTMF receiver in 22-pin DIP or 24-pin SO
- Decodes all 16 DTMF digits
- Excellent dial tone and speech immunity
- Meets telephone impulse noise immunity standards
- Digitally selectable sensitivity to -38 dBm
- Selectable 4-bit hexadecimal or binary-coded 2-of-8 output
- Fabricated using low-power CMOS technology
- Operates at 5V (75T957) or 12V (75T957A)
- Second source of Teltone M-957

4

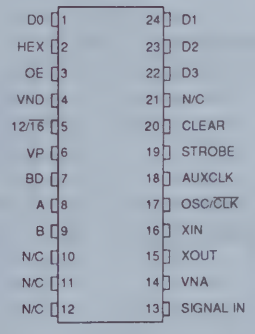
BLOCK DIAGRAM



PIN DIAGRAMS



22-pin DIP



24-pin SO

CAUTION: Use handling procedures necessary for a static sensitive component.

DESCRIPTION (Continued)

The SIGNAL IN input to the SSI 75T957/957A interfaces readily to telephone lines, radio receivers, tape players and other DTMF signal sources. Inputs A and B control sensitivity to a maximum of -38 dBm, while the 12/$\overline{16}$ input determines the signals to be detected. The pre-processing stages of the SSI 75T957/957A filter out dial tone and noise, split the signal into its high frequency group and low frequency group components, and hard limit each component to provide automatic gain control. Four discriminators in each group then detect the individual tones. Post-processing stages of the SSI 75T957/957A time the tone durations and store binary data for outputting as determined by the HEX input. The STROBE output is activated by the presence of valid data in the output register and cleared by the detection of a valid end-of-signal pause or by the CLEAR input. An early signal presence indicator, BD, facilitates applications requiring tone blocking. The data outputs operate with simple logic circuits or microprocessors and are three-state enabled to facilitate bus-oriented architectures.

PIN DESCRIPTION

NAME	22-pin DIP	24-pin SO	TYPE	DESCRIPTION
SIGNAL IN	12	13	I	DTMF input. Timings are shown in Figure 1. Internally biased so that the input signal may be AC coupled. SIGNAL IN also permits DC coupling as long as the input voltage does not exceed the positive supply. Proper coupling is shown in Figure 3. See Table 1 for the frequency pairs associated with each DTMF signal.
12/$\overline{16}$	5	5	I	DTMF signal detection control. When 12/$\overline{16}$ is at logic "1," the SSI 75T957 detects the 12 most commonly used DTMF signals (1 through #). When 12/$\overline{16}$ is at logic "0," the SSI 75T957 detects all 16 DTMF signals (1 through D).
A, B	8, 9	8, 9	I	Binary DTMF signal sensitivity control inputs. A and B select the sensitivity of the SIGNAL IN input to a maximum of -38 dBm.
D3, D2 D1, D0	20, 21 22, 1	22, 23 24, 1	O	Data outputs. When enabled by the $\overline{OE}$ input, the data outputs provide the code corresponding to the detected digit in the format programmed by the HEX pin. See Table 1. The data outputs become valid after a tone pair has been detected and are cleared when a valid pause is timed. Timings are shown in Figure 1.
$\overline{OE}$	3	3	I	Output enable. When $\overline{OE}$ is at logic "1," the data outputs are in the CMOS push/pull state and represent the contents of the output register. When $\overline{OE}$ is driven to logic "0," the data outputs are forced to the high-impedance or "third" state. Timings are shown in Figure 1.

PIN DESCRIPTION (Continued)

NAME	22-pin DIP	24-pin SO	TYPE	DESCRIPTION
HEX	2	2	I	Binary output format control. When HEX is at logic "1" the output of SSI 75T957 is full, 4-bit binary. When HEX is at logic "0," the output is binary coded 2-of-8. Table 1 shows the output codes.
STROBE	18	19	O	Valid data indication. STROBE goes to logic "1" after a valid tone pair is sensed and decoded at the data outputs. STROBE remains at logic "1" until a valid pause occurs or the CLEAR input is driven to logic "1," whichever is earlier. Once cleared, STROBE will not rise to a logic "1" until a new valid tone (preceded by a valid pause) is detected. Timings are shown in Figure 1.
CLEAR	19	20	I	STROBE control. Driving CLEAR to logic "1" forces the STROBE output to logic "0." When CLEAR is at logic "0," STROBE is forced to logic "0" only when a valid pause is detected. Tie to VNA or VND when not used.
BD	7	7	O	Button down. A logic "1" BD indicates a signal has been detected and is being validated. BD precedes STROBE and data outputs.
XIN, XOUT	15, 14	16, 15	I	Crystal connections. When an auxiliary clock is used, XIN should be tied to logic "1." See Figure 4.
OSC/$\overline{\text{CLK}}$	16	17	I	Time base control. When OSC/$\overline{\text{CLK}}$ is at logic "1," the output of the SSI 75T957's internal oscillator is selected as the time base. When OSC/$\overline{\text{CLK}}$ is at logic "0" and XIN is at logic "1," the AUXCLK input is selected as the time base.
AUXCLK	17	18	O	Auxiliary clock input. When OSC/$\overline{\text{CLK}}$ is at logic "0" and XIN is at logic "1," the AUXCLK input is selected as the SSI 75T957's time base. The auxiliary input must be 3.58 MHz divided by 8 for the SSI 75T957 to operate to specifications. If unused, AUXCLK should be left open.
VNA, VND	13, 4	14, 4	-	Negative analog and digital power supply connections. Separated on the chip for greater system flexibility, VNA and VND should be at equal potential.
VP	6	6	-	Positive power supply connection.
N/C	10, 11	10-12, 21	-	Not connected. These pins have no internal connection and may be left floating.

SSI 75T957/957A TIMING (-40°C ≤ TA ≤ +85°C; 4.5V ≤ VP ≤ 13.2V. Refer to Figure 1.)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
t_{ON}	Tone Time	for detection	40	-	-	ms
		for rejection	-	-	20	ms
t_{OFF}	Pause Time	for detection	40	-	-	ms
		for rejection	-	-	20	ms
t_D	Detect Time		25	-	46	ms
t_P	Release Time		35	-	50	ms
t_{SU}	Data Setup Time		7	-	-	µs
t_H	Data Hold Time		4.2	-	5.0	ms
tcl	Strobe Clear Time		-	160	250	ns
t_{PW}	Clear Pulse Width		200	-	-	ns
t_{BD}	BD Detect Time		7	-	22	ms
t_{BR}	BD Release Time		2	-	18	ms
	Output Enable Time	C_L = 50pF, R_L = 1KΩ	-	200	300	ns
	Output Disable Time	C_L = 35pF, R_L = 500Ω	-	150	200	ns
	Output Rise Time	C_L = 50pF	-	200	300	ns
	Output Fall Time	C_L = 50pF	-	160	250	ns

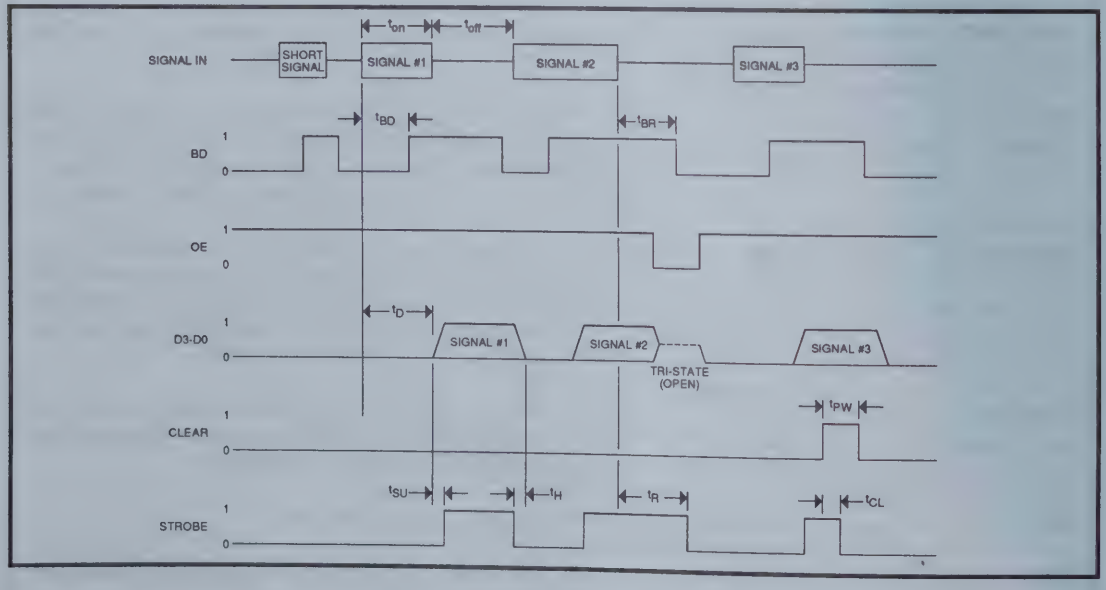


FIGURE 1: Timing Diagram

TABLE 1: DTMF TO BINARY DECODING

DIGIT	LOW-FREQUENCY COMPONENT (Hz)	HIGH-FREQUENCY COMPONENT (Hz)	HEX OUTPUT	BINARY CODED 2-OF-8 OUTPUT
			D3 D2 D1 D0	D3 D2 D1 D0
1	697	1209	0001	0000
2	697	1336	0010	0001
3	697	1477	0011	0010
4	770	1209	0100	0100
5	770	1336	0101	0101
6	770	1477	0110	0110
7	852	1209	0111	1000
8	852	1336	1000	1001
9	852	1477	1001	1010
0	941	1336	1010	1101
*	941	1209	1011	1100
#	941	1477	1100	1110
A	697	1633	1101	0011
B	770	1633	1110	0111
C	852	1633	1111	1011
D	941	1633	0000	1111

Note: The SSI 75T957 detects signals A through D when the 12/$\overline{16}$ input is at logic "0."

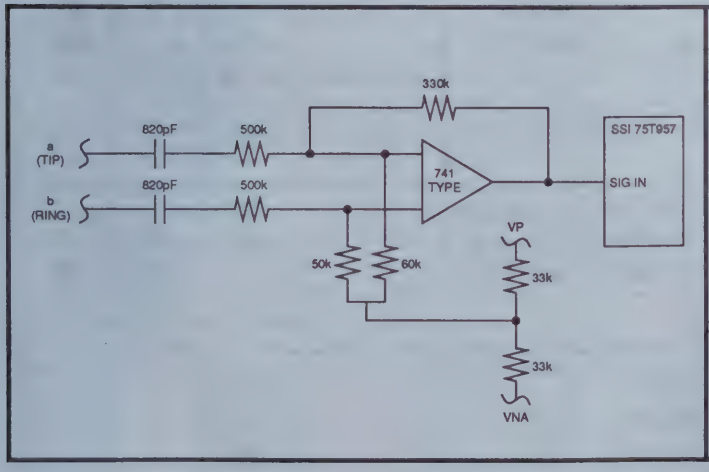
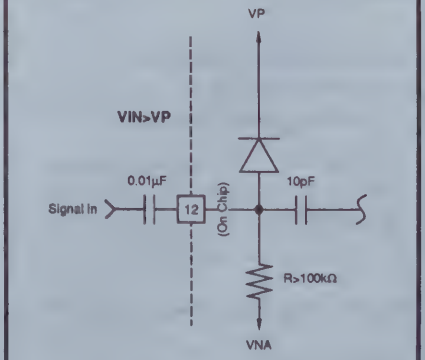


FIGURE 2: Telephone Line Differential Input Interface



NOTE: Coupling capacitor needn't be used when VIN is less than VP.

FIGURE 3: Input Signal Configuration

ABSOLUTE MAXIMUM RATINGS

(Operation above absolute maximum ratings may permanently damage the device.)

PARAMETER	CONDITIONS	RATING
DC Supply Voltage - V_P	VND=VNA=0V	16.0V
Input Voltage	All inputs except SIGNAL IN	(V_P + 0.5V) to (VND - 0.5V)
SIGNAL IN Voltage		(V_P + 0.5V) to (V_P - 22V)
Storage Temperature		-65° to 150°C
Operating Temperature		-40° to 85°C
Lead Temperature	Soldering, 5 sec.	260°C
Power Dissipation		1W

ELECTRICAL CHARACTERISTICS

(-40°C ≤ T_A ≤ +85°C)

PARAMETER	CONDITIONS		MIN	NOM	MAX	UNITS
SIGNAL IN Input Requirements						
Signal Level (per tone) (See Note 1)	V_P=12V	A=0, B=0	-24	-	+6	dBm
		A=1, B=0	-27	-	+3	dBm
		A=0, B=1	-30	-	0	dBm
		A=1, B=1	-	-32	-	dBm
	V_P=5V	A=0, B=0	-32	-	-2	dBm
		A=1, B=0	-35	-	-5	dBm
		A=0, B=1	-38	-	-8	dBm
		A=1, B=1	-	-40	-	dBm
Signal Frequency Deviation with Detection			±(1.5% +2)	±2.5%		Hz
Signal Frequency Deviation without Detection			±3.5%	±3.0%	-	Hz
Twist	See Note 2	-	-	±10	dB	
Gaussian Noise	See Note 3	-	12	A-7	dB	
Dial Tone Level (per tone)	F ≤ 480 Hz; see Note 4		-	-	A+22	dB
Digital Input Requirements (See Note 5)						
Logic 0 Voltage	V_P=12V	0	-	3.6	V	
	V_P=5V	0	-	1.5	V	
Logic 1 Voltage	V_P=12V	8.4	-	12.0	V	
	V_P=5V	3.5	-	5.0	V	

ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Digital Output Characteristics (See Note 5)					
Logic 0 Voltage	V_P=12V, Io = 1.0mA	0	-	1.2	V
	V_P=5V, Io = 0.4mA	0	-	0.5	V
Logic 1 Voltage	V_P=12V, Io = -0.5mA	10.8	-	12.0	V
	V_P=5V, Io = -0.2mA	4.5	-	5.0	V
Three-State Leakage		-	-	10.0	µA
Miscellaneous Characteristics					
CMOS Latch-up Voltage	See Note 7	20	-	-	V
SIGNAL IN Input Impedance	F=1kHz||15pF	100k	-	-	Ω
Power Requirements					
Supply Current	V_P=12V	-	20	40	mA
	V_P=5V	-	9	18	mA
Power Dissipation	V_P=12V, see Note 6	-	204	480	mW
(outputs open)	V_P=5V, see Note 6	-	30	90	mW
Power Supply Wide Band Noise	A=0, B=0				
	V_P=12V	-	-	25	mVpp
	V_P=5V	-	-	10	mVpp

Notes:
1. With an ambient temperature of 25°C, the signal duration and signal interval are at minimum, and the signal frequency deviation and twist are at maximum. The unit "dBm" refers to decibels above or below a reference power of one milliwatt into a 600-ohm load. (For example, -24dBm equals 49mVrms.)
2. Twist is defined as the ratio of the level of the high-frequency DTMF component to the level of the low-frequency DTMF component.
3. With an ambient temperature of 25°C, the signal level is at A+5, the signal frequency deviation and twist are at 0, and the signal applied is 50ms off and 50ms on. The A level is the minimum detect level selected.
4. The signal duration and signal interval are at minimum, and the signal frequency deviation and twist are at maximum. The A level is the minimum detect level selected.
5. Logic levels shown are referenced to VND.
6. For an ambient temperature of 25°C.
7. Power supply excursions above this value can cause device damage.

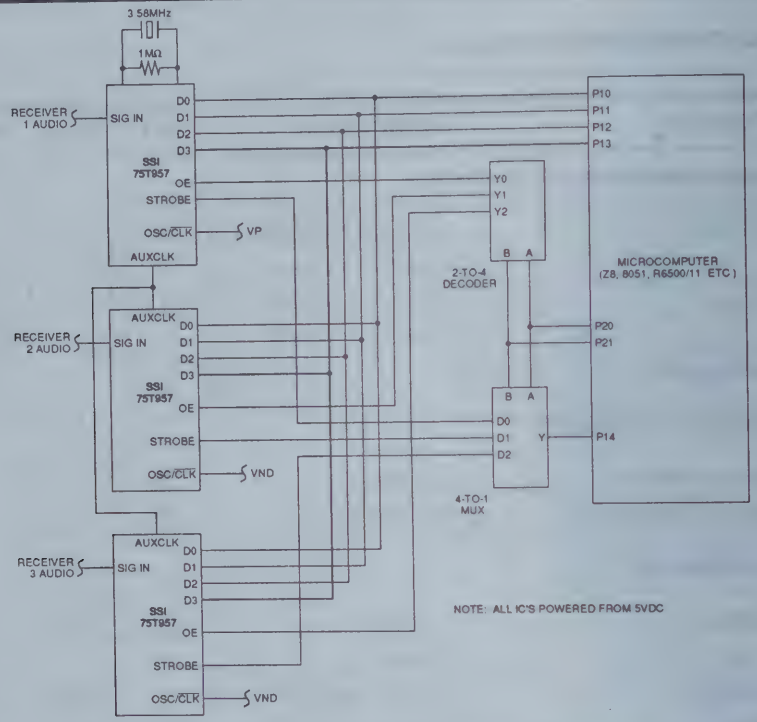


FIGURE 4: Multiple Receiver/Microprocessor Interface

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 75T957 22-pin Plastic DIP, 5V-only	SSI 75T957-IP	75T957-IP
SSI 75T957 24-pin SOL, 5V-only	SSI 75T957-IL	75T957-IL
SSI 75T957A 22-pin Plastic DIP, 5-12V operation	SSI 75T957A-IP	75T957A-IP
SSI 75T957A 24-pin SOL, 5-12V operation	SSI 75T957A-IL	75T957A-IL

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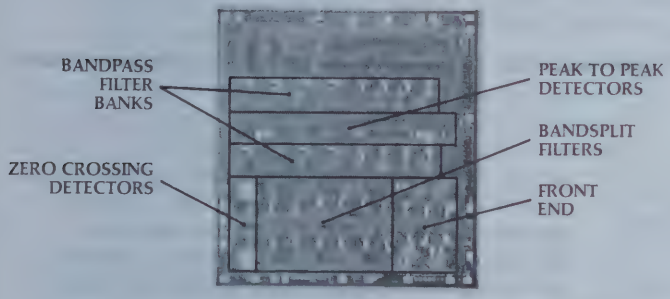
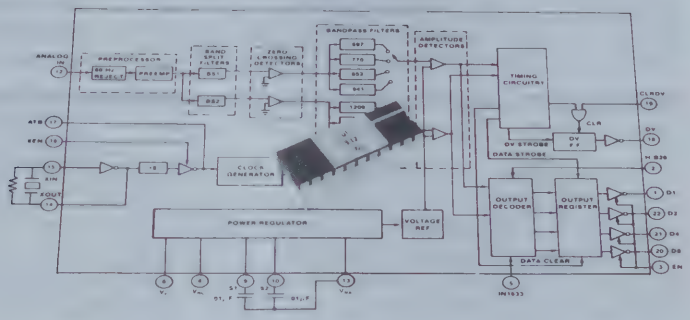
Application Guide

SSi Monolithic Dual-Tone Multi-Frequency (DTMF) Receivers





4

INTRODUCTION

The Silicon Systems integrated DTMF Receivers and Transceivers are complete Touch-Tone™ detection and generation systems. Each can operate in a stand-alone mode for the majority of telecommunications applications, thereby providing the most economical implementation of DTMF signaling systems possible. Each combines precision active filters and analog circuits with digital control logic on a monolithic CMOS integrated circuit. SSI DTMF chip use is straightforward and the external component requirements are minimal. This application guide describes device operation, performance, system requirements and typical application circuits for the SSI DTMF chips.

HOW THE SSI DTMF CIRCUITS WORK

GENERAL DESCRIPTION OF OPERATION

The task of a DTMF Receiver is to detect the presence of a valid DTMF signal on a telephone line or other transmission medium. The presence of a valid DTMF signal indicates a single dialed digit; to generate a valid digit sequence, each DTMF signal must be separated by a valid pause.

Table 1 gives the established Bell system standards for a valid DTMF signal and a valid pause. The SSI DTMF Receivers meet or exceed these standards.

PARAMETER	VALUE
One Low-Group Tone, and	697, 770, 852 or 941 Hz
One High-Group Tone	1209, 1336, 1477 or 1633 Hz
Frequency Tolerance	fo ± (1.5% + 2 Hz)
Amplitude Range	–24 dB ≤ A ≤ 6 dBm @ 600Ω (Dynamic Range 30 dB)
Relative Amplitude (Twist)	$-8\,dB \le \frac{\text{High Group Tone}}{\text{Low Group Tone}} \le +4\,dB$
Duration	40 ms or longer
Inter-tone Pauses	40 ms or longer

Table 1: Bell System Standards

GENERAL DESCRIPTION (Continued)

Similar device architecture is used in all SSI DTMF Receivers. Figure 1 shows the SSI 75T202 Block Diagram. This architecture is implemented in all SSi single chip receivers, as well as SSi Transceivers. In general terms, the detection scheme is as follows: The input signal is pre-filtered and then split into two bands, each of which contains only one DTMF tone group. The output of each band-split filter is amplified and limited by a zero-crossing detector. The limited signals, in the form of square waves, are passed through tone frequency bandpass filters. Digital logic is then used to provide detector sampling and determine detection validity, to present the digital output data in the correct format, and to provide device timing and control.

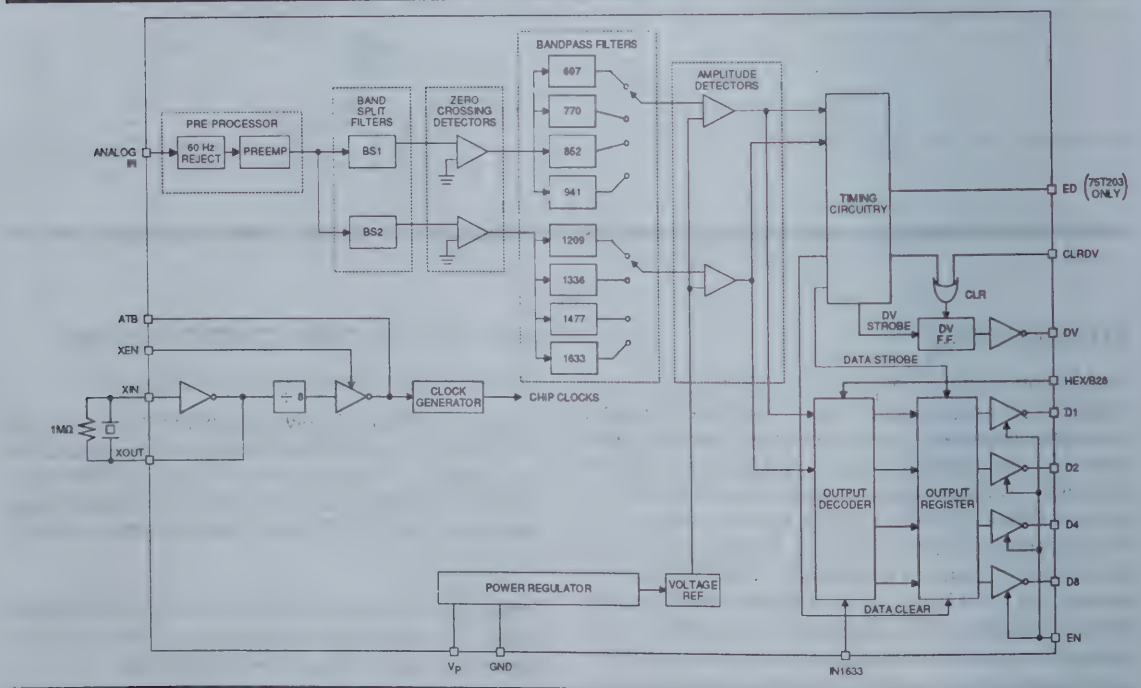


Figure 1: SSI 75T202 Block Diagram

PERFORMANCE CONSTRAINTS

SPEECH IMMUNITY AND NOISE TOLERANCE

The two largest problems confronting a DTMF Receiver are:

1) Distinguishing between valid DTMF tone pairs and other speech or stray signals that contain DTMF tone pair frequencies. This is referred to as Speech Immunity.

2) Detecting valid tone pairs in the presence of noise, which is typically found in the telephone (or other transmission medium) environment. This is referred to as Noise Tolerance.

The SSI DTMF Receivers use several techniques to distinguish between valid tone pairs and other stray signals. These techniques are explained in later sections. Briefly, the techniques are:

1) Pre-filtering of audio signal. Removes supply noise and dial tone from input audio signal and emphasizes the voice frequency domain.

2) Zero-cross detection. Limits the acceptable level of noise during detection of a tone pair. Important for speech rejection.

3) Valid tone pair/pause sampling. Samples the detection filters and checks for consistency before determining that a received tone pair or pause is valid.

DETAILED DESCRIPTION OF OPERATION

AUDIO PREPROCESSOR

The Audio Preprocessor is an analog filter that band limits the input analog signal between 500 Hz and 6 KHz. In addition, it emphasizes the 2 KHz to 6 KHz voice region.

Band limiting suppresses power supply and dial tone frequencies, and high frequency noise. The emphasized voice region helps to equalize the audio response since many phone lines tend to roll off at about 1 KHz. In addition, preservation of the upper voice frequencies is important in providing speech immunity.

TONE BAND SPLITTING

After the analog signal is preprocessed, it is then split into two bands, each of which contains only one DTMF tone group. The band-split filters are actually band-stop filters to maintain all frequencies except the *other* tone group; this is done to maintain all analog information to enhance speech immunity but not allow the other tone group to act as interfering noise for the band being detected. These band-stop filters have "floors" that limit the amount of tone pair twist which further enhances speech immunity. See device data sheets for acceptable twist limits.

ZERO-CROSSING DETECTORS

The output of each band-split filter is amplified and limited by a zero-crossing detector (limiter). The function of the zero-crossing detector is to produce a square wave at the prime frequency emanating from the band-split filter. If a pure tone is not present, as in the case of voice or other interfering noise, a rectangular wave with a variable period will result. Proportional to the interference, the limiter output power is spread over a broad frequency range as the zero crossings "dither." When a high level of noise or speech occurs, no single bandpass filter pair will contain significant power long enough to result in a tone detection. On the other hand, when a pure DTMF tone exists with acceptable noise levles, the output of the limiter will not have any significant dither and tone detection will occur. The zero-crossing detector also acts as AGC (Automatic Gain Control) in that the output amplitude is independent of input amplitude; this additionally establishes an acceptable signal-to-noise ratio not dependent on tone amplitude.

BANDPASS FILTERS & AMPLITUDE DETECTORS

The bandpass filters perform tone frequency discrimination. Their responses are tailored so that if the frequency of the limited square wave from the zero-crossing detector is within the tone frequency tolerance, the fitler output will exceed the amplitude detector threshold. The amplitude detectors are interrogated periodically by the digital control circuitry to acertain the presence of only one tone in each band for the required duration. In a similar fashion, valid pauses are measured by the absence of valid tone pairs for the specified time.

TIMING AND LOGIC

During the qualification process, the output decoder gererates the proper digital code for the received DTMF tone pair. After the fidelity and duration of this signal have been verified, the timing circuitry latches this code into the output register and raises the data valid (DV) flag.

The only precision external element needed for the SSI DTMF Receivers is a 3.58 MHz parallel resonant crystal (color-burst frequency) with a .01% tolerance for the on-board oscillator. A 1 MΩ 10% resistor should be connected in parallel with the crystal. This generates the precise clock for the filters and for the logic timing and control of the chip.

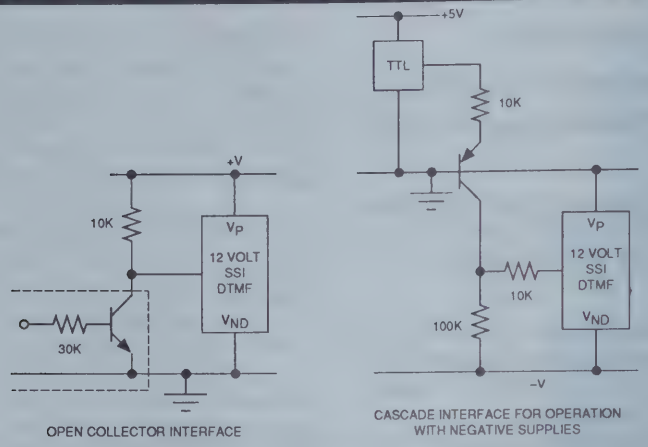


Figure 2: Interface Circuits for Conversion from TTL Output Levels to 12V SSI DTMF Input Levels

CIRCUIT IMPLEMENTATION

Standard CMOS technology is used for the entire circuit. Logic functions use standard low-power circuitry while the analog circuits use precision switched-capacitor-filter technology.

HOW TO USE THE SSI DTMF RECEIVERS

PRECAUTIONS

Although static protection devices are provided on the high-impedance inputs, normal handling precautions observed for CMOS devices should be used.

All CMOS parts are prone to a destructive latch-up mode. This behavior is inherent to these parts due to their physical structure. The latch-up mode can best be described as a low impedance, high current state existing between the power supply connections on a CMOS chip. This is also referred to as triggering of parasitic SCR behavior.

The most common cause of a latch-up mode is operating a CMOS part outside its rated power supply voltage. This over-voltage need not be applied at power supply pins only to cause latch-up. Latch-up can occur when over-voltage is applied at any input or output. For the SSI DTMF Receivers & Transceivers, the pin voltages should be constrained to the range between VN – 0.5V and VP + 0.5V (except the analog input pin whose conditions are discussed below). Clamping diodes should be utilized wherever necessary to ensure that voltage ratings are not exceeded.

Another cause for latch-up is fast dv/dt transients affecting the chip. These transients are encountered in applications that require the connection/disconnection of "live" boards. While these applications are very rare and their implementation is best avoided, it must be mentioned that whenever they are necessary, they present a severe environment for CMOS parts. Care must be taken in such instances to ensure that ground planes and rails are connected first and disconected last. This will go a long way in eliminating voltage transients.

Voltage transients that exist on power lines must also be eliminated. High voltage transients caused by switching of high current devices can trigger latch-up. High frequency decoupling is a requirement for the proper operation of the SSI DTMF devices. A 0.01µF to a 0.1µF ceramic decoupling capacitor should be connected to the power supply pin at the chip.

POWER SUPPLY

Excessive power supply noise should be avoided, and to aid the user in this regard, power supply hook-up options are provided on some devices.

Since the digital circuitry of the devices possess the high noise immunity characteristics of CMOS logic, it is the analog section that is affected most by power supply noise. On those SSI DTMF Receivers that have separate Analog Negative and Digital Negative supply connections (grounds), namely VNA and VND, an unfiltered supply may be used at VND. It is necessary that VND and VNA differ no more than 0.5V.

The analog circuitry of the devices require low power supply noise levels as specified on the device Data Sheet. The effects of excessive power supply noise are decreased tone amplitude sensitivity and less tone detection frequency bandwidth. Power supply noise can be significantly reduced by decoupling the chip with a 0.1µF

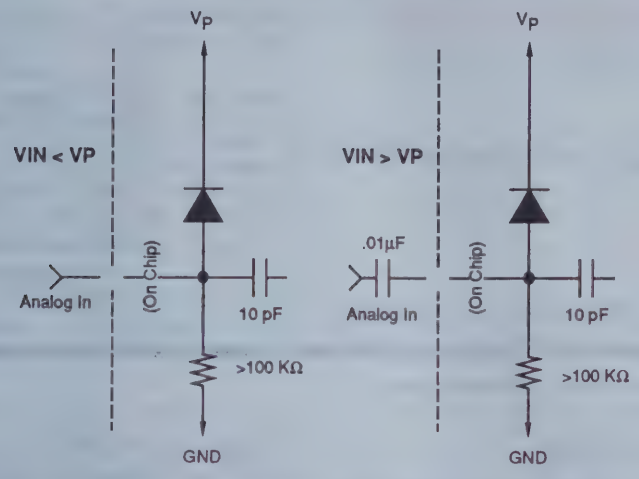


Figure 3: Direct and AC Coupled Configurations

ceramic capacitor. Power supply noise effects will be slightly less if the analog input is referenced to VP. This is normally accomplished by connecting VP to ground and utilizing a negative power supply.

DIGITAL INPUTS

The digital inputs are directly compatible with standard CMOS logic devices powered by VP and VN (or VND). The input logic levels should swing within 30% of VP or VN to insure detection. Any unused input must be tied to VN or VP. Figure 2 shows methods for interfacing TTL outputs to 12V SSI DTMF Receivers.

ANALOG INPUT

The analog input is the signal input pin for the devices, and is specially biased to facilitate its connection to external circuitry, as shown in Figure 3. The signal level at the analog input pin must not exceed the positive supply as stated on the device data sheets. If this condition cannot be guaranteed by the external circuitry, the signal must be AC coupled into the chip with a .01µF ± 20% capacitor.

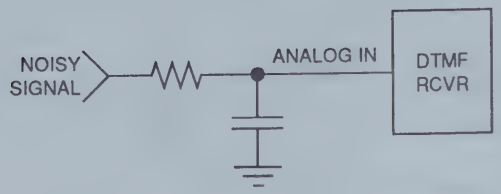
ANALOG INPUT NOISE

The SSI DTMF Receivers will tolerate wide-band input noise of up to 12 dB below the lowest amplitude tone component during detection of a valid tone pair. Any single interference frequency (including tone harmonics) between 1 KHz and 6 KHz should be at least 20 dB below the lowest amplitude tone component. Adherence to these conditions will ensure reliable detection and full tone detection frequency bandwidth. Because of the internal band limiting, noise with frequencies above 8 KHz can remain unfiltered. However, noise near the 56 KHz internal switched-capacitor-filter sampling frequency will be aliased (folded back) into the audio spectrum; noise above 28 KHz therefore should be low-pass filtered with a circuit as shown in Figure 4 using a cut-off frequency (Fc) of 6.6 KHz.

A 1 KHz cut-off frequency filter can be used on "normal" phone lines for special applications. When a phone line is particularly noisy, tone pair detection may be unreliable. A 1 KHz low pass filter will remove much of the noise energy but maintain the tone groups; however, a decreased speech immunity will result. This usage should only be considered for applications where speech immunity is not important, such as control paths that carry no speech.

Some DTMF tone pair generators output distorted tones which the SSI DTMF Receivers may not detect reliably (inexpensive extension telephones are an example). Most of the interfering harmonics of these may be removed by the use of a 3 KHz low-pass filter as in Figure 4. Some speech immunity degradation will result. It should be mentioned that when using low-pass filters, a higher cut-off frequency will preserve more of the speech immunity advantages.

The SSI DTMF Receivers provide superior speech immunity and noise rejection. The analog signals are subjected to stringent criteria and rigorous qualification in order to assure that only true DTMF tone pairs are detected and decoded properly. Stray signal and noise with sufficient amplitude will cause a DTMF receiver to disqualify a DTMF tone pair.



F_C (KHZ)	R (KΩ) (±5%)	C (μF) (±20%)
1.0	1.6	0.1
3.1	5.1	.01
6.6	2.4	.01

SUGGESTED
COMPONENT VALUES

Figure 4: Filter for Use in Noisy Environments

ANALOG INPUT NOISE (Continued)

Such a condition can be occasionally encountered when using DTMF "beepers." Beepers are normally used to transmit DTMF signals from dial-pulse phones. It has been observed that the non-linearity in the response of carbon microphones in telephone handsets introduces intermodulation products, which actually produce new frequency components. These components happen to fall direclty into the useful bandwidths of some of the basic tones that the receiver must detect. Because of the presence of these components (normally referred to as third-tone) with a valid DTMF tone, detection is disabled. To inhibit the more common higher frequency third tones from arriving to the receiver, the circuit shown in Figure 5 is suggested.

TELEPHONE LINE INTERFACE

In applications that use an SSI DTMF Receiver to decode DTMF signals from a phone line, a DAA (Direct Access Arrangement) must be implemented. Equipment intended for connection to the public telephone network must comply with and be registered in accordance to FCC Part 68. For PBX applications refer to EIA Standard RS-464.
Some of the basic guidelines are:

1) Maximum voltage and current ratings of the SSI DTMF Receivers must not be exceeded; this calls for protection from ringing voltage, if applicable, which ranges from 80 to 120V RMS over a 20 to 80 Hz frequency range.
2) The interface equipment must not breakdown with high-voltage transient tests (including a 2500V peak surge) as defined in the applicable document.
3) Phone line termination must be less than 200Ω DC and approximately 600Ω AC (200-3200 Hz).

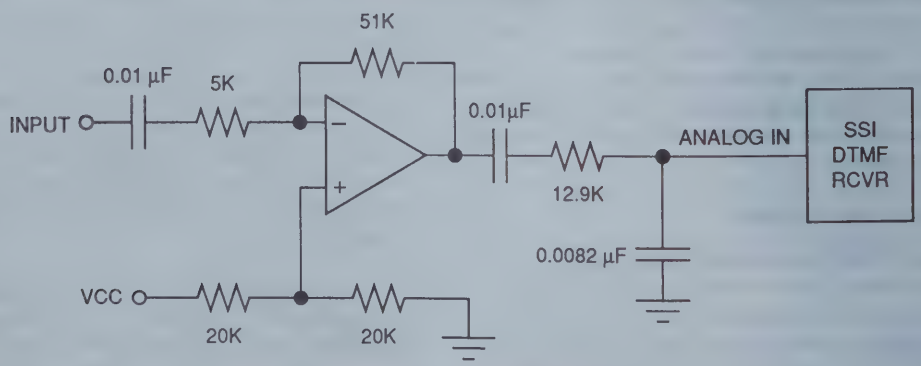


Figure 5: Filter for Use in Environments where a Third Tone Exists

4) Termination must be capable of sustaining phone line lop current (off-hook condition) which is typically 18 to 120 mA DC.

5) The phone line termination must be electrically balanced with respect to ground.

6) Public phone line termination equipment must be registered in accordance to FCC Part 68 or connected through registered protection circuitry. Registration typically takes about six months.

Ready made DAA devices are also available. One source is Cermetek Microelectronics, Sunnyvale, California.

Figure 6 shows a simplified phone line interface using a 600Ω 1:1 line transformer. Transformers specially designed for phone line coupling are available from many transformer manufacturers.
Figure 7 shows a more enhanced version of Figure 6. These added features include:

1) A 150V surge protector to eliminate high voltage spikes.

2) A Texas Instruments TCM 1520A ring detector, optically isolated from the supervisory circuitry.

3) Back-to-back Zener diodes to protect the DTMF (and optional multiplexer Op-Amp) from ringer voltage.

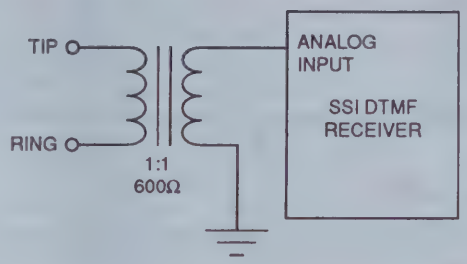


Figure 6: Simplified Phone Line Interface

4) Audio multiplexer which allows voice or other audio to be placed on the line (a recorded message, for example) and not interfere with incoming DTMF tone detection.

An integrated voice circuit may also be implemented for line coupling, such as the Texas Instruments TCM 1705A, however, this approach is typically more expensive than using a transformer as shown below.

OUTPUTS

The digital outputs of the SSI DTMF Receivers (except XOUT) swing between VP and VN (or VND) and are fully compatible with standard CMOS logic devices powered

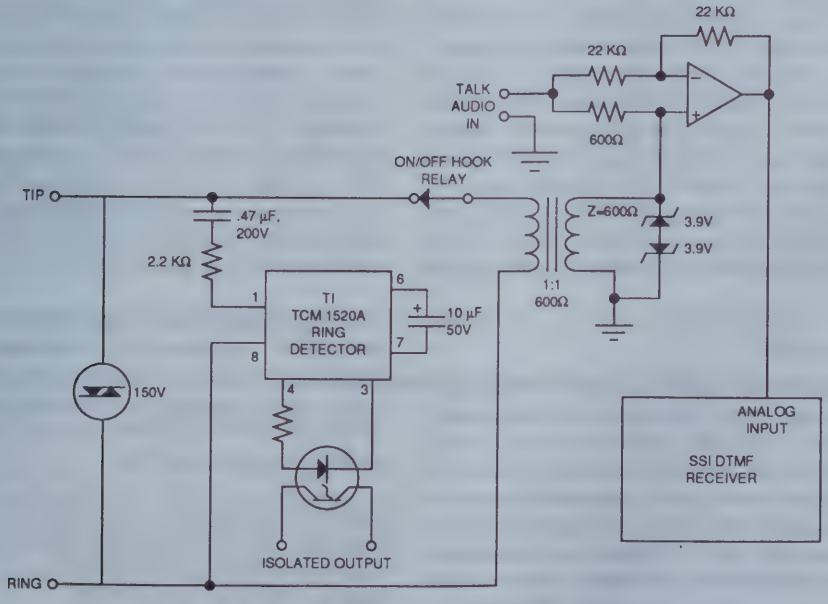


Figure 7: Full Featured Phone Line Interface

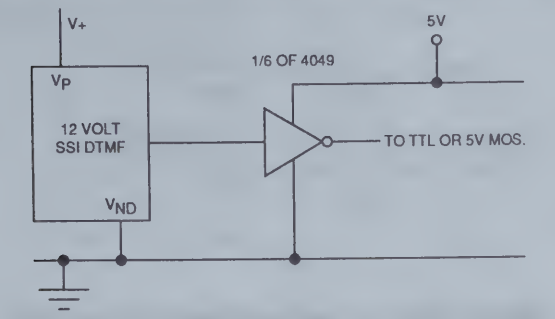


Figure 8: SSI 12V DTMF to TTL Level Interface

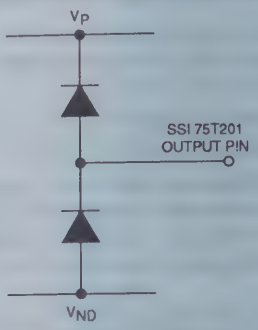


Figure 9: Equivalent Circuit of SSI DTMF Receiver Data Output in High Impedance State

from VP and VN. The 5V DTMF devices will also interface directly to LSTTL. The 12V DTMF devices can interface to TTL or low voltage MOS with the circuit in Figure 8.

Data Outputs D8, D4, D2 and D1 are three-state enabled to facilitate interface to a three-state bus. Figure 9 shows the equivalent circuit for the data outputs in the high impedance state. Care must be taken to prevent either substrate diode in Figure 9 from becoming forward biased or damage may result.

TIMING

Within 40 ms of a valid tone pair appearing at the DTMF Receiver Analog Input, the Data Outputs D8, D4, D2 and D1 will become valid. SSI 75T201 timing and specifications are shown in Figure 10 and Table 2 respectively (refer to the device data sheet for other timing diagrams). Seven microseconds after the data outputs have become valid DV will be raised. DV will remain high and the outputs valid while the valid tone pair remains present. Within 40 ms after the tone pair stops, the DTMF will recognize a valid pause. DV is lowered approximately 45 ms following the end of the tone pair, and the data outputs all set to zero 4.56 ms following Dv going low. DV will strobe at least for the same duration as the received tone pair.

SYSTEM INTERFACE

Provision has been made on the SSI DTMF Receivers for handshake interface with an outside monitoring system. In this mode, the DV strobe is polled by the monitoring system at least once every 40 ms to determine whether a new valid tone pair has been detected. If DV is high, the coded data is stored in the monitoring system and the CLRDV is pulsed high. With some systems operating in the handshake mode, it may be desirable to know when a valid pause has occurred. Ordinarily this would be indicated by the falling edge of DV. However, in the handshake mode, DV is cleared by the monitoring system each time a new valid tone pair is detected and, therefore, cannot be used to determine when a valid pause is detected. The detection of a valid pause in this case may be observed by detecting the clearing of the Data Outputs. Since, in hexadecimal format (the mode normally used with a handshake interface), the all zero state represents a commonly unused tone pair (D), the detection of a valid pause may be detected by connecting a four-input NOR gate to the device outputs and sensing the all zero state.

TIME BASE

The SSI DTMF Receivers contain an on-chip oscillator for a 3.5795 MHz parallel resonant quartz crystal or ceramic resonator. The crystal (or resonator) is placed between XIN and XOUT in parallel with a 1 MΩ resistor, while XEN is tied high. Since the switched-capacitor-filter time base is derived from the oscillator, the tone detect band frequency tolerance is proportional to the time base tolerance. The SSI DTMF Receiver frequency response and timing is guaranteed with a time base accuracy of at least ± 0.01%. To obtain this accuracy the CTS Part No. MP036 or Workman Part No. CY1-C or equivalent quartz crystal is recommended. In less critical applications a suitable ceramic resonator may be implemented.

The use of a ceramic resonator requires the addition of two 30 pF ± 10% capacitors; one between XIN and VN (or VND) and the other between XOUT and VN (or VND). Extra caution should be used to avoid stray capacitance on the resonant circuit when using a ceramic resonator instead of a quartz crystal.

When the oscillator is connected as above and XEN is tied high, the ATB (Alternate Time Base) pin delivers a square wave output at one-eighth the oscillator frequency (447.443 KHz nominal). The ATB pin can be converted to a time base input by tying XEN low; ATB can

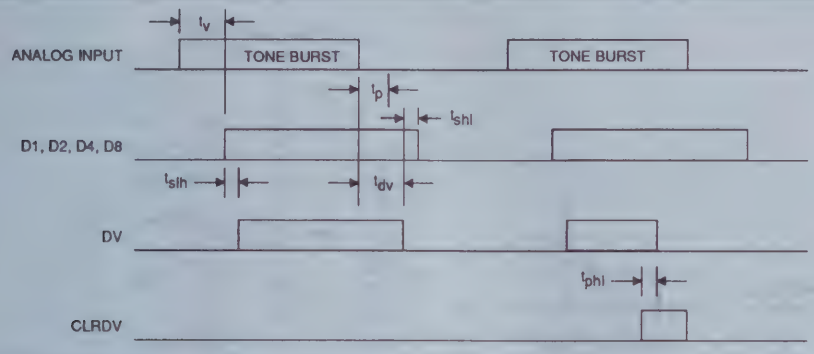


Figure 10: SSI 75T201 Timing Diagram

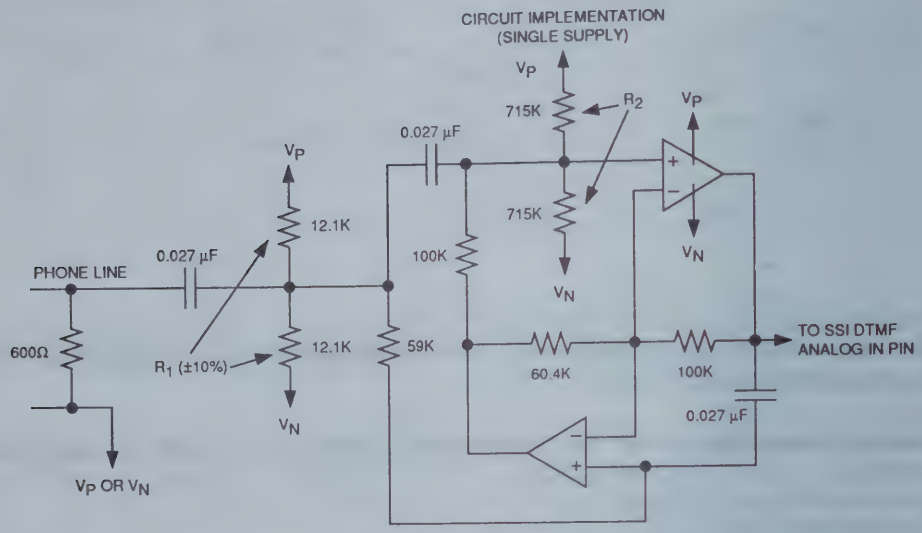
PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
t_v	Tone Detection Time		20	25	40	ms
t_{slh}	Data Overlap of DV Rising Edge	CLRDV = VND, EN = VP	7			µs
t_p	Pause Detection Time		25	32	40	ms
t_{dv}	Time between end of Tone and Fall of DV		40	45	50	ms
t_{shl}	Data overlap of DV Falling Edge		4	4.56	4.8	ms
t_{phl}	Prop. Delay: Rise of CLRDV to fall of DV	Cl = 300 pF Measured at 50% points			1	µs
	Output Enable Time	Cl = 300 pF, Rl = 10K See Note 1			1	µs
	Output Disable Time	Cl = 300 pF, Rl = 1K ΔV = 1V, See Note 2			1	µs
	Output 10-90% Transition Time	Cl = 300 pF			1	µs

Note 1: Measured from 50% point of Rising Edge of EN to the 50% point of the data output with Rl to opposite rail.
Note 2: Measured from 50% point of Falling Edge of EN to time at which output has changed 1V with Rl to opposite rail.

Table 2: SSI 75T201 Timing Specifications (−40°C ≤ TA ≤ +85°C, VP − VND = VP − VNA = 12V ± 10%)

then be externally driven from another device such as the ATB output of another DTMF. No crystal is required for the ATB input device; XIN must be tied high if unused. Several SSI DTMF Receivers can be driven with a single crystal (refer to device data sheet for fan-out limit).

XOUT is designed to drive a resonant circuit only and is not intended to drive additional devices. If a 3.58 MHz clock is needed for more than one device and it is desirable to use only one resonant device, an outside inverter should be used for the time base, buffered by a second inverter or buffer. The buffer output would then drive XIN of the SSI DTMF Receiver as well as the other device(s); XOUT must be left floating and XEN tied high.



Note: All resistors 1%, all caps 5%, unless noted, op-amps: 1/2 LM1458 or equivalent

Figure 11: Dial Tone Reject Filter

DIAL TONE REJECTION

The SSI DTMF Receivers incorporate enough dial tone rejection circuitry to provide dial tone tolerance of up to 0 dB. The SSI 75T957 Receiver has on-board circuitry that provides 22 dB dial tone tolerance. Dial tone tolerance is defined as the total power of precise dial tone (350 Hz and 440 Hz as equal amplitudes) relative to the lowest amplitude tone in a valid tone pair. The filter of Figure 11 may be used for further dial tone rejection. This filter exhibits an elliptic highpass response that provides a minimum of 18 dB rejection at 350 Hz, and 24 dB rejection at 440 Hz so long as the component tolerances indicated are observed. The DTMF on-chip filter rejects 350 Hz at least 6 dB more than 440 Hz. Therefore, employing the filter of Figure 11 yields a dial tone tolerance of +24 dB.

PRINTED CIRCUIT BOARD IMPLEMENTATION

The SSI DTMF Receivers are analog in nature and should be treated as such; circuit noise should be kept to a minimum. To be certain of this, all input and output lines should be kept away from noise sources (high frequency data or clock lines); this is especially true for the Analog Input. Noise in the ground or power supply lines can be avoided by running separate traces to supportive logic circuits or by running thicker (lower resistance) busses. Capacitance power supply bypassing should be performed at the device. Refer to the Power Supply section above.

PERFORMANCE DATA

A portion of the final SSI DTMF Receiver device characterization uses the Mitel CM7290 tone receiver test tape. The evaluation circuit shown in Figure 12 was used to characterize the SSI 75T201. The speed and output level of the tape deck must be adjusted so that the calibration tone at the beginning of the tape is at exactly 1000 Hz and 2V rms.

The Mitel tape tests yield similar results on all of the SSI DTMF Receivers. Test results for the SSI 75T201 are summarized in Table 3. In short, the measured performance data demonstrates that the SSI DTMF Receivers are monolithic realizations of a full "central office quality" DTMF Receiver.

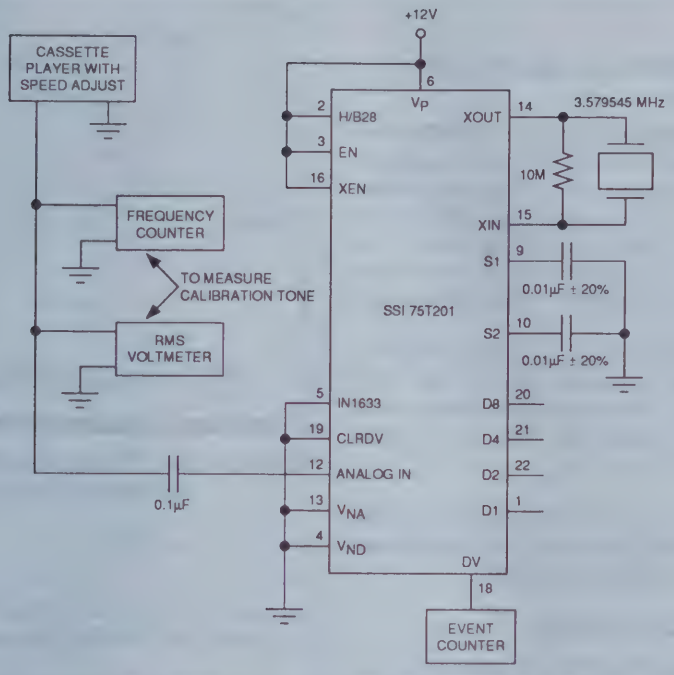


Figure 12: Circuit for Receiver Evaluation

TEST #	RESULTS
2a, b	B.W. = 5.0% of fo
2c, d	B.W. = 5.0% of fo
2e, f	B.W. = 5.3% of fo
2g, h	B.W. = 4.9% of fo
2i, j	B.W. = 5.0% of fo
2k, l	B.W. = 5.3% of fo
2m, n	B.W. = 5.3% of fo
2o, p	B.W. = 4.8% of fo
3	160 decodes
4	Acceptable Amplitude Ratio (Twist) = –19.1 dB to +15.2 dB
5	Dynamic Range = 32.5 dB
6	Guard Time = 23.3 ms
7	100% Successful Decodes at N/S Ratio of –12 dBV
8	2-3 Hits Typical on Talk-Off Test

Table 3: Mitel #CM7290 Tape Test Results for SSI 75T201 (Averaged for 10 parts)

APPLICATIONS

CREATING HEXADECIMAL "0" OUTPUT UPON DIGIT "0" DETECTION

To be consistent with pulse-dialing systems, the SSI DTMF Receivers provide a hexadecimal "10" output upon the detection of a digit "0" tone pair when in the hexadecimal code format. However, some applications may instead require a hexadecimal "0" with a digit "0" detection. The circuit of Figure 13 shows an easy method to recode the hexadecimal outputs to do this using only 4 NOR gates.

Note that this circuit will not give proper code for the "*", "B", or "C" digits and will cause both digits "D" and "0" to output hexadecimal "0." This circuit should therefore be considered for numeric digits only. The output code format is shown in Table 4.

This circuit is useful for applications that require a display of dialed digits; the digit display usually requires a hexadecimal "0" input for a "0" to be displayed.

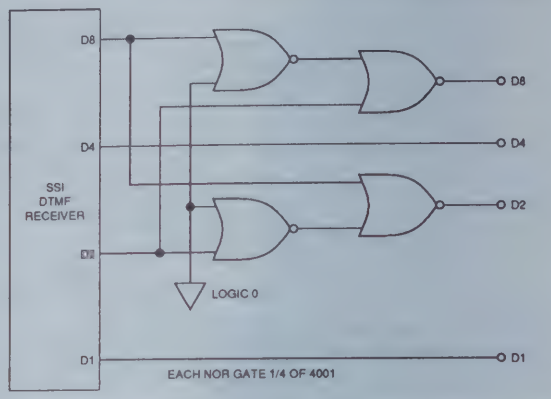


Figure 13: Hex "0" Out with Digit "0" Detect Conversion Circuit

16-CHANNEL REMOTE CONTROL

DTMF signaling provides a simple, reliable means of transmitting information over a 2-wire twisted pair. The complete schematic of a 16-channel remote control is shown in Figure 14. When one of the key pad buttons is depressed, a tone pair is sent over the transmission medium to the SSI DTMF Receiver.

The 4514 raises one of its 16 outputs in response to the 4-bit output code from the DTMF. The output at the 4514 will remain high until the next button is depressed.

Hexadecimal & Fig. 12 Circuit					Hexadecimal				
Digit	D8	D4	D2	D1	Digit	D8	D4	D2	D1
1	0	0	0	1	1	0	0	0	1
2	0	0	1	0	2	0	0	1	0
3	0	0	1	1	3	0	0	1	1
4	0	1	0	0	4	0	1	0	0
5	0	1	0	1	5	0	1	0	1
6	0	1	1	0	6	0	1	1	0
7	0	1	1	1	7	0	1	1	1
8	1	0	0	0	8	1	0	0	0
9	1	0	0	1	9	1	0	0	1
0	1	0	1	0	0	0	0	0	0
*	1	0	1	1	*	0	0	0	1
#	1	1	0	0	#	1	1	0	0
A	1	1	0	1	A	1	1	0	1
B	1	1	1	0	B	0	1	0	0
C	1	1	1	1	C	0	1	0	1
D	0	0	0	0	D	0	0	0	0

Table 4: Output Code of Figure 13

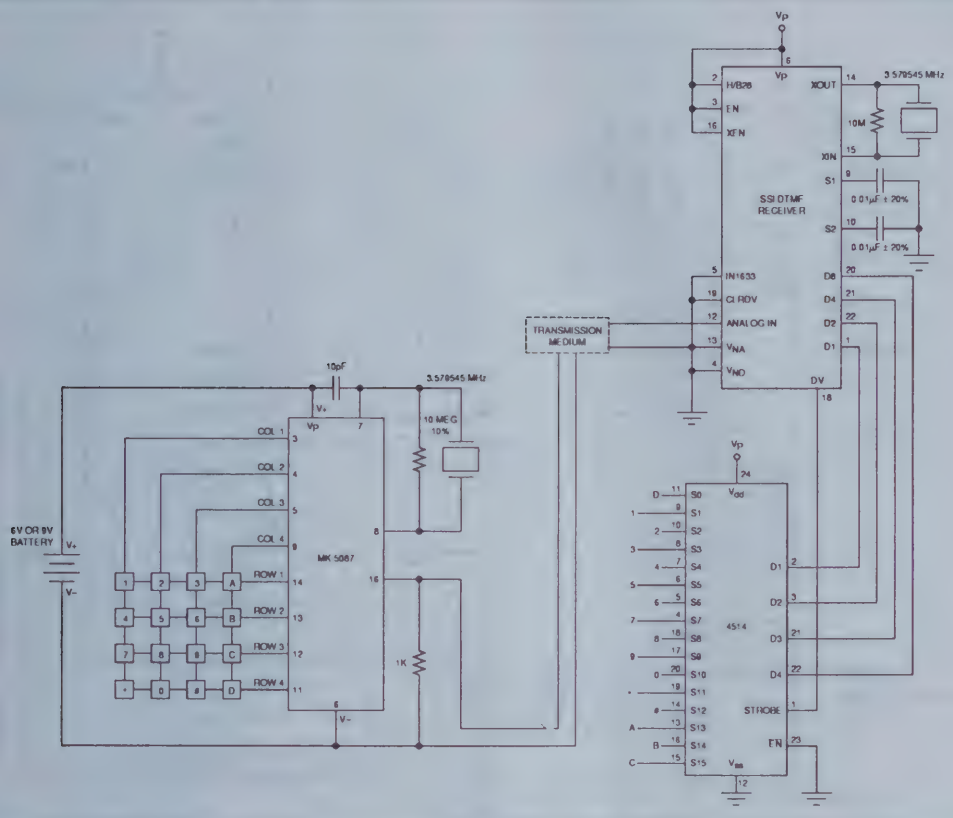


Figure 14: 16-Channel Remote Control

2-0F-8 OUTPUT DECODE

The circuit shown in Figure 15 can be used to convert the binary coded 2-of-8 to the actual 2-of-8 code (or 2-of-7 if detection of 1633 Hz tone is inhibited). The output data will be valid while DV is high. If it is desired to force the eight outputs to zero when a valid tone is not present, DV should be inverted and connected to both E–NOT inputs of the 4555.

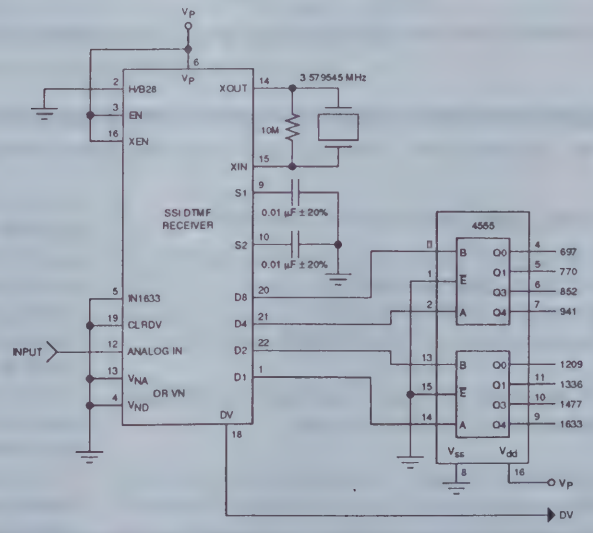


Figure 15: Touch-Tone™ to 2-of-8 Output Converter

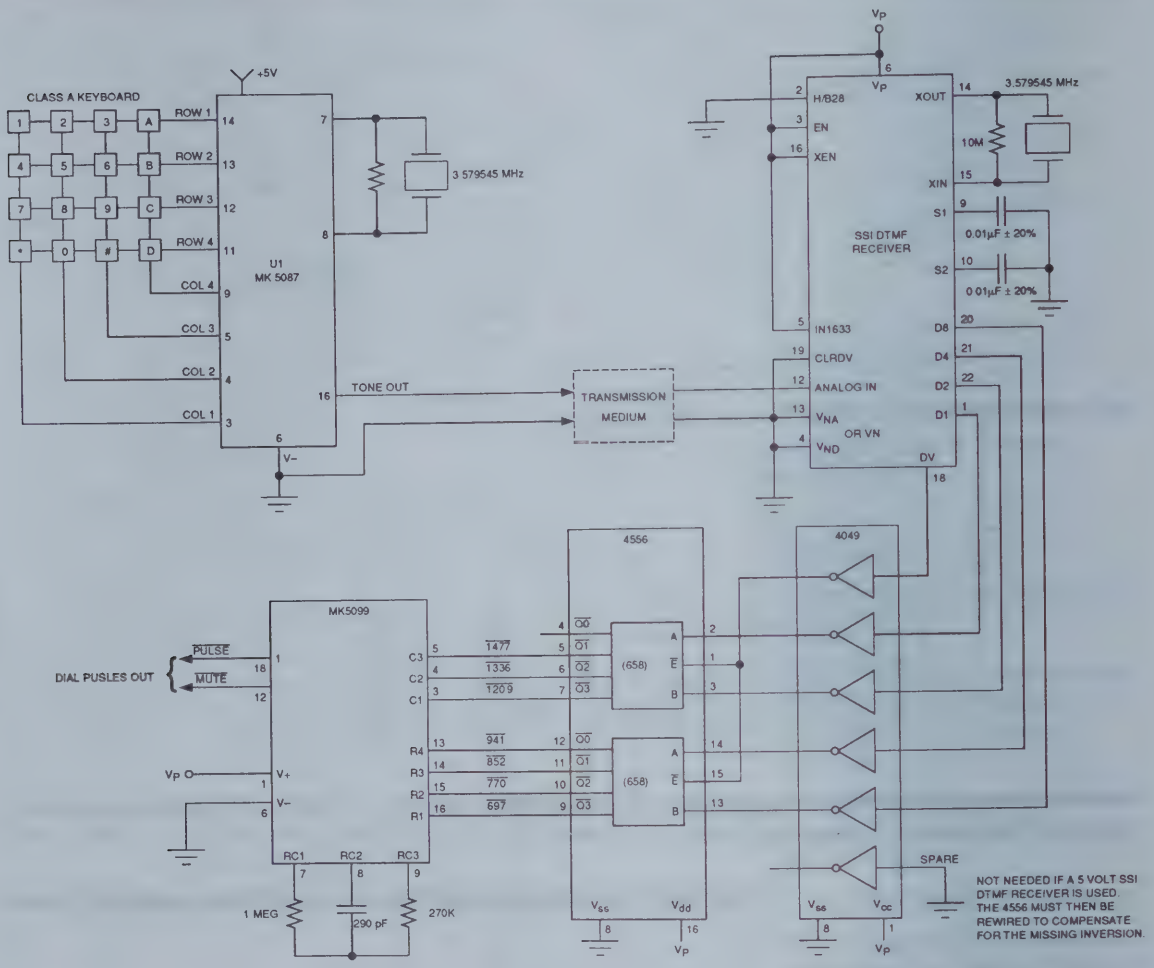


Figure 16: Touch-Tone™ to Rotary Dial Pulse Converter Adding Rotary Dial Pulse Detection Capabilities

DTMF TO ROTARY DIAL PULSE CONVERTER

The 2-of-8 output of Figure 15 can be modified to interface with a pulse dialer as shown in Figure 16. If a 12V DTMF is used the 4049 will translate the 12V outputs to the 5V swings required for the MK5099 pulse dialer.

Figure 17 shows the interface for adding pulse detection and counting to a SSI DTMF Receiver.

The loop detector provides a digital output representing the telephone loop circuit "make" and "break" condition associated with rotary pulse dialing. For the circuit of Figure 17, ground represents a "make" and VP a "break." The loop detector feeds dial pulses to IC-1, a binary counter, and to IC-2A, a re-triggerable "one-shot." When a dial pulse appears the Q1-NOT output of IC-2A immediately goes low, resetting IC-1. The clock input to IC-1 is delayed by R1-C1 so that reset and count input do not overlap. The binary outputs of IC-1 will reflect the pulse count and 0.2 seconds after the last pulse the Q1-NOT output will go high. C3-R3 differentiate this pulse and clock the output latch, IC-3, holding the output pulse until the next digit.

The 0.2 second timeout of IC-2A indicates the end of dial pulsing since even a slow (8 pps) dial would input another pulse every 0.125 seconds. The binary outputs of IC-1 are paralleled with those of the SSI DTMF Receiver

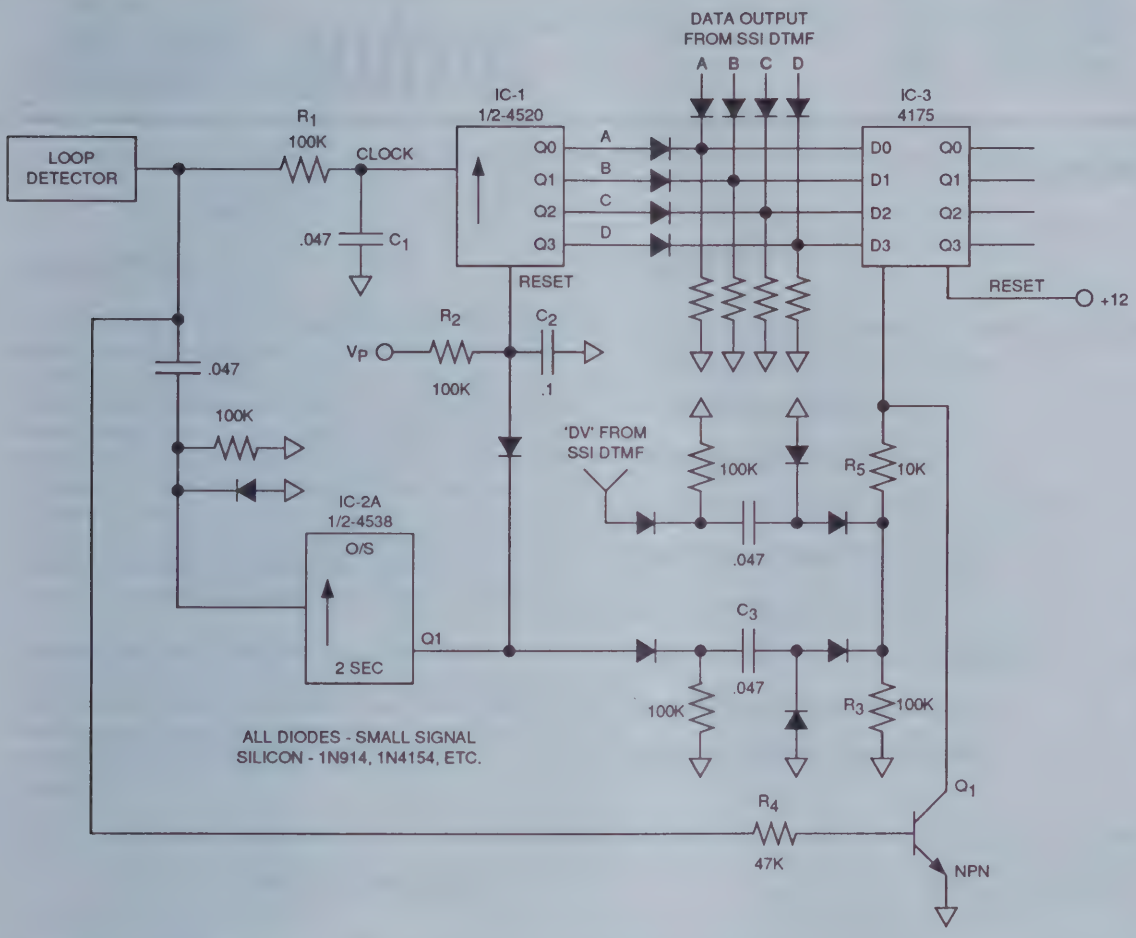


Figure 17: Adding Pulse Detection and Counting to the SSI DTMF Receiver

circuit through diodes to the inputs of IC-3. A pulldown resistor is necessary on each IC-3 input pin. IC-1 must be a binary, not BCD, counter.

With a 4175 for IC-3 the output data is latched until the next valid input, whether from a rotary dial or dual tone instrument. A unique situation exists, however, when going on-hook. The loop detector will output a continuous level of VP which would trigger IC-2A and put a single count into IC-1. A high level from the loop detector also turns on Q1, pulling the clock input of IC-3 to ground. Since the loop detector output will be low at the completion of dialing, all outputs are valid even when the telephone is placed on-hook, an important consideration if output data is recorded.

NOTES:

SSI 75T980
Call Progress Tone Detector

July, 1989

DESCRIPTION

The SSI 75T980 Call Progress Tone Detector circuit allows automatic equipment to monitor tones in dial telephone systems that relate to the routing of calls. Such tones commonly include dial tones, circuits-busy tones, station-busy tones, audible ringing tones and others. By sensing signals in the range of 305 to 640 Hz, the SSI 75T980 does not require the use of precision tones to function. This means that tones which vary with location or call destination can be detected regardless of their exact frequency. The SSI 75T980 is sensitive to signals from 0 dBm to -40 dBm.

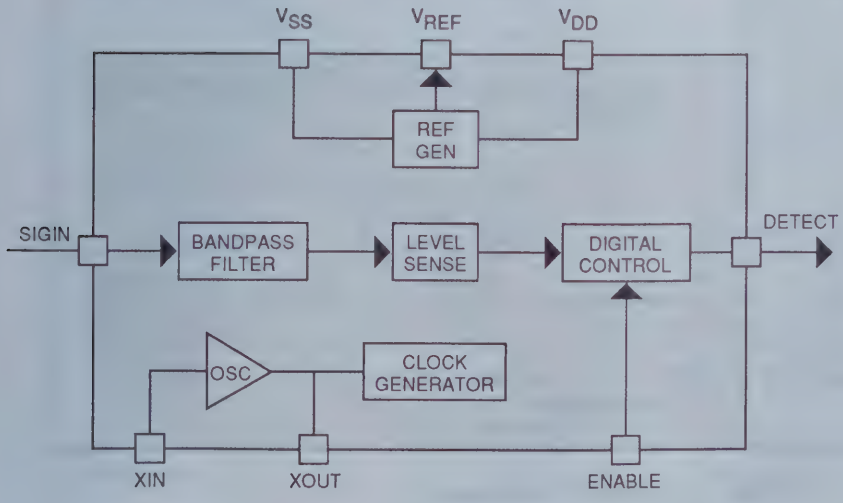
The low power CMOS switched capacitor filters used in the SSI 75T980 derive their accuracy from a 3.58 MHz clock, which in turn may be derived from other devices in the system being designed. The SSI 75T980 is available in a plastic 8-pin DIP and 16-pin SO packages.

FEATURES

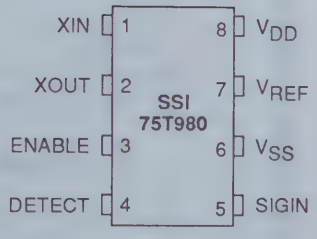
- Detects tones throughout the telephone progress supervision band (305 to 640 Hz)
- Sensitivity to -40 dBm
- Dynamic range over 40 dB
- 40 ms minimum detect (50 ms to output)
- Single supply CMOS (low power)
- Supply range 4.5 to 5.5 VDC
- Uses 3.58 MHz crystal or external clock
- 8-pin DIP and 16-pin SO packages
- Second source of Teltone M-980

4

BLOCK DIAGRAM



PIN DIAGRAMS



8-pin DIP

CAUTION: Use handling procedures necessary for a static sensitive component.

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
SIGIN	I	Accepts analog input signal. See "Electrical Characteristics" for voltage levels, and "Timing Characteristics" for timing.
DETECT	O	Call progress detect output. Goes to logic "1" when signal in 305-460 Hz band is sensed. See "Timing Characteristics."
ENABLE	I	Application of logic "1" on this pin enables the output; logic "0" disables output.
V_{REF}	O	Supplies voltage at half V_{DD} for voltage reference of on-chip op amps.
XIN, XOUT	I	Crystal connections to on-chip oscillator circuit.
V_{DD}	-	Positive power supply connection
V_{SS}	-	Negative power supply connection

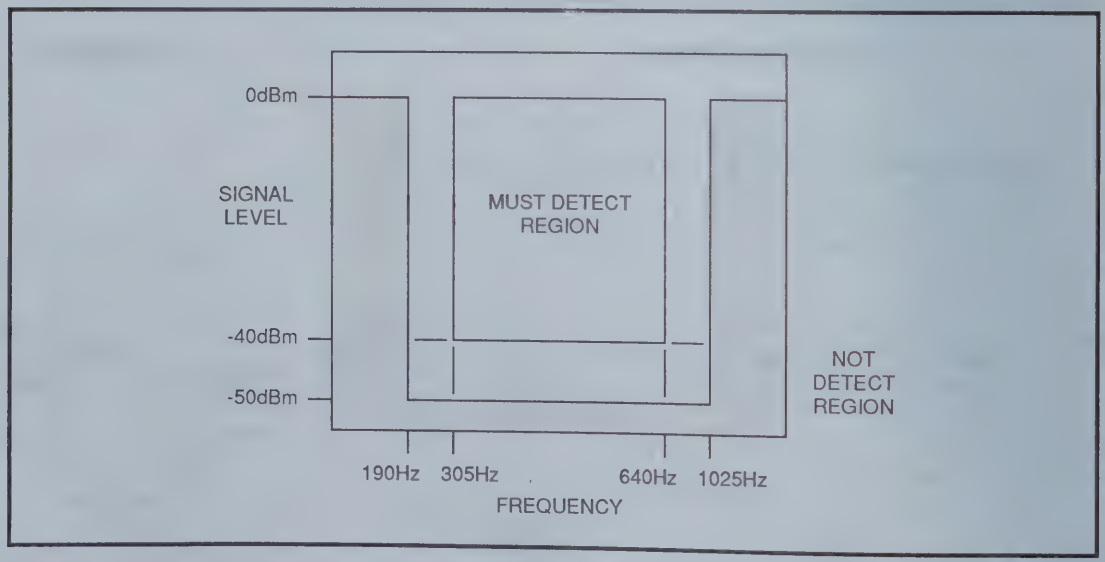


FIGURE 1: Detect and Reject Regions

ABSOLUTE MAXIMUM RATINGS
(Operation above absolute maximum ratings may permanently damage the device.)

PARAMETER	CONDITIONS	RATING
DC Supply Voltage	V_{DD}–Vss	16.0V
Input Voltage	All inputs except SIGNAL IN	(V_{DD} + 0.5V) to (Vss – 0.5V)
SIGNAL IN Voltage		(V_{DD} + 0.5V) to (Vss – 22V)
Storage Temperature		–65°C to 150°C
Operating Temperature		0°C to 70°C
Lead Temperature	Soldering, 5 sec.	260°C

ELECTRICAL CHARACTERISTICS
(Ta = 25°C, V_{DD} – Vss = 4.5V to 5.5V, dBm is referenced to 600Ω)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Supply Current	V_{DD} – Vss = 5V	-	4	10	mA
Signal level for detection	305-640 Hz	–40	-	0	dBm
Signal level for rejection	305-640 Hz	-	-	–50	dBm
	f>1025 Hz, f <190 Hz	-	-	0	dBm
DETECT output (Iout = +1mA)	Logic 0	-	-	0.5	V
	Logic 1	4.5	-	-	V
ENABLE, XIN input (Iin=10μA)	Logic 0	Vss	-	Vss+0.2	V
	Logic 1	V_{DD}–0.2	-	V_{DD}	V
XIN duty cycle		40	-	60	%
XIN, XOUT loading		-	-	10	pF
VREF output	Deviation	–2	(V_{DD}+Vss)/2	+2	%
	Resistance	3.25	-	6.75	kΩ
SIGIN input	Maximum voltage	V_{DD}–10	-	V_{DD}	V
	Impedance (500 Hz)	80	-	-	kΩ

TIMING CHARACTERISTICS
(T_A = 25°C, V_{DD} – V_{SS} = 4.5V to 5.5V)

PARAMETER		CONDITIONS	MIN	MAX	UNITS
t_{MD}	Signal duration for detection	305-640 Hz	40	-	ms
t_{ND}	Signal duration for rejection	305-640 Hz	-	20	ms
	Interval duration for detection	Signal dropping from –40 dBm to –50 dBm (t_2)	40	-	ms
		Signal dropping from 0 dBm to –50dBm (t_1)	90	-	ms
t_D	Detect time		-	50	ms
t_B	Tone dropout bridging		-	20	ms

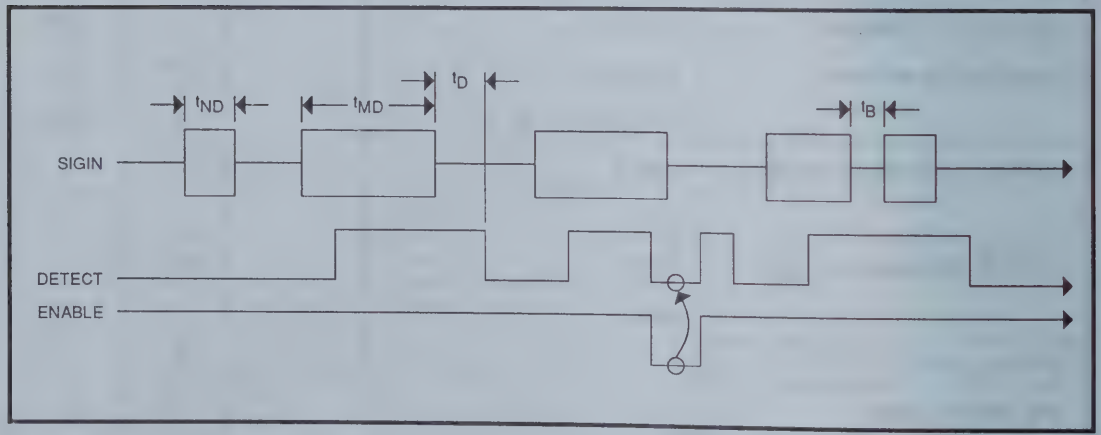


FIGURE 2: Basic Timing

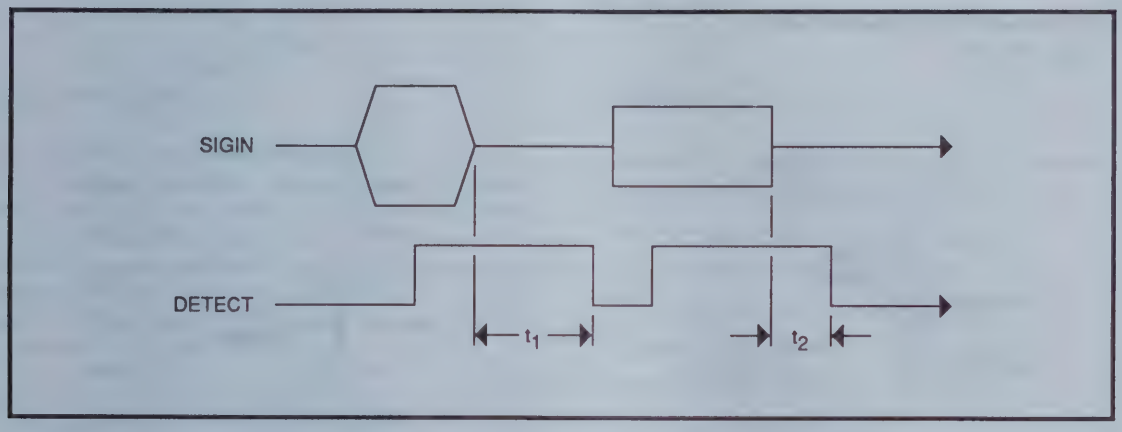


FIGURE 3: Effect of Amplitude on Timing

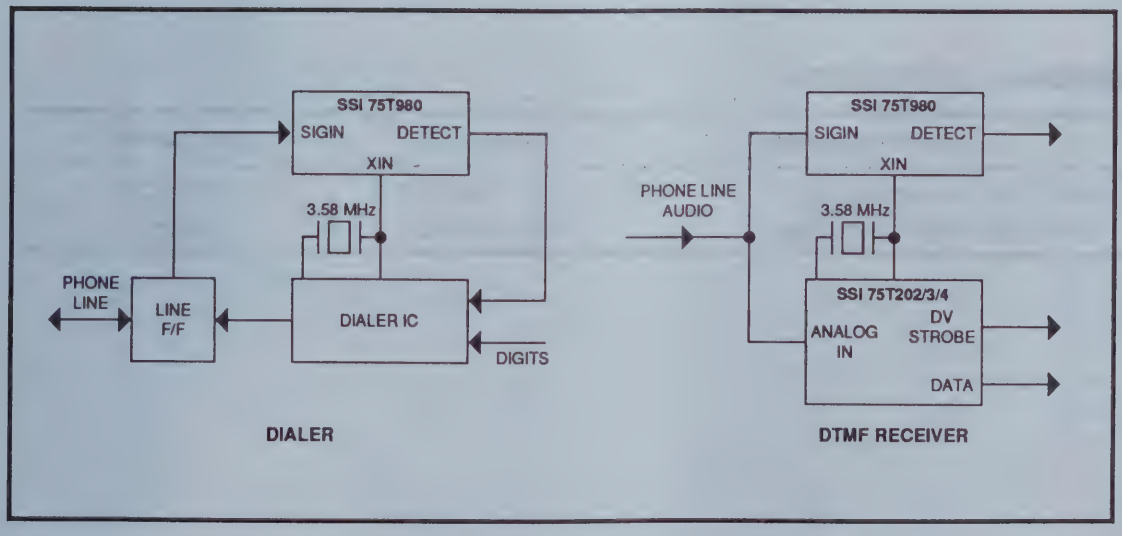
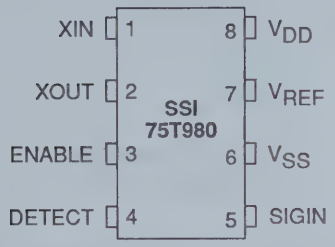


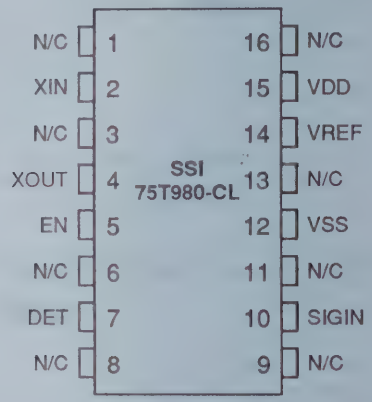
FIGURE 4: Applications Circuits

SSI 75T980
Call Progress
Tone Detector

PACKAGE PIN DESIGNATIONS
(TOP VIEW)



8-PIN DIP



16-PIN SO

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 75T980 8-pin Plastic DIP	SSI 75T980-CP	75T980-CP
SSI 75T980 16-pin SO Package	SSI 75T980-CL	75T980C

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SSI 75T981/982
Precise Call Progress Tone Detector

May, 1989

DESCRIPTION

The SSI 75T981 and SSI 75T982 Precise Call Progress Tone Detector circuits enable automatic monitoring of tones in dial telephone systems for the purpose of routing calls. Built using CMOS switched capacitor technology, each has four independent channels for detecting precise tones in the 305 to 640 Hz range. The outputs of the channels have a response related to the respective tone durations.

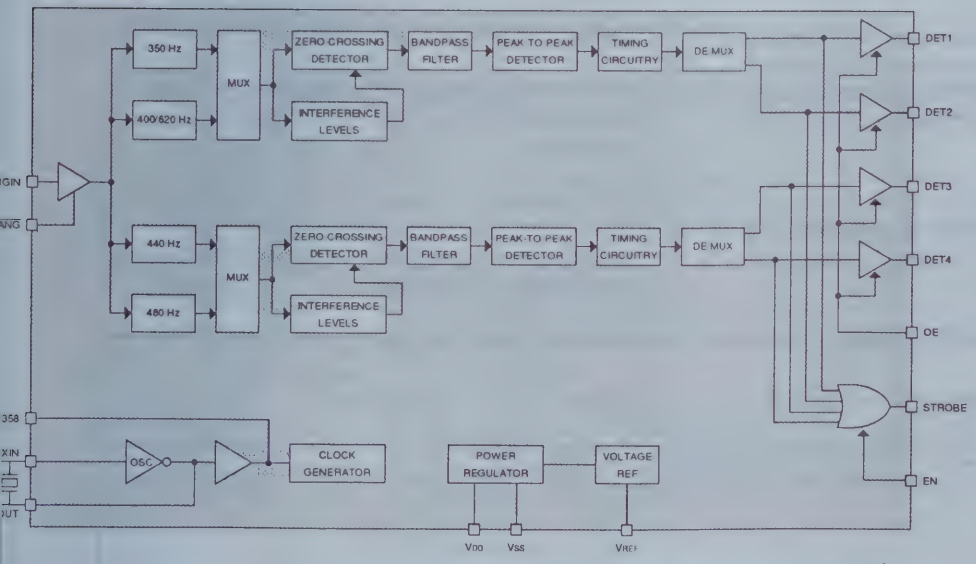
The SSI 75T981 and SSI 75T982 are identical except for the tones detected. The SSI 75T981 will decode 350Hz, 400Hz, 440Hz and 480Hz. The SSI 75T982 will decode 350Hz, 440Hz, 480Hz and 620Hz tones.

FEATURES

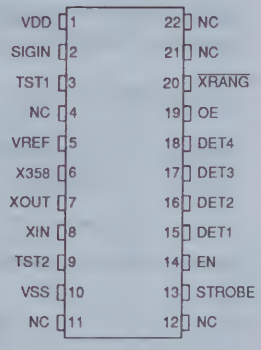
- Detects & decodes precise tones throughout 305-640Hz telephone progress band
- 35dB dynamic range
- Single supply CMOS (low power)
- Adjustable gain sensitivity
- Supply range 4.75 to 5.5 VDC
- Uses 3.58 MHz crystal
- Three-state outputs
- Standard 22-pin DIP
- Second source to Teltone M981 and M982

4

BLOCK DIAGRAM



PIN DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

CIRCUIT OPERATION

The functional block diagram is shown on page 1. Channels 1 and 2, and 3 and 4 are multiplexed, respectively as shown. Each channel starts with a 4-pole band-pass filter that reduces the amplitude of the out-of-band signals. The output of the front-end filter is fed into two circuits, one being a zero-crossing detector which functions as a limiter-AGC, and the other being a circuit that controls the level of the interference floor based on the level of the incoming signal. The output of the ZCD, and energy-limited signal, is fed into a peak-to-peak detector that determines if the precise frequency is present by checking the amplitude of the signal from the back-end filter. Pulses from the peak-to-peak detector, which indicate the presence of the precise tone, are counted to time the duration of the input pulsed-tone. If the criteria of the specifications are met, the appropiate detect output goes to the high state. As shown in the block diagram, all circuitry after the front-end filters is multiplexed. A digital demultiplexer follows the P-P detector to provide the four distinct outputs.

SIGIN

The input signal is applied to the SIGIN pin and is AC-coupled into the front-end filters. The SSI 75T981 and SSI 75T982 can amplify a low level signal by 10dB when the $\overline{\text{XRANG}}$ pin is held low.

DET OUTPUTS & OE

Outputs DET1-4 are CMOS push-pull when enabled (OE="1") and high impedance when disabled (OE="0"). A "1" on a DET pin indicates that the appropriate valid tone pulse was detected (see Table 1). Detect timing is shown in Figure 1.

STROBE & EN

The STROBE pin is the logical OR of the DETn outputs and will indicate when any one of the four call progress tones has been detected. STROBE is unaffected by OE but goes to a high impedance state when EN="0".

XIN, XOUT & X358

Internal timing and clocks are derived form the 3.58 MHz clock. The SSI 75T981 and SSI 75T982 contain an on-board inverter with sufficient gain to provide oscillation when connected to a low cost "colorburst" crystal. The crystal is connected between XIN and XOUT . A 1MΩ 10% resistor is also connected between these pins. In this mode, X358 is a clock frequency output available to drive other parts requiring the same frequency.

The part will also operate with an external digital clock (duty cycle 40% to 60%).

VREF

Internal analog signal reference voltage. Noise or interference coupled onto this pin may degrade chip functionality.

TST1 & TST2

Manufacturer's special test pins. These pins should be left floating, not grounded.

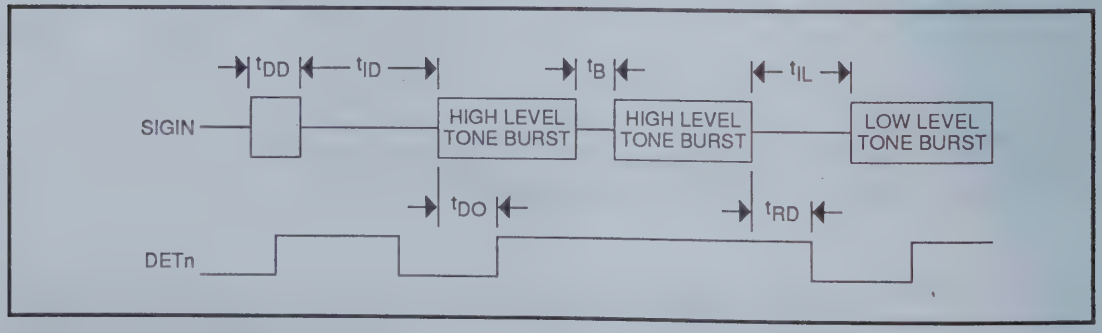


FIGURE 1: TIMING DIAGRAM

TIMING CHARACTERISTICS
(T_A = 25°C, V_{DD}-V_{SS} = 4.75V to 5.5V)

PARAMETER		CONDITIONS	MIN	MAX	UNITS
t_{DD}	Signal Duration for Detection	In band, see Electrical Char.	200	-	ms
t_{DO}	Time to Output	In band, see Electrical Char.	-	200	ms
t_B	Bridge Time	In band, see Electrical Char.	-	30	ms
t_{ID}	Signal Duration for Rejection	Noise at SIGIN: –50 dBm, 0.2-3.4 kHz	-	160	ms
t_{RD}	Time to Release	Noise at SIGIN: –50 dBm, 0.2-3.4 kHz	-	200	ms
t_{IL}	Interval Duration for Detection of Both Signals	High to Low; High = 0 dBm, Low = –25 dBm	1	-	s
t_{EN}	DETn Pin Enable Time, Z to Low or High	C_L = 50 pF, R_L = 100 kΩ	-	450	ns
t_{DS}	DETn pin Disable Time, Low or High to Z	C_L = 50 pF, R_L = 100 kΩ	-	450	ns

4

TABLE 1: FREQUENCY DETECTION

SIGNAL PRESENT (fo)		DET1	DET2	DET3	DET4	OE	STROBE	EN
75T981	75T982							
350Hz	350Hz	1	X	X	X	1	1	1
400Hz	620Hz	X	1	X	X	1	1	1
440Hz	440Hz	X	X	1	X	1	1	1
480Hz	480Hz	X	X	X	1	1	1	1
Other In-Band		0	0	0	0	1	0	1
Any		High Impedance				0	0	0

Note: Out-of-band tones may cause short detect pulses if at sufficient amplitude and pulsed duration.

ELECTRICAL CHARACTERISTICS
($0°C \leq T_A \leq 70°C$)

PARAMETER	CONDITIONS	MIN	MAX	UNITS
VDD		4.75	5.5	V
Oscillator Frequency Deviation	At XOUT from 3.57959 MHz	–0.01	+0.01	%
Power Supply Noise	0.1–5 KHz	-	20	mVp-p
Current Drain	VDD=5.5V, TA=0°C	-	30	mA
Must Detect Signal				
Frequency Range		–1.0	+1.0	% of fo
Level (See Note 2)	$\overline{XRANG}$=0; In-Band, see Table 1	–35	–10	dBm
	$\overline{XRANG}$=1; In-Band, see Table 1	–25	0	dBm
Must Reject Signal Level	$\overline{XRANG}$=0; Noise at SIGIN: –50dBm, 0.2–3.4 KHz	-	–60	dBm
	$\overline{XRANG}$=1; Noise at SIGIN: –50dBm, 0.2–3.4 KHz	-	–50	dBm
Level Skew Between Adjacent In-Band Signals for Detection of both	See Note 4	-	6	dB
Steady State Response Must Detect Level	fo–5% > f > fo+5%, See Note 3, See Timing Characteristics	-	0	dBm
SIGIN Pin				
Voltage Range		VDD–10	VDD	V
Input Impedance	Resistance; f=500 Hz	80	-	KΩ
	Capacitance	-	15	pF
Gain	$\overline{XRANG}$=0	9.9	10.1	dB
$\overline{XRANG}$ Pin				
VIL		-	0.5	V
VIH		VDD–2.0	-	V
Pullup Current	$\overline{XRANG}$=VSS	-	–10	µA
Detect Pins, DETn				
VOL	ISINK = –1mA	-	0.5	V
VOH	ISOURCE = 1mA	VDD–0.5	-	V
IOZ	VO = VDD, VSS	-	±1	µA

ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	CONDITIONS	MIN	MAX	UNITS
STROBE Pin				
VOL	ISINK = –1mA	-	0.5	V
VOH	ISOURCE = 1mA	VDD–0.5	-	V
OE, EN Pins				
VIL		-	0.5	V
VIH		VDD–2.0	-	V
Pullup Current	OE, EN = VSS	-	–10	µA
External Clock				
VIL	XOUT Open	-	0.2	V
VIH	XOUT Open	VDD–0.2	-	V
Duty Cycle	XOUT Open	40	60	%
XIN, XOUT Loading				
Capacitance	Crystal oscillator active	-	10	pF
Resistance	Crystal oscillator active	20	-	MΩ
X358 Pin (CL = 20pF)				
VOL	ISINK = –10µA	-	0.2	V
VOH	ISOURCE = 10µA	VDD–0.2	-	V
Duty Cycle		40	60	%

Notes:

1. All parameters are specified at VDD=5 volts and $\overline{\text{XRANG}}$ at a logical "high" state, which implies unity front-end gain. Power levels in dBm are referenced to 600Ω.

2. A post-filter AGC is employed to enhance end-of-tone detection for high-level signals. A drop in amplitude of the input tone may cause an end-of-tone (interval) indication.

3. Large input voltage transients may cause excessive ringing in the highly selective filter, causing spurious detection. The detects are not considered as incorrect circuit operation.

4. Any tone 40Hz – 1% from fo must adhere to this specification, where fo is defined in Table 1.

ABSOLUTE MAXIMUM RATINGS
(Operation above absolute maximum ratings may damage the device.)

PARAMETER	CONDITIONS	RATING
DC Supply Voltage	V_{DD} – Vss	+7V
Input Voltage	All inputs except SIGIN	Vss – 0.3V to V_{DD} + 0.3V
SIGIN Voltage		V_{DD} – 18V to V_{DD} + 0.3V
Storage Temperature		–65°C to 150°C
Operating Temperature		0°C to 70°C
Lead Temperature	Soldering, 10 sec.	260°C

NORMAL CALL PROGRESS TONES AND SEQUENCE (Refer to Figure 2.)

TONE	FREQUENCY (Hz)	CADENCE
Precision Dial Tone	350 + 440	Continuous
Old Dial Tones	600 + 120 or 133 and other combinations	Continuous
Precision Busy	480 +620	0.5 s on 0.5 s off
Old Busy	600 +120	0.5 s on 0.5 s off
Precision Reorder	480 +620	0.3 s on local 0.2 s off reorder
Old Reorder	600 +120	0.2 s on toll 0.3 s off reorder 0.25 s on toll 0.25 s off local
Precision Audible Ringback	440 +480	2 s on 4 s off
Old Audible Ringback	420 +40 and other combinations	2 s on 4 s off

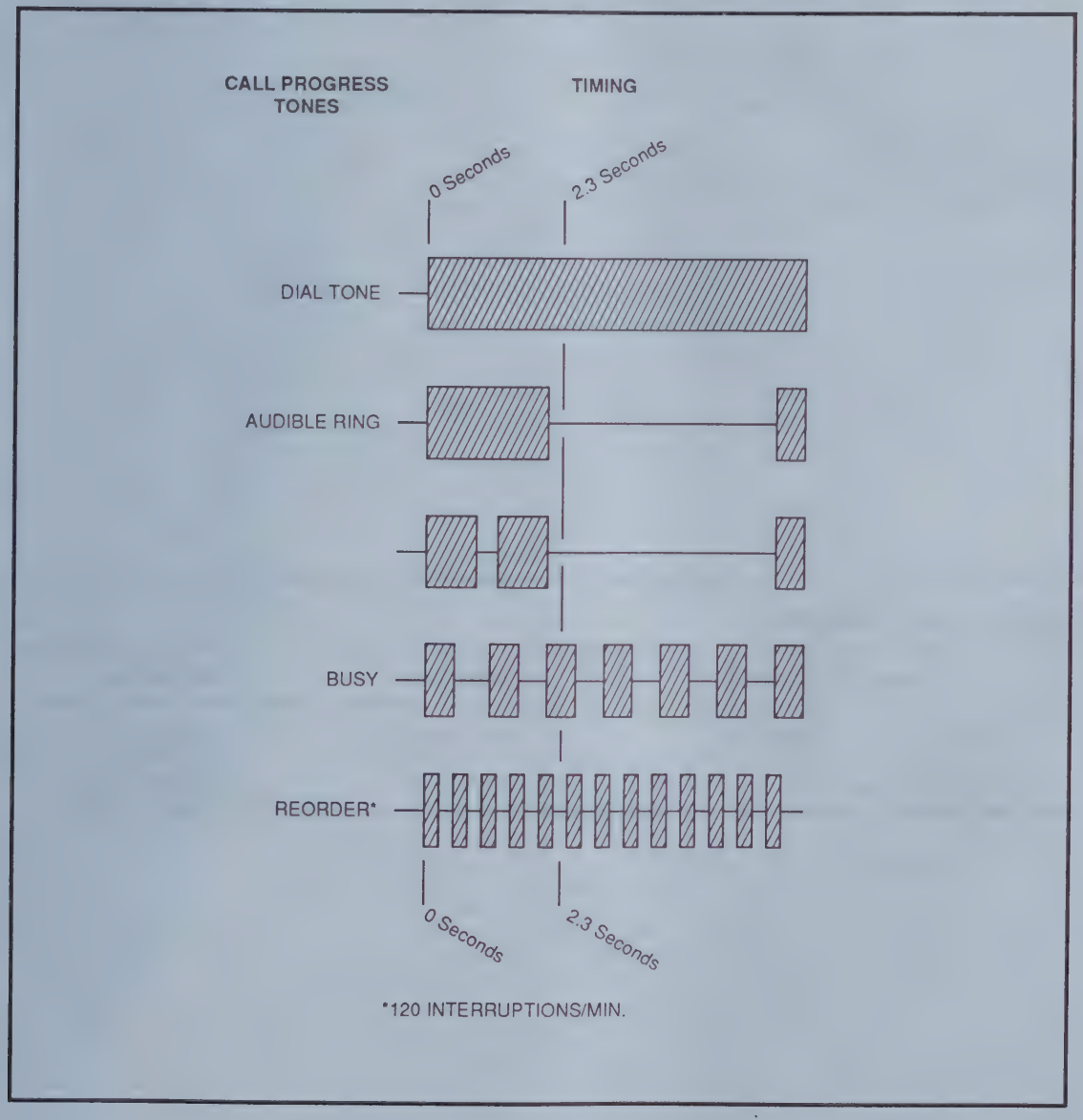
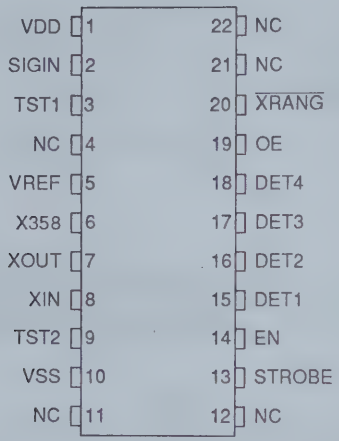


FIGURE 2: NORMAL CALL PROGRESS TONES AND SEQUENCE

SSI 75T981/982
Precise Call Progress Tone Detector

PACKAGE PIN DESIGNATIONS
(TOP VIEW)



22 - PIN DIP

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 75T981 22-Pin Plastic DIP	SSI 75T981-CP	75T981-CP
SSI 75T982 22-Pin Plastic DIP	SSI 75T982-CP	75T982-CP

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Section 5

TELEPHONY/ DIGITAL TELECOM

TELEPHONY INTEGRATED CIRCUITS SELECTOR GUIDE

TELEPHONY IC SELECTION CHART						
APPLICATIONS	PRODUCTS	CENTRAL OFFICE		CUSTOMER PREMISES		PRODUCT DESCRIPTION
MARKETS SERVED	SSI DEVICE NUMBER	SUBSCRIBER NETWORK	C.O. INTERCONNECT EQUIPMENT	PUBLIC NETWORK	PRIVATE NETWORK	
T1/ISDN PRIMARY RATE APPLICATIONS • Channel Banks • Digital Cross-connects • Channel Service Units	78P233					T1/Primary Rate Line Interface
CEPT/ISDN PRIMARY RATE APPLICATIONS • PBX's • Multiplexers	78P234					CEPT/ Primary Rate Line Interface
ANALOG TONE SIGNALING APPLICATIONS	75T201					12V DTMF Receiver
• Central Office Switches • PBX's	75T202					5V DTMF Receiver
• Auto-Dialers • Test Equipment	75T203					DTMF Receiver with Early Detect
	75T981 & 2					Precise Call Progress Detect
• Toll Call Signaling	78A207					MFR1 Receiver
• Maintenance Terminating Units	78A400					2713 Hz Detect, 4-Wire Loopback
•Leased Line Diagnostics	78A420					Loopback with Gain Block
CONSUMER APPLICATIONS	75T204					Low-Cost DTMFReceiver
• Telephone Answering Machines	75T957					DTMF Rcvr. with Dial Tone Reject
• Pay Telephones • Modems • Security Systems	75T2089					DTMF Transceiver
	75T2090					DTMF Xcvr. with Call Progress
	75T2091					DTMF Xcvr. w/CPD Early Detect
• Business Phone Systems	75T980					Call Progress Detect
• Analog Matrix Switching	78A093					12 x 8 Analog Crosspoint Switch

SSI 78A093A/B
CMOS 12x8x1 Crosspoint Switch With Control Memory

June, 1989

DESCRIPTION

The SSI 78A093 is a 12x8 matrix-array crosspoint-switching IC for telecom-switching and industrial control-routing applications. Standard integrated features include microprocessor-control inputs, line decoder, address latches, and 6 Vp-p analog-signal capability. The product is available with two different power supply configurations: The SSI 78A093A accepts power through the VSS and VDD pins; the SSI 78A093B has an altered pin-out and offers a separate logic ground pin. Both versions offer excellent crosstalk immunity, low feedthrough (–95dB at 1KHz), extra-high isolation between any two switches connected to X0 channel, and less than 1% total distortion at 0 dBm. The X0 channel is optimized for "ON HOLD" use by providing high isolation between switches connected to X0. The SSI 78A093 employs CMOS design technology for low-power operation. Power requirement for both the A and B versions of the SSI 78A093 is 5 to 16 volts. Both versions are packaged in a standard 40-pin plastic DIP or 44-pin PLCC.

FEATURES

- 96 crosspoint switches in a 12x8 array
- µP-compatible control inputs
- On-chip line demultiplexer
- Low ON resistance: 28 ohms at VDD = 12V typical
- 5 to 16-volt supply operating range
- 6 Vp-p analog signal capability
- Address latches on-chip
- Optimized performance on X0 channel
- Less than 1% total distortion at 0 dBm
- -95 dB feedthrough at 1KHz
- Extra-low crosstalk between any two switches connected to X0
- 78A093B version offers separate logic ground for flexible system design
- Low-power CMOS design
- TTL or CMOS-compatible inputs
- 40-pin plastic DIP or 44-pin PLCC

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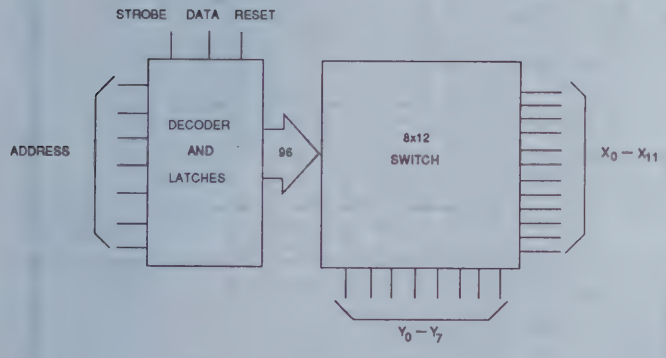
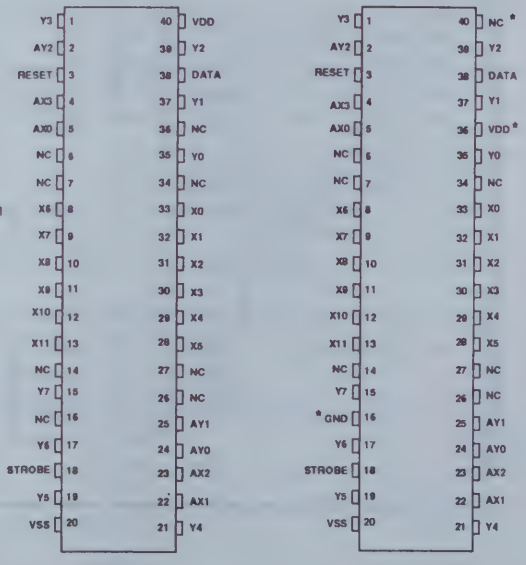
BLOCK DIAGRAM



PIN DIAGRAM



NOTE: Please see last page for PLCC pinout.

* different pins relative to 78A093A

CAUTION: Use handling procedures necessary for a static sensitive component.

SSI 78A093A/B
CMOS 12x8x1
Crosspoint Switch
With Control Memory

FUNCTIONAL DESCRIPTION

A functional block diagram of the device is presented in Figure 1. The IC contains a 12x8 matrix of analog switches, each with a latch to maintain its on (closed) or off (open) state. Seven ADDRESS lines, AX0-AX3 and AY0-AY2, are provided to address any one of the 96 switches. The DATA line may be held high to turn the switch on, or low to turn it off. The state of the ADDRESS and DATA lines can be set concurrently or separately. Finally, a positive pulse to the STROBE line initiates the action determined by the ADDRESS and DATA lines. All 96 switches may be turned off by forcing the RESET line high. All control lines (ADDRESS, DATA, STROBE, and RESET) are level sensitive.

The IC has two power supply configurations: the A-version has VDD and VSS power supply pins; the B-version has VDD, VSS and a GND pin. The GND pin is provided as a reference voltage for digital inputs. For proper operation, the positive supply must be at least 4.5 volts above GND.

The switches are designed to provide low resistance connections when turned on. Any Y switches connecting to the X0 channel are optimized to provide lower ON resistance. Furthermore, the X0 channel switches, when turned on, provide maximized isolation between the Y channels when X0 is grounded or connected to a low impedance source.

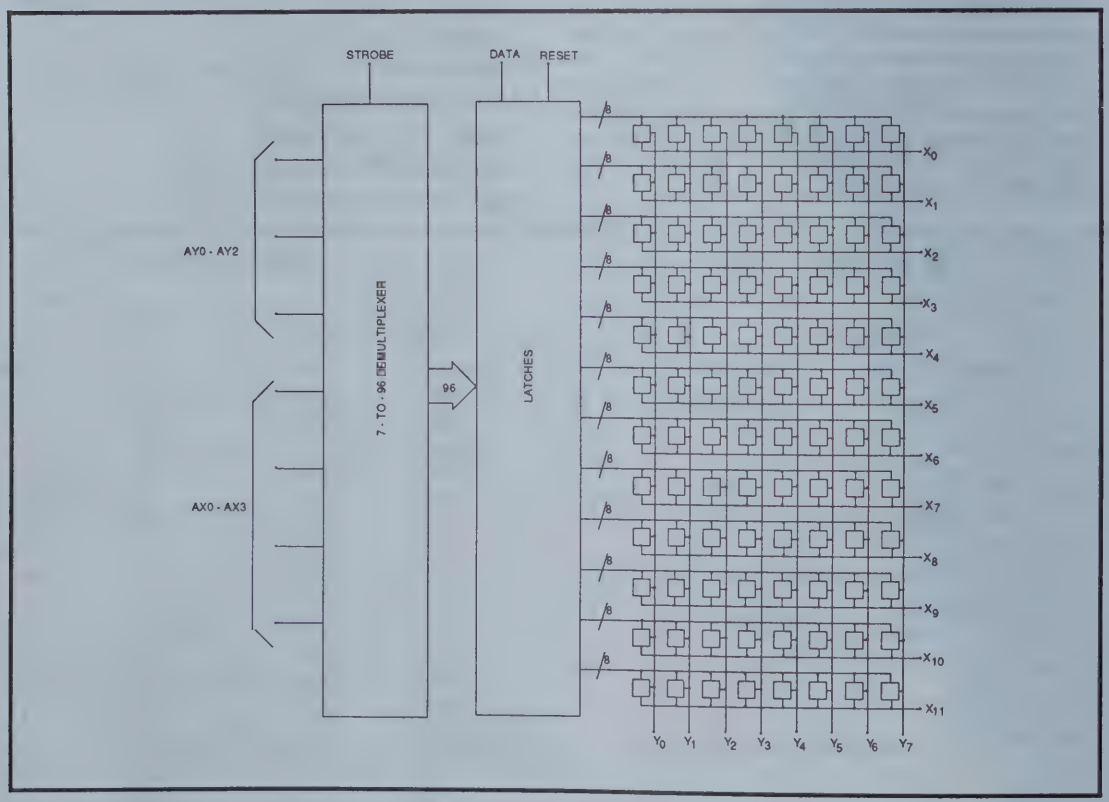


FIGURE: 1

PIN DESCRIPTION

NAME	A-PIN # (DIP)	B-PIN # (DIP)	TYPE	DESCRIPTION
POWER				
VDD	40	36	I	Positive power supply.
VSS	20	20	I	Negative power supply.
GND	-	16	I	Digital signal ground.
ADDRESS				
AX0-AX3	4, 5, 22, 23		I	X address lines. These 4 pins are used to select one of the 12 rows of switches. Refer to the truth table in figure 2, for legal addresses.
AY0-AY2	2, 24, 25		I	Y address lines. These 3 pins are used to select one of the 8 columns of switches. Refer to the truth table in figure 2, for legal addresses.
CONTROL				
DATA	38		I	This input determines if the selected switch will be turned on (closed) or off (opened). If the pin is held high, the selected switch will be closed. If the pin is held low, the switch will be opened.
STROBE	18		I	This pin enables whatever action is selected by the address and DATA pins. When the STROBE pin is held low, no switch openings or closing take place. When the STROBE pin is held high, the switch addressed by the select lines will be opened or closed (depending upon the state of the DATA pin).
RESET	3		I	Master Reset. This pin turns off (opens) all 96 switches. The states of the above control lines are irrelevant. This pin is active high.
DATA				
X0-X11	8-13, 28-33		I/O	Analog Input/Outputs. These pins are connected to the rows of the switch matrix.
Y0-Y7	1, 15, 17, 19, 21, 35, 37, 39		I/O	Analog Input/Outputs. These pins are connected to the columns of the switch matrix.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Exposure to absolute maximum rating conditions for extended periods may cause permanent damage to the device or affect device reliability.

PARAMETER	RATING	UNIT
VDD with respect to VSS	-0.5 to 17.6	V
GND (B-Version only)	VSS -0.5 to VDD +0.5	V
Storage Temperature	-65 to 150	°C
Control Signals	GND -0.5 to VDD +0.5	V
Analog Signals	7	Vpp
Lead Temperature (soldering, 10 seconds)	300	°C

Address							Connections
AX0	AX1	AX2	AX3	AY0	AY1	AY2	
0	0	0	0	0	0	0	X0 - Y0
1	0	0	0	0	0	0	X1 - Y0
0	1	0	0	0	0	0	X2 - Y0
1	1	0	0	0	0	0	X3 - Y0
0	0	1	0	0	0	0	X4 - Y0
1	0	1	0	0	0	0	X5 - Y0
0	1	1	0	0	0	0	no connection
1	1	1	0	0	0	0	no connection
0	0	0	1	0	0	0	X6 - Y0
1	0	0	1	0	0	0	X7 - Y0
0	1	0	1	0	0	0	X8 - Y0
1	1	0	1	0	0	0	X9 - Y0
0	0	1	1	0	0	0	X10 - Y0
1	0	1	1	0	0	0	X11 - Y0
0	1	1	1	0	0	0	no connection
1	1	1	1	0	0	0	no connection
0	0	0	0	1	0	0	X0 - Y1
↓	↓	↓	↓	↓	↓	↓	↓ ↓
1	0	1	1	1	0	0	X11- Y1
0	0	0	0	0	1	0	X0 - Y2
↓	↓	↓	↓	↓	↓	↓	↓ ↓
1	0	1	1	0	1	0	X11- Y2
0	0	0	0	1	1	0	X0 - Y3
↓	↓	↓	↓	↓	↓	↓	↓ ↓
1	0	1	1	1	1	0	X11- Y3
0	0	0	0	0	0	1	X0 - Y4
↓	↓	↓	↓	↓	↓	↓	↓ ↓
1	0	1	1	0	0	1	X11- Y4
0	0	0	0	1	0	1	X0 - Y5
↓	↓	↓	↓	↓	↓	↓	↓ ↓
1	0	1	1	1	0	1	X11- Y5
0	0	0	0	0	1	1	X0 - Y6
↓	↓	↓	↓	↓	↓	↓	↓ ↓
1	0	1	1	0	1	1	X11- Y6
0	0	0	0	1	1	1	X0 - Y7
↓	↓	↓	↓	↓	↓	↓	↓ ↓
1	0	1	1	1	1	1	X11- Y7

address not allowed

FIGURE 2: Truth Table

RECOMMENDED OPERATING CONDITIONS

The recommended operating conditions for the device are indicated in the table below. Performance specifications do not apply when the device is operated outside these limits.

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNIT
VDD with respect to VSS		4.5		16.0	V
VDD with respect to GND		4.5		16.0	V
GND with respect to VSS		0		5.5	V
Analog Input Voltages VIN				6	Vpp
Analog Currents				10	mA
Ambient Temperature		0		85	°C

D.C. CHARACTERISTICS

TA = 25°C, VSS = 0V, GND = 0, VDD = 4.5V or 13.2V, RL = 1K, CL = 50pF, UNLESS OTHERWISE NOTED. Positive current is defined as flowing into the device.

PARAMETERS		CONDITIONS	MIN	NOM	MAX	UNIT
Supply Current IDD				14	20	mA
CROSSPOINT						
ON resistance	X0 channel (X0-Yj)	VIN ≤ 6Vp-p		20		Ω
RON	other channels (Xi-Yj)	VIN ≤ 6 Vp-p		28	45	Ω
ON resistance var.	X0 channel (X0-Yj)			5		Ω
Δ RON	other channels (Xi-Yj)			15	25	Ω
X capacitance	CX	(Switch off)			20	pF
Y capacitance	CY	(Switch off)			30	pF
CONTROL						
Input HIGH voltage	VIH	A-Version B-Version	2.0 GND +2.0			V V
Input LOW voltage	VIL	A-Version B-Version			0.8 GND +0.8	V V
Input leakage	IL		-0.1		0.1	µA

DYNAMIC CHARACTERISTICS AND TIMING

TA = 25°C, VDD = 4.5V or 13.2V, VSS = 0V, GND = 0V, RL = 1K, CL = 50 pF, UNLESS OTHERWISE NOTED. Digital input rise and fall times are 5nS. Output times are defined as the time to rise or fall from 0% to 10% of the full swing (see figure 3).

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNIT
CROSSPOINT					
Propagation Delay	1 Vp-p sine wave @ 10KHz		18	30	ns
Distortion	1 Vp-p sine wave		0.2	1.0	%
Feedthrough	10 KHz, any switch off		-90	-80	dB
Yi to Yj isolation on X0 channel	Any two Y channels: Yi, Yj, X0-Yi, X0-Yj are on Xo grounded, Rin = 1K		-90	-60	dB
Crosstalk	1Vp-p sine wave 1KHz		-97		dB
	1Vp-p sine wave 10KHz		-92		
CONTROL					
Delay: strobe to out TSZ			60	160	ns
Delay: address to out TAZ				200	ns
Delay: data to out TDZ				180	ns
Delay: reset to out TRZ			100	180	ns
Data setup time TSU			30		ns
Address setup time TAS			30		ns
Data hold time TH			30		ns
Address hold time TAH			30		ns
Strobe Pulse Width TST			50		ns
Reset Pulse Width TRST			50		ns

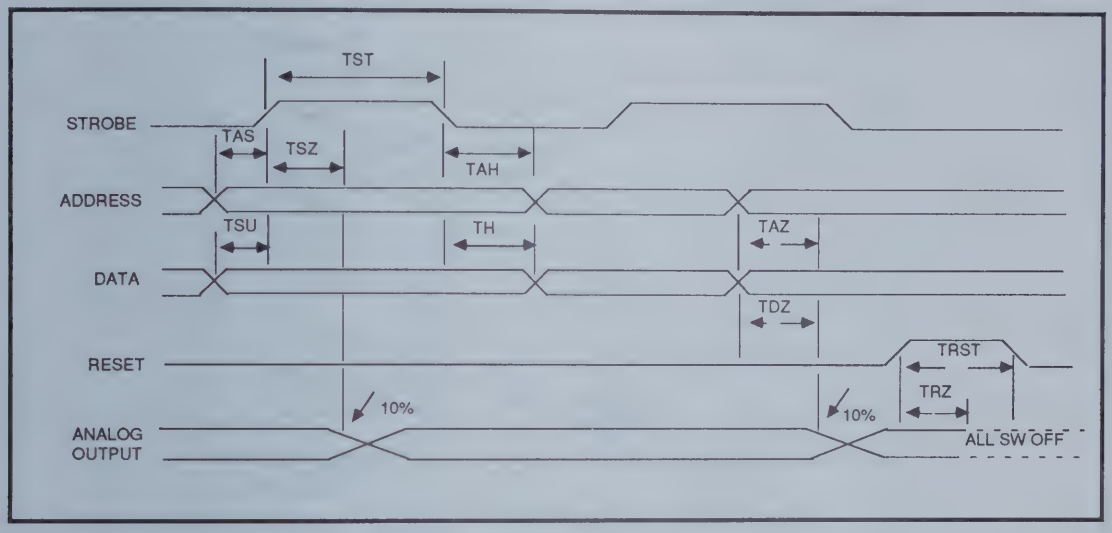


FIGURE 3: Timing Diagram

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APPLICATIONS INFORMATION

Although the SSI 78A093 allows switching 96 possible signal paths, it is not limited to applications of only an 8x12x1 configuration. Figure 4 shows a method of addressing 4 separate 78A093's. In this example, the RESET, DATA, and ADDRESS lines are connected in parallel for the four devices. The logic for lines A, B and STROBE go to a 2-line to 4-line decoder with the STROBE used to both enable and clock the data. This decode (or a wider one) could be easily implemented with a single programmable logic device.

Figure 5 shows a case where both the X and Y lines have been expanded. This may be useful for applications where several different source/destination paths need to be controlled by a single controller. The A and B lines are decoded to select the desired device.

In Figure 6, the Y-lines of all devices are connected in parallel to allow an 8x48x1 switch configuration. The A and B inputs become in effect an extension of the X-address line. This could also be used to make a 32x12x1 matrix by tying the X-lines in parallel with the A and B inputs used as Y-address lines.

Figure 7 shows an application where switches in 2 devices are connected at the same time in a 12x8x2 matrix. This would be useful in applications requiring the switching of differential signals.

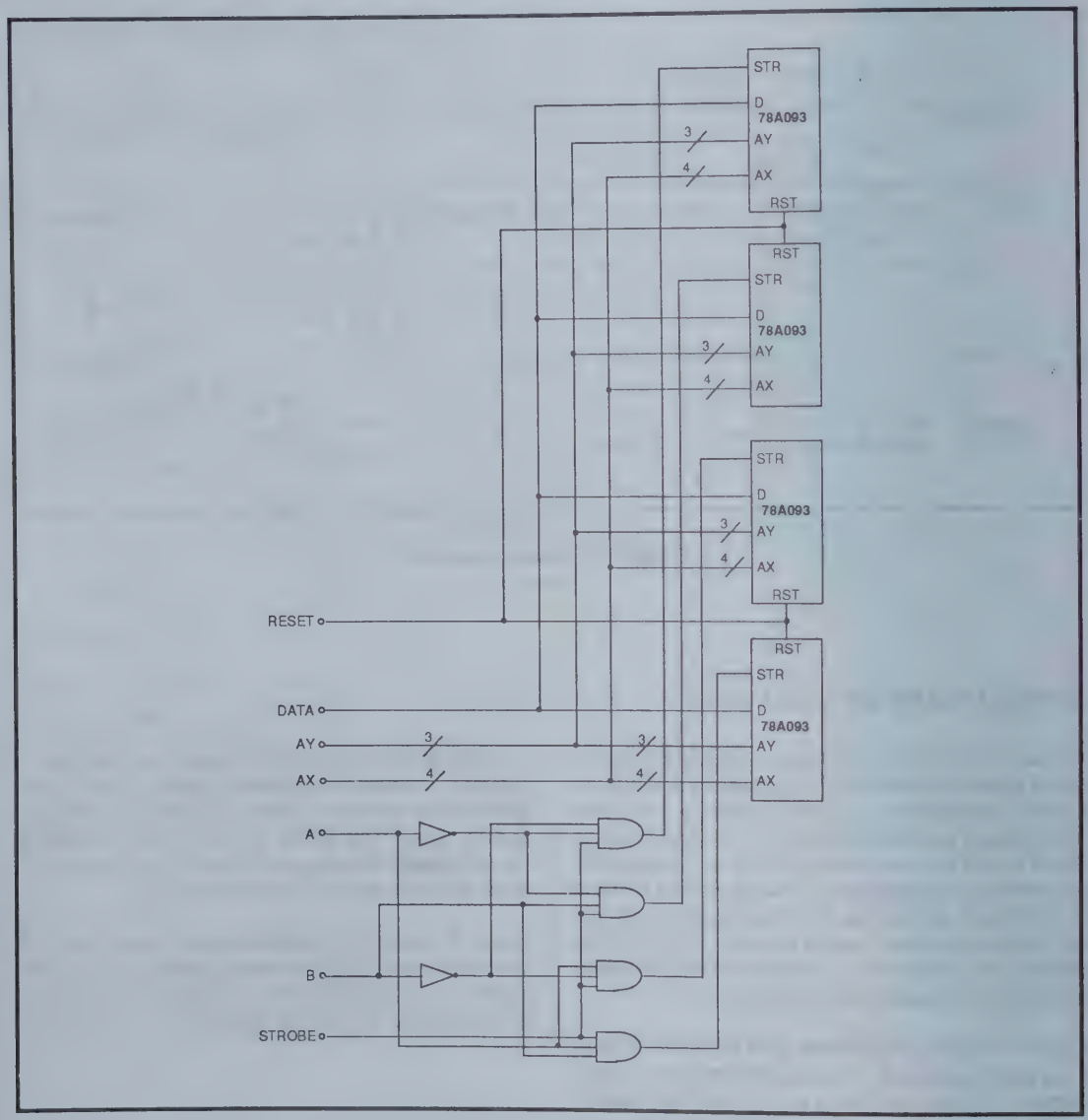


FIGURE 4

FIGURE 5

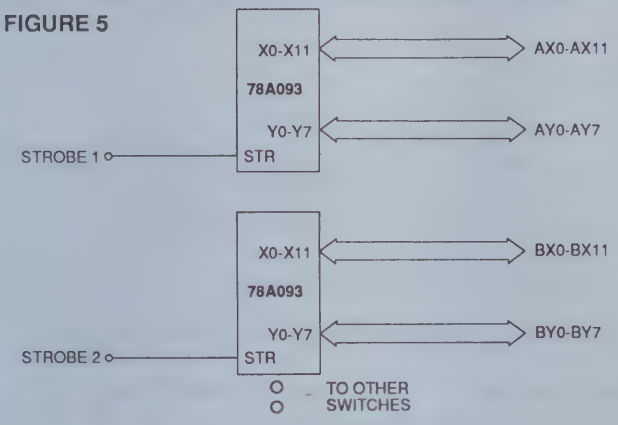


FIGURE 6

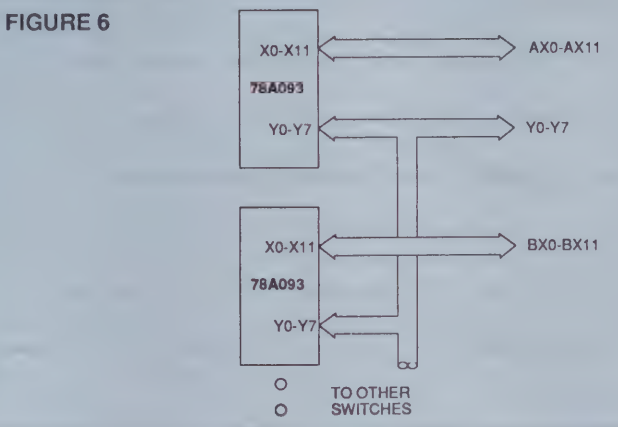
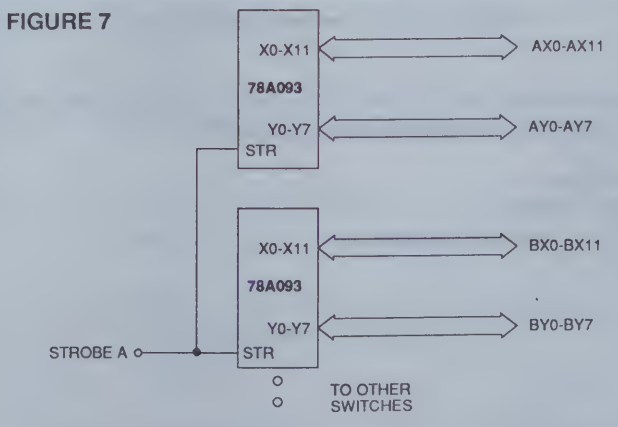


FIGURE 7



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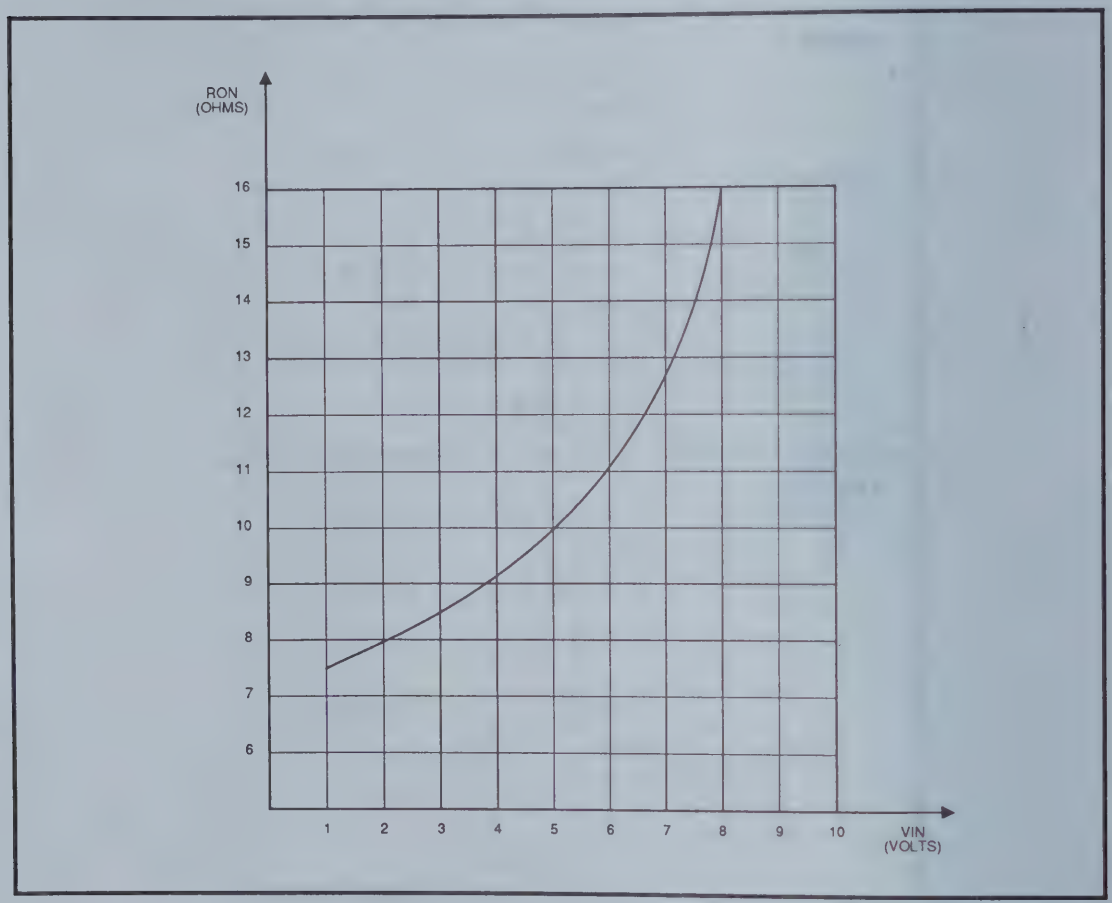


FIGURE 8: X0 - Channel: RON vs. VIN

Figure 8 is valid for all switches connected to the X0 channel only. The graph describes the behavior of the switch resistance RON as a function of the analog signal voltage VIN.

TEST CONDITIONS: VSS = 0V
VDD = 13.2V
RL = 1KΩ (Load Resistance)

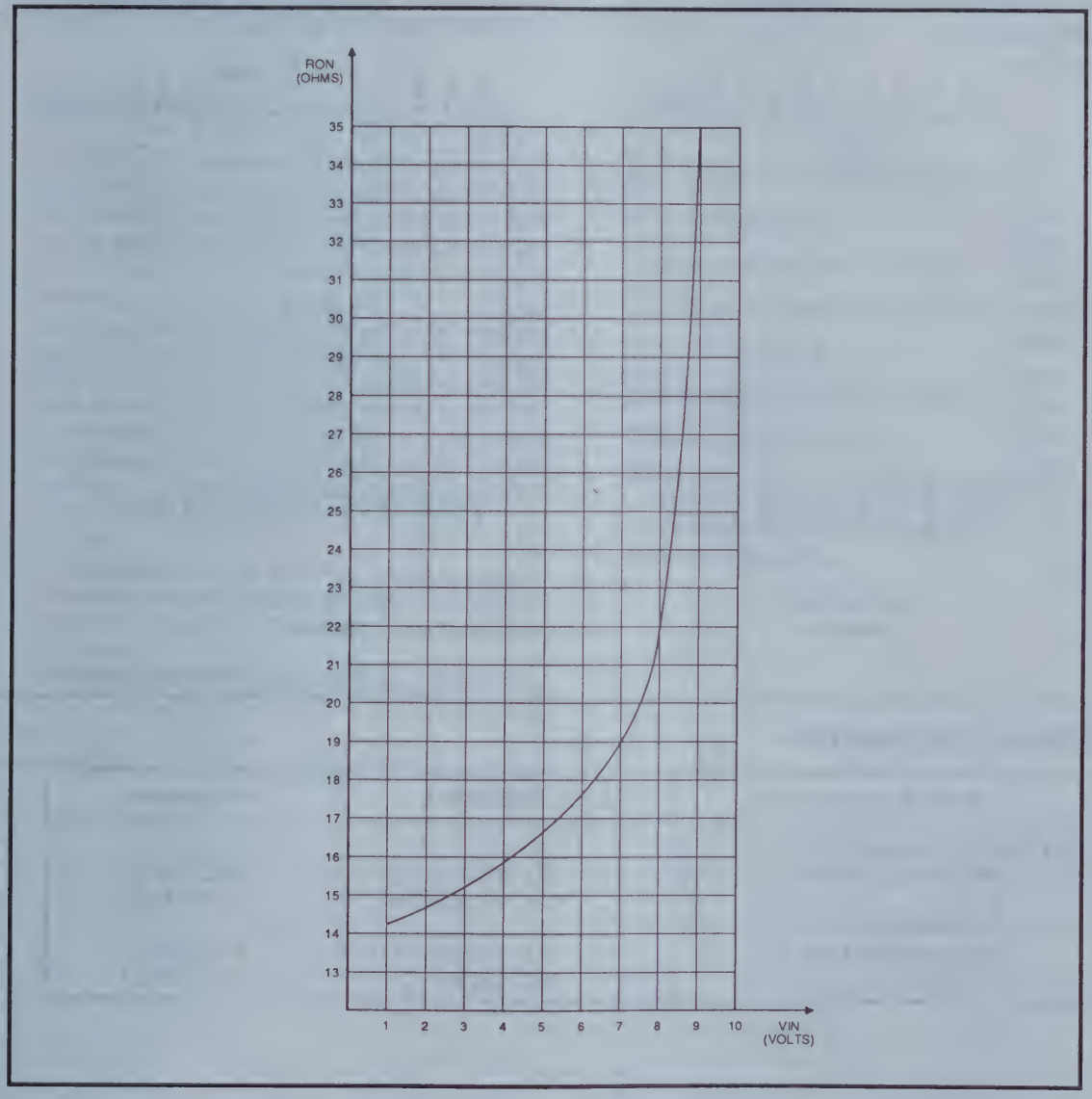


FIGURE 9: X1 - X11 Channel: RON vs. VIN

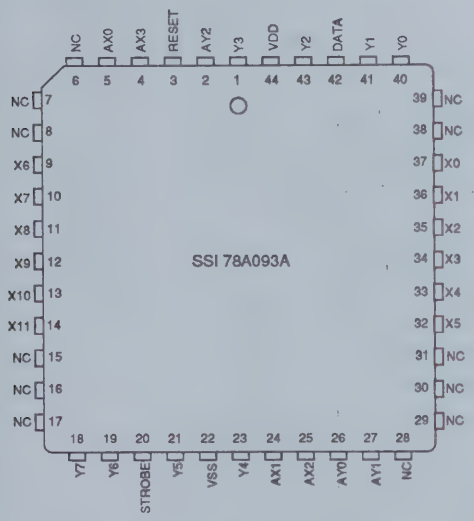
Figure 9 is valid for all switches connected to X1 thru X11 channels. The graph describes the behavior of the switch resistance RON as a function of the analog signal voltage VIN.

TEST CONDITIONS: VSS = 0V
VDD = 13.2V
RL = 1KΩ (Load Resistance)

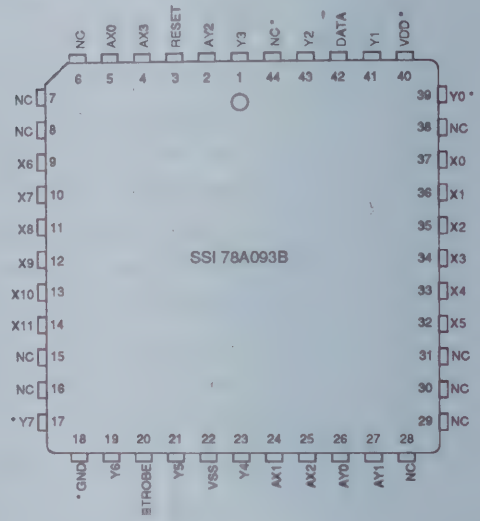
SSI 78A093A/B
CMOS 12x8x1
Crosspoint Switch
With Control Memory

PACKAGE PIN DESIGNATIONS
(TOP VIEW)

Refer to the SSI Data Book for package dimensions.
Please see Page 1 for PDIP pinout.



44 - Pin PLCC
78A093A



44 - Pin PLCC
78A093B

* different pins relative to 78A093A

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 78A093, Version A		
Plastic Dual-In-Line	SSI 78A093A-CP	78A093A-CP
PLCC	SSI 78A093A-CH	78A093A-CH
SSI 78A093, Version B		
Plastic Dual-In-Line	SSI 78A093B-CP	78A093B-CP
PLCC	SSI 78A093B-CH	78A093B-CH

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SSI 78A207
MFR1 Receiver

June, 1989

DESCRIPTION

The SSI 78A207 is a single-chip, Multi-Frequency (MF) receiver that can detect all 15 tone-pairs, including ST and KP framing tones. This receiver is intended for use in equal access applications and thus meets both Bell and CCITT R1 central office register signalling specifications.

The SSI 78A207 employs state-of-the-art switched capacitor filters in CMOS technology. The receiver consists of a bank of channel-separation bandpass filters followed by zero-crossing detectors and frequency-measurement bandpass filters, an amplitude check circuit, a timer and decoder circuit, and a clock generator. The device does not attempt to identify strings of digits by the KP (key pulse) and ST (stop) tone pairs.

No anti-alias filtering is needed if the input signal is band-limited to 26 KHz. The only external component required is an inexpensive television "color burst" 3.58 MHz crystal.

The outputs interface directly with standard CMOS or TTL circuitry and are three-state enabled to facilitate bus-oriented architecture.

FEATURES

- Meets Bell and CCITT R1 specifications
- 20-pin plastic DIP
- Single low-tolerance 5V supply
- Detects all 15 tone-pairs including ST and KP
- Long KP capability
- Built-in amplitude discrimination
- Excellent noise tolerance
- Outputs in either "n of 6" or hexadecimal code
- Three-state outputs, CMOS-compatible and TTL-compatible

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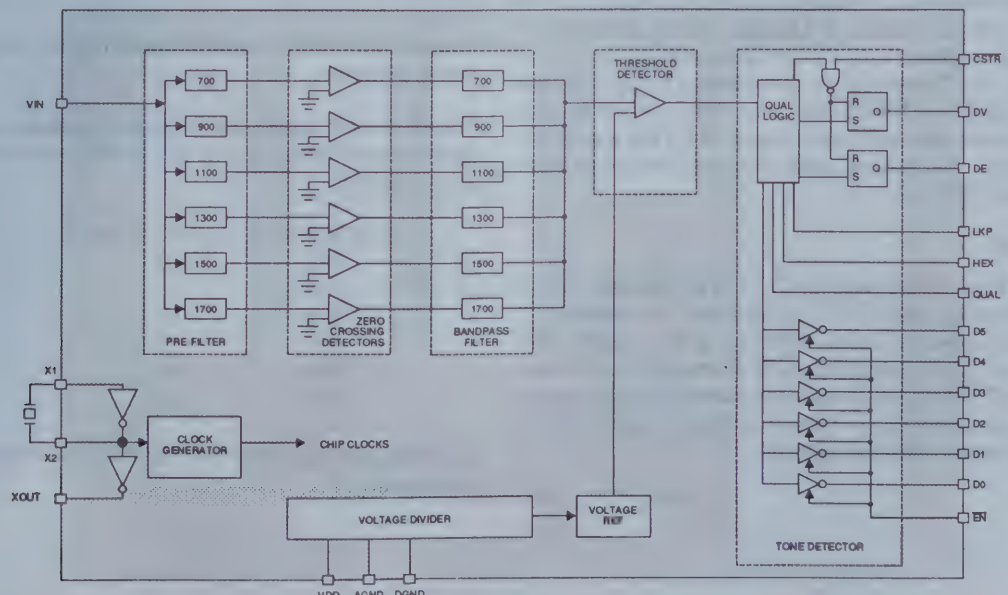
BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

VIN

This pin accepts the analog input. It is internally biased to half the supply and is capacitively coupled to the channel separation filters. The input may be DC coupled as long as it does not exceed VDD or drop below GND. Equivalent input circuit is shown below in Figure 1.

CRYSTAL OSCILLATOR

The SSI 78A207 contains an on-board inverter with sufficient gain to provide oscillation when connected to a low cost television "color-burst" crystal. The on-chip clock signals are generated from the oscillator. The crystal is connected between X1 and X2.

XOUT is a 3.58 MHz square wave capable of driving other circuits as long as the capacitive load does not exceed 50 pF. Other devices driven by XOUT should use X1 as the input pin, while X2 should be left floating.

LKP

The KP timer control: When high, the KP detect time is increased. When low, the KP detect time is the same as for other tones.

QUAL

Enables tone pair qualification. When low, the threshold detector outputs are passed to the data outputs (D0-D5) without validation in the format selected by the HEX pin. These outputs, plus strobes DV and DE, are updated once per 2.3 ms frame. Note that the strobes will cycle once per frame (even when the inputs are stable.) As always, data changes only when both strobes are low.

$\overline{\text{CSTR}}$

This input clears both the DV and DE strobes, and is active low. After $\overline{\text{CSTR}}$ is released, the strobes will remain low until a new detect (or error) occurs. The output data is latched by $\overline{\text{CSTR}}$ and will not change while $\overline{\text{CSTR}}$ is low, even in the event that a new detect is qualified internally. (Note that improper use of $\overline{\text{CSTR}}$ may result in missed detects.)

$\overline{\text{EN}}$

The three-state enable control: When low, the D0-D5 outputs are in the low impedance state. In an interrupt oriented microprocessor interface, $\overline{\text{EN}}$ and $\overline{\text{CSTR}}$ will often be tied together to provide automatic reset of the strobes when the output data is enabled.

STROBE PINS - DV AND DE

Valid data is indicated on the DV strobe pin, and data errors are indicated on the DE strobe pin. Whenever a valid 2 of 6 code has been detected, the DV strobe rises. It remains high until the code goes away, or the $\overline{\text{CSTR}}$ line is activated. When an invalid code is detected, e.g., 1 of 6, 3 of 6, etc., the DE strobe remains high until all errors stop, a valid tone pair is detected, or the $\overline{\text{CSTR}}$ line is activated. Once cleared by $\overline{\text{CSTR}}$, DE will not reactivate until a new invalid condition is detected. The DE and DV strobes will never be high simultaneously.

DATA OUTPUT MODES

The digital output format may be either "n of 6" or 4-bit hexadecimal.

For "hex" mode, the HEX pin is pulled high. Outputs D0 to D3 provide a 4-bit code identifying one of the 15 valid tone combinations according to Table1.

The outputs will be cleared to zero when no valid tone pair is present.

For the "n of 6" mode, the HEX pin is pulled low, and each output represents one of the six frequencies as shown below:

FREQUENCY	OUTPUT PIN
700	D0
900	D1
1100	D2
1300	D3
1500	D4
1700	D5

The outputs will be cleared to zero when no valid tone is present.

TABLE 1:

Channels	Tone Pair Freq.	Name	D3	D2	D1	D0
0-1	700, 900	1	0	0	0	1
0-2	700, 1100	2	0	0	1	0
1-2	900, 1100	3	0	0	1	1
0-3	700, 1300	4	0	1	0	0
1-3	900, 1300	5	0	1	0	1
2-3	1100, 1300	6	0	1	1	0
0-4	700, 1500	7	0	1	1	1
1-4	900, 1500	8	1	0	0	0
2-4	1100, 1500	9	1	0	0	1
3-4	1300, 1500	0	1	0	1	0
2-5	1100, 1700	KP	1	0	1	1
4-5	1500, 1700	ST	1	1	0	0
1-5	900, 1700	ST1	1	1	0	1
3-5	1300, 1700	ST2	1	1	1	0
0-5	700, 1700	ST3	1	1	1	1
	any other signal		0	0	0	0

NOTE: In the hex mode, D4 = DE and D5 = DV.

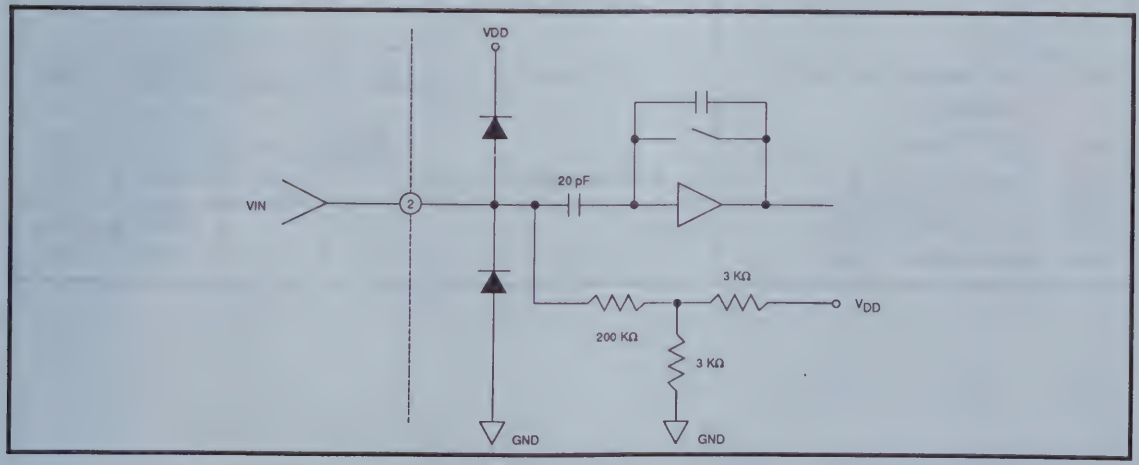


FIGURE 1: VIN Equivalent Input Circuit

TIMING SPECIFICATIONS

	PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Ton	Tone Time, KP (LKP = VDD)	detect	55			ms
Ton		reject			30	ms
Ton	Tone Time, KP (LKP = DGND)	detect	30			ms
Ton		reject			10	ms
Ton	Tone Time, All Others	detect	30			ms
Ton		reject			10	ms
Tpse	Pause Time	detect	20			ms
Tbr		reject			10	ms
Tsu	Data Setup Time		6			µs
Th	Data Hold Time		7			µs
Tskew	Tone Skew Tolerance				4	ms
Tstr	Minimum Strobe Pulse Width					
	QUAL High		20			ms
	QUAL Low		2			ms
Tsep	Minimum Strobe Separation					
	QUAL High		20			ms
	QUAL Low		2			ms
Tr	Rise Time DV, DE, D0-D5 10-90%	CL = 20 pF			100	ns
Tf	Fall Time DV, DE, D0-D5 10-90%	CL = 20 pF			100	ns
Tw	$\overline{\text{CSTR}}$ Width		50			ns
Ten	Data Enable Time	CL = 20 pF			100	ns
Tdis	Data Disable Time				100	ns
Trst	Strobe Reset Time	CL = 20 pF			100	ns

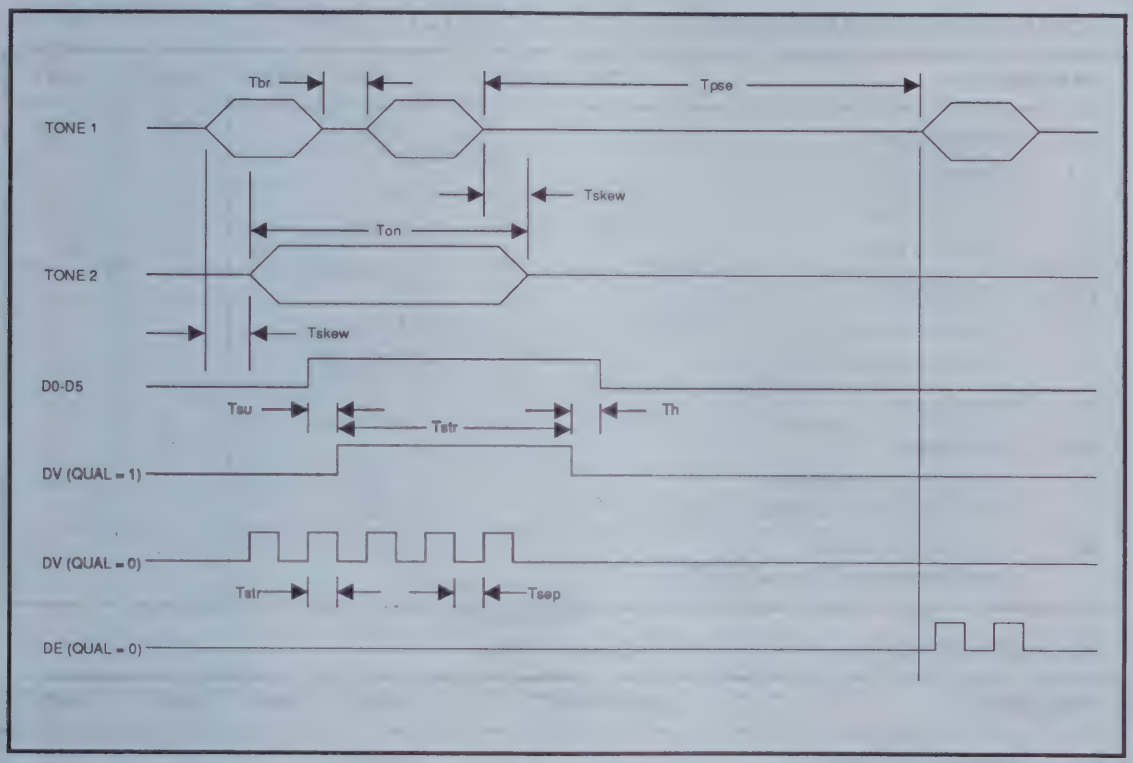


FIGURE 2: SSI 78A207 Timing Diagram

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

(Operating above absolute maximum ratings may damage the device.)

PARAMETER	RATING	UNIT
DC Supply Voltage V_{DD}	+ 7	V
Operating Temperature	0 to 70 (Ambient)	°C
Storage Temperature	65 to 150	°C
Power Dissipation (25°C) (Derate above TA=25°C @ 6.25 mW/°C)	650	mW
Input Voltage	(V_{DD} + 0.3V) to -0.3	V
DC Current into any input	±10	mA
Lead Temperature (Soldering, 10 sec.)	300	°C

DC ELECTRICAL CHARACTERISTICS (0°C ≤ TA ≥ 70°C, VDD = 5V ± 10%)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Idd	Supply Current				20	mA
Vol	Output Logic 0					
	Iol = 8 mA				0.5	V
	Iol = 1 mA				0.4	V
Voh	Output Logic 1					
	Ioh = -4 mA		VDD-1.0			V
	Ioh = -1 mA		VDD-0.5			V
Vih	Input Logic 1		2.0			V
Voh	Input logic 0				0.8	V
Zin	Analog Input Impedance (Input between VDD and AGND)		100K 30 pF			Ω
Iin	Digital Input Current (Input between VDD and DGND)		-50		50	µA

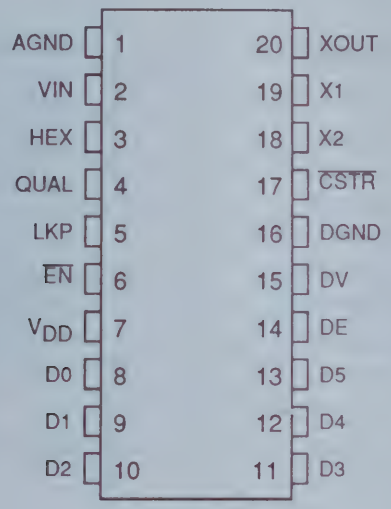
AC CHARACTERISTICS (0°C ≤ TA ≥ 70°, VDD = 5V ± 10%)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
F	Frequency for Detect Tolerance		±(0.015 xFo + 5)			Hz
A	Amplitude for Detect	each tone	-25		0	dBm
			0.123		2.191	Vpp
AN	Amplitude for no Detect				-35	dB
					0.039	Vpp
TW	Twist Tolerance	$TW=\frac{\text{high tone}}{\text{low tone}}$	-6		+6	dB
T3	Third MF Tone Reject Amp	relative to highest amplitude tone	-15			dB
N60	60 HZ Tolerance	not more than one error	81			dBm
		in 2500 10-digit calls	0.777			Vpp
N180	180 HZ Tolerance	same as above	68			dBm
			0.174			Vpp
Nn	Noise Tolerance[1]	same as above			-20	dB
NI	Impulse Noise Tolerance[2]	same as above			+12	dB

NOTES: 1. C-message weighted. Measured with respect to highest amplitude tone.

2. With noise tape 201 per PUB 56201. Measured with respect to highest amplitude tone.

PACKAGE PIN DESIGNATIONS
(TOP VIEW)



20 - PIN DIP

5

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 78A207 20-Pin Plastic DIP	SSI 78A207-CP	78A207-CP

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NOTES:

SSI 78A400/420
Four-Wire Loopback IC

June, 1989

DESCRIPTION

The SSI 78A400 is a low-power CMOS integrated circuit that provides the 2713 and 2913 Hz detector and control circuitry needed to perform remote loopback testing on 4-wire telephone lines. As the major functional block in a Maintenance Terminating Unit (MTU), the SSI 78A400 offers a compact, low-power, high performance alternative to currently available discrete loopback circuitry.

The highly integrated SSI 78A400 incorporates a precise tone detector with guard-band and signal-timing qualification, a programmable fail-safe timer for loopback, and a loopback output for controlling an external relay. A manual-enable feature also allows for on-site loopback testing in the field. The SSI 78A420 has the added feature of two uncommitted operational amplifiers for the purpose of adding gain or loss to the signal path.

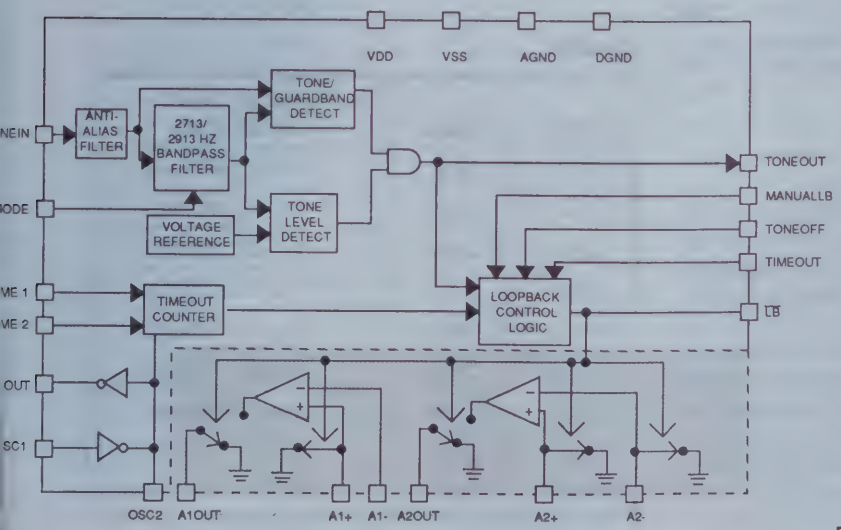
The SSI 78A400/420 Loopback Control IC employs advanced CMOS design technology for low power operation (±5 volts, at less than 50mW dissipation). Operation conforms to Bell Publications 43003/43004 specifications.

FEATURES

- Precise selectable 2713/2913 Hz tone detection.
- SSI 78A420 with added gain/loss block.
- Integrated tone-detect and timing functions.
- Crystal-controlled timers and filters assure high accuracy.
- Immune to false activation by voice, data or 2600 Hz tone.
- Provision for on-site manual loopback and release.
- Adjustable time-out provides for automatic loopback deactivation.
- Performs auto reset during start-up.
- Compatible with Bell Publications 43003/43004 specifications.
- Low power CMOS designs: ±5 volts power at < 50mW dissipation.
- Compact 16-pin DIP or 18-pin SOIC packages for 78A400; 22-pin DIP for 78A420.

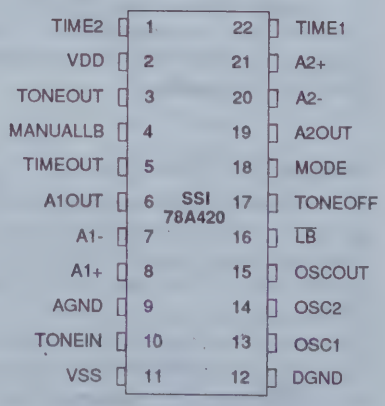
5

BLOCK DIAGRAM



Area enclosed in dotted lines ⬚ applies to SSI 78A420 only.

PIN DIAGRAM



(SSI 78A400 pin-out shown inside)

CAUTION: Use handling procedures necessary for a static sensitive component.

CIRCUIT OPERATION

LOOPBACK AND RELEASE

Functionally, the 78A400 works by receiving a 2713 or 2913 Hz tone sent from the test source, qualifying this tone for a specified time interval, and enabling a loopback-control output that activates a relay to bridge the transmit and receive lines in the 4-wire circuit. A pre-characterized test pattern is then transmitted from the central office, looped back to the receive line, received, and interpreted to determine if there is a problem with line integrity. At the completion of the test, the loopback is terminated by a second qualified 2713 or 2913 Hz command tone, or by a fail-safe timer that responds to a selectable time-out interval preset during installation. (See Table 1.)

Activating the loopback connection ($\overline{LB}$=0) is accomplished on removal of a valid tone that has been present for 1.6 seconds. The loopback is released by a second valid tone that is present for 0.8 seconds. The loopback function can also be controlled manually by the MANUALLB pin. (See Table 2.) A reset during power-on inhibits activation of the loopback by maintaining the $\overline{LB}$ pin in a high state for 2.8 seconds after power is applied.

Prior to tone qualification, a tone dropout of greater than 22ms will be detected as a loss of tone, while a tone dropout of less than 7ms will be ignored. After tone qualification, a tone dropout of greater than 175ms will be detected as a loss of tone, whereas a tone dropout of less than 80 ms will be ignored. (Refer to the Timing Diagram.)

TONE DETECT CIRCUITRY

The 78A400 is capable of detecting either of two tones, centered at 2713 Hz or 2913 Hz. The 2713 Hz (±7 Hz) tone will be detected when the MODE pin is tied high. The 2913 Hz (±7 Hz) tone will be detected when the MODE pin is tied low. Tone energy is required to be between 0 dBm and -32 dBm in order for detection to occur. The tone will not be detected if its energy is less than -40 dBm or if its frequency deviation is greater than ±37 Hz from the center frequency.

TONE-TO-GUARD CIRCUITRY

If guard energy between 300 Hz and 2450 Hz is present, along with a qualified tone (as described under Tone Detect Circuitry), and the ratio between the qualified tone and the guard energy is greater than 18 dB, then a valid tone/guard condition will be detected. A valid tone/guard condition will not be detected for a tone-to-guard ratio of less than 6 dB.

OPERATING STATE SELECTION

Various loopback activation and release states can be selected using the MANUALLB, TONEOFF, and TIMEOUT control inputs. Manual loopback, loopback disable and loopback release options can be selected using these inputs, as noted in Table 2.

GAIN/LOSS BLOCK

In addition to the 4-wire loopback circuitry provided by the SSI 78A400, the SSI 78A420 provides two uncommitted operational amplifiers that can be adjusted by external components as a gain/loss block during loopback. During the loopback inactive condition ($\overline{LB}$ = high), all the operational amplifier inputs and outputs, except A1, are tied to the internal analog ground. The A1 pin is left floating.

TABLE 1

TIME1	TIME2	Timeout Times Normal Mode
Low	Low	1.5 ± 0.1 Minutes
Low	High	2 ± 0.1 Minutes
Low	Open	4 ± 0.1 Minutes
High	Low	6 ± 0.1 Minutes
High	High	9 ± 0.1 Minutes
High	Open	12 ± 0.1 Minutes
Open	Low	15 ± 0.1 Minutes
Open	High	18 ± 0.1 Minutes
Open	Open	20 ± 0.1 Minutes

TABLE 2

MANUALLB	TONEOFF	TIMEOUT	OPERATING STATE
low	low	low	Disables tone activated loopback ($\overline{LB}$ pin high).
low	low	high	Upon loopback activation by tone, circuit returns to loopback release state after time as defined by TIME1 and TIME2 pins.
low	high	low	Upon loopback activation by tone, circuit returns to loopback release state after losing the tone for more than 0.15 seconds and then receiving a second tone of 0.8 seconds duration.
low	high	high	Upon loopback activation by tone, circuit returns to loopback released state by timeout or tone, whichever occurs first.
high	x	x	Circuit is in loopback active ($\overline{LB}$ pin low) condition; tone detect circuitry is deactivated in order for tones not to interfere with this manual state.

PIN DESCRIPTION

I/O	LABEL	PIN NUMBER		DESCRIPTION
		78A400	78A420	
-	VDD	1	2	Positive power supply, 5V +20%, -10%
-	VSS	7	11	Negative power supply, -5V +10%, -20%
-	AGND	5	9	Analog ground
-	DGND	8	12	Digital ground
I I	OSC1 OSC2	9 10	13 14	Connection for a 3.5795 MHz parallel mode crystal. Crystal variation should not exceed a max of ±0.04%. An external CMOS logic level clock may be used to drive OSC2 if the crystal input is not used. OSC1 should then be tied to DGND.
O	OSCOUT	11	15	Oscillator buffered output. Outputs 3.5795 MHz clock in normal mode.
I I	TIME 1 TIME2	15 16	22 1	Timeout time control pins. Controls the loopback timeout sequence as shown in Table 1.
I	MODE	14	18	Tone-detect frequency selection. To detect 2713 Hz tone, tie the MODE pin high. To detect 2913 Hz tone, tie the MODE pin low.

PIN DESCRIPTION (continued)

I/O	LABEL	PIN NUMBER		DESCRIPTION
		78A400	78A420	
O	TONEOUT	2	3	Output from the tone detect section used for monitoring internal signals in test mode only.
I	TONEIN	6	10	Input for 2713 Hz tone detector.
O	$\overline{LB}$	12	16	Loopback digital output. A low state indicates a loopback activate condition. A high state indicates a loopback release condition. TTL compatible.
I	MANUALLB	3	4	Input to manually set chip into loopback active condition. See Table 2.
I	TONEOFF	13	17	Input to incorporate tone disable of loopback. See Table 2.
I	TIMEOUT	4	5	Input to incorporate timeout disable of loopback. See Table 2.
I	A1–	NA	7	Inverting gain/loss block input.
I	A1+	NA	8	Non-inverting gain/loss block input.
O	A1OUT	NA	6	Gain/loss block output.
I	A2–	NA	20	Inverting gain/loss block input.
I	A2+	NA	21	Non-inverting gain/loss block input.
O	A2OUT	NA	19	Gain/loss block output.

ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
Supply Voltage	VDD	6.5	V
Supply Voltage	VSS	-6.5	V
Storage Temperature		-65 to 150	°C
Soldering Temperature (10 sec.)		260	°C
Applied Voltage, All Inputs		VSS-0.3 to VDD+0.3 or 50mA	V
Output Voltage, All outputs		DGND-0.3 to VDD+0.3 or 50mA	V

NOTE: All inputs and outputs are protected from static charge using built-in, industry standard protection devices and all outputs are short-circuit protected.

RECOMMENDED OPERATING CONDITIONS

PARAMETER		CONDITIONS	MIN	MAX	UNITS
Ambient Temperature			–40	85	°C
Positive Power Supply	VDD		4.5	6	V
Negative Power Supply	VSS		–6	–4.5	V
Supply Variation	VDD – | VSS |		–1	1	V
Digital Ground (DGND)			VSS–0.1	AGND+0.1	V
Crystal Frequency Variation		3.5795 MHz	–0.04	+0.04	%
Digital Inputs, Low	MANUALLB TONEOFF		DGND–0.3	DGND+0.8	V
Digital Inputs, High			DGND+3	VDD+0.3	V
Input Low Voltage	TIME1, TIME2		DGND	DGND+0.3	V
Input Medium Voltage	TIME1, TIME2	Pin open			
Input High Voltage	TIME1, TIME2		VDD–0.4	VDD	V
Input Low Voltage	MODE	Test mode	VDD–1.7	VDD–1.5	V
Input High Voltage	MODE	Normal mode	VDD–0.1	VDD	V
Input Current	(All Inputs)	DGND≤VIN≤VDD	–100	100	µA
Input Low Voltage	OSC2	External Frequency	DGND–0.3	DGND+0.4	V
Input High Volyage	OSC2	Source; OSC1 at DGND	DGND+3	VDD+0.3	V

DC ELECTRICAL CHARACTERISTICS

PARAMETER		CONDITIONS	MIN	MAX	UNITS
Positive Supply Current	IDD				
In Loopback		Outputs unloaded		9	mA
Not In Loopback		Outputs unloaded		8	mA
Negative Supply Current	ISS				
In Loopback		Outputs unloaded		–9	mA
Not In Loopback		Outputs unloaded		–8	mA
Analog Ground (AGND) Supply Current			–250	+250	µA
Output High Voltage	$\overline{LB}$, OSCOUT	IOUT = –0.4mA	DGND+2.4	VDD	V
Output Low Voltage	$\overline{LB}$, OSCOUT	IOUT = 4mA		DGND+0.4	V
Output High Voltage	TONEOUT	IOUT = –40µA	VDD–0.5		V
Output Low Voltage	TONEOUT	IOUT = 40µA		VSS+0.5	V

DYNAMIC CHARACTERISTICS AND TIMING

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
Tone Detection						
Frequency	2713 Hz	Mode = high	2706		2720	Hz
Frequency	2913 Hz	Mode = low	2906		2920	Hz
Amplitude			–32		0	dBm
Tone To Guard Band Ratio		300–2450 Hz Guard Energy	18			dB
Tone Dropout Reject	T_{TDB}	Before Qualification			7	ms
Tone Dropout Detect	T_{TDB}	Before Qualification	22			ms
Tone Dropout Reject	T_{TDA}	After Qualification			80	ms
Tone Dropout Detect	T_{TDA}	After Qualification	175			ms
Tone Detect Qualification Time						
Loopback Activate			1.5	1.6	1.7	s
Loopback Release			0.7	0.8	0.9	s
Tone Rejection						
Frequency	2713 Hz	Mode = high	$F_0 \leq 2676$; $F_0 \geq 2750$Hz			
Frequency	2913 Hz	Mode = low	$F_0 \leq 2876$; $F_0 \geq 2950$Hz			
Amplitude			–40			dBm
Tone To Guard Band Ratio					6	dB
Alias Energy Detect		Energy > 90KHz	–36			dBm
Input Impedance At Tone In				100		KΩ
Power On Reset Delay Time				2.8		s

GAIN/LOSS CHARACTERISTICS

PARAMETERS	CONDITION	MIN	NOM	MAX	UNITS
Input Offset Voltage	$\overline{LB}$ = Low			20	mV
Unity Gain Bandwidth	$\overline{LB}$ = Low	0.8			MHz
Max. Output Voltage Swing	$\overline{LB}$ = Low, RL = 5K CL ≤30 pF, THD ≤1%	4.0			Vpp
Input Referred Noise Voltage	$\overline{LB}$ = Low			0.16	$\mu V/\sqrt{Hz}$
Input Common Mode Voltage	$\overline{LB}$ = Low	VSS+2.0		VDD–2.0	V
Open Loop DC Gain	$\overline{LB}$ = Low	80			dB
(Loopback inactive) Shorting Pin To GND Resistance	$\overline{LB}$ = High			200	Ω

APPLICATION

The 78A400 would typically reside in a 4-wire telephone line Maintenance Terminating Unit (MTU), as shown in Figure 1. In this application, the 78A400 monitors the receiver side of the 4-wire telephone circuit for a loopback command signal (a 2713 Hz tone) to be sent from testing equipment in the telephone company's central office.

When the loopback command tone is received, the 78A400 qualifies the tone for frequency, amplitude, and adequate level above other energy in the guard band frequency range of 300-2450 Hz. Additional to these qualifications, the tone must also be continuous for 1.6 seconds. After this timed interval, termination of the qualified tone will activate the $\overline{LB}$ output (logic "0"). This extensive command-tone qualification prevents false loopback activation, which could cause an interruption of normal line communications.

Activation of the $\overline{LB}$ output drives a loopback relay that bridges the transmit and receive signal paths, disconnecting the customer premises equipment from the phone line. Once this loopback is in place, the central office test equipment can transmit known test signals on the transmit line and receive these signals back on the receive line. A comparison of these test results with predetermined line-characterization data allows verification of the integrity of the network, without the need for a service call. Upon completion of the testing sequence, the MTU is returned to its operational state by transmitting a second qualified tone from the central office to deactivate the loopback connection. As a backup, a fail-safe timer, adjusted during MTU setup, will also cause release of the loopback after a pre-set time interval.

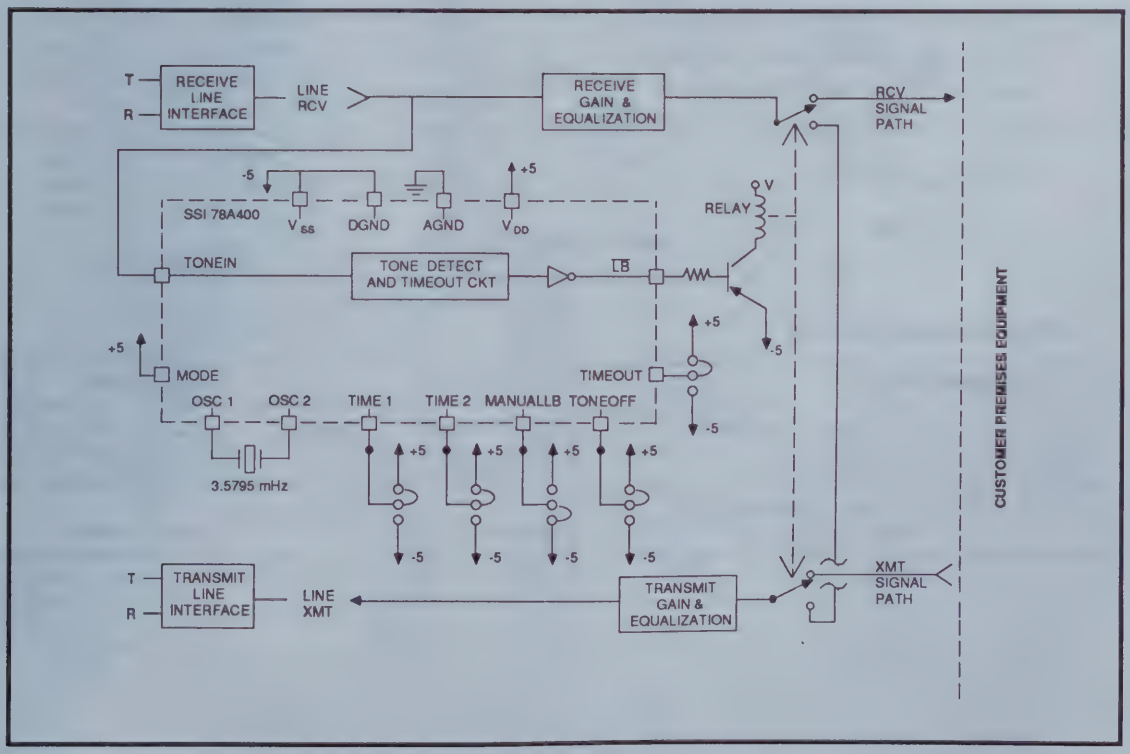
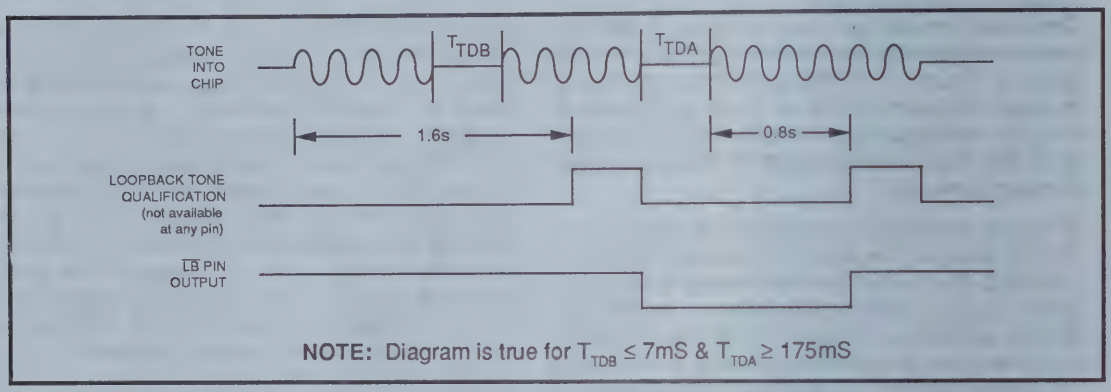


FIGURE 1: SSI 78A400 4-Wire Loopback Controller Typical MTU Application

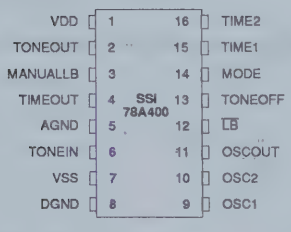
SSI 78A400/420
Four-Wire Loopback IC

TIMING DIAGRAM

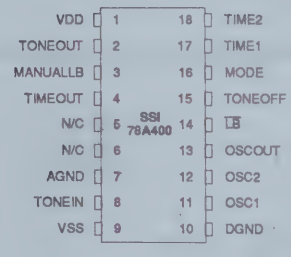


NOTE: Diagram is true for $T_{TDB} \leq 7mS$ & $T_{TDA} \geq 175mS$

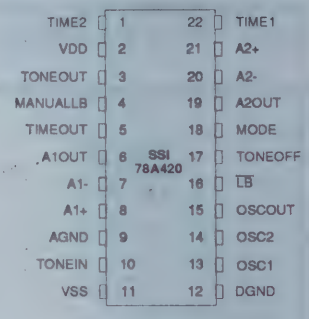
PACKAGE PIN DESIGNATIONS



16-PIN DIP



18-PIN SMALL OUTLINE



22-PIN DIP

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 78A400 16-Pin Plastic Dual-in-line	SSI 78A400-IP	78A400-IP
SSI 78A400 18-Pin Small Outline	SSI 78A400-IL	78A400-IL
SSI 78A420 22-Pin with Gain/Loss Block Plastic Dual-in-line	SSI 78A420-IP	78A420-IP

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SSI 78P233
DS-1 Line Interface

June, 1989

DESCRIPTION

The SSI 78P233 DS-1 Line Interface is a bipolar integrated circuit that provides the interface functions necessary to convert DS-1-level signals to TTL-level and conversely. The receiver section accepts alternate-mark-inversion (AMI) encoded line data and provides separated and synchronized data and clock outputs. The transmitter section accepts data and clock and produces AMI pulses of appropriate shape for transmission. A loopback multiplexer is also provided that permits interchange of the signals between the sections.

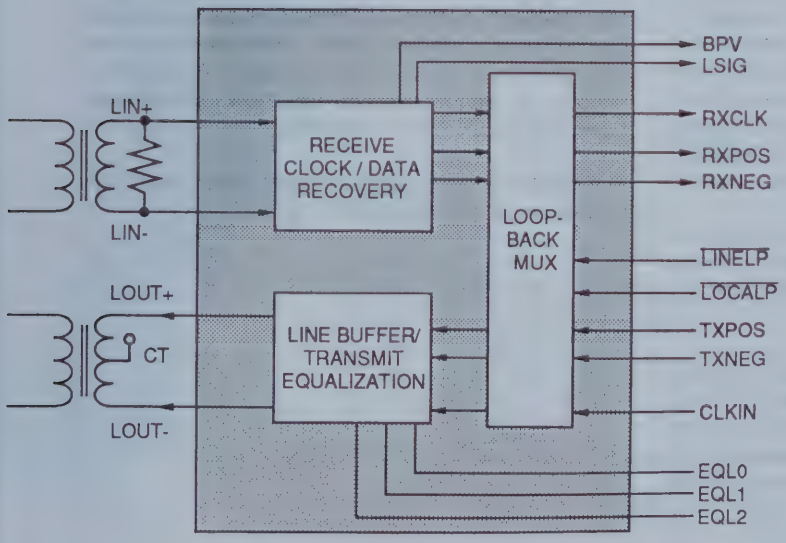
The 78P233 requires a single 5V supply. It is available in three different packages: standard, 600-mil DIP; narrow, 300-mil DIP; small outline (SOIC).

FEATURES

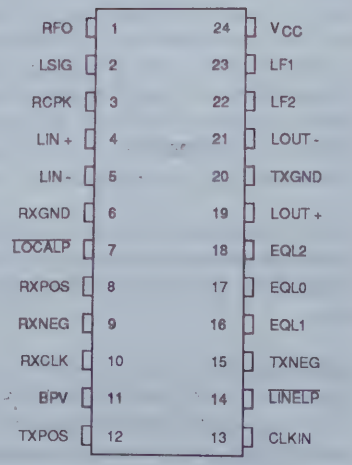
- Single-chip transmit and receive DS-1 Line Interface
- Unique clock recovery circuit, requires no crystals or tuned components
- Variable jitter tolerance, adjustable with external components
- Pulse-shape transmission conformant with AT&T Compatibility Bulletin 119 specifications
- Six different line equalization settings for pulse-shaping at the DSX-1 level
- Two alternate transmit settings for 6V-peak pulses
- Standard unipolar TTL-level clock & data ports for easy equipment interface
- Line-loopback and local-loopback control
- Loss-of-signal indication
- Bipolar violation detection

5

BLOCK DIAGRAM



PIN DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

FUNCTIONAL DESCRIPTION

The device consists of receiver and transmitter sections together with a "loopback" means which permits interchange of signals between the sections (See Figure 1).

RECEIVER

The receiver input is normally transformer-coupled to the source of encoded alternate polarity pulses. To provide a tracking threshold for amplitude-detecting these pulses, the signal is peak detected and a fixed percentage of the peak value is applied to the comparators which detect individual positive and negative pulses. An external R-C network is required to provide the proper storage of the peak reference value. Should the detected peak value fall below an acceptable level, the Loss of Signal (LSIG) output becomes active. This output may be used as a logical control signal or is able to drive a fault indicator LED directly.

Outputs of the data comparators are connected to the clock recovery circuits. The clock recovery system employs a unique phase-locked-oscillator loop which has an auxiliary frequency-sensitive acquisition loop which is active only when cycle-slipping occurs between the received signal rate and the internal oscillator. This system permits the loop to independently lock to the frequency and phase of the incoming data stream without the need for high-precision and/or adjustable oscillators or tuned circuits. Non-precision external components are required, however, to establish the oscillator center frequency and loop bandwidth.

The phase-locked reference oscillator is employed to strobe the detected data into output latches and is also available as an output for externally synchronizing the data.

Additional circuits are provided to detect received bipolar violations. These deviations from the alternate mark inversion format are detected when two or more successive pulses of the same polarity are received. A resultant violation output is in time coincidence with the violating received signal output.

TRANSMITTER

The transmitter combines unipolar logical inputs with an input clock to provide positive and negative output pulses onto a transformer-coupled line.

Internal equalizer networks are selected by combinations of the three Equalizer Select inputs so that the waveform at the terminal end of various lengths of cable is as required. Note that the transmitter output pulse widths are determined by the input clock width, so that it must be carefully controlled to provide acceptable outputs.

The transmitter pulse selection logical function is arranged so that the simultaneous occurrence of both positive and negative transmit data inputs inhibits the output driver. Moreover, the driver has a current-limiting feature which protects the circuit in the event of a shorted load or inadvertent shorting of an output to the supply voltage.

LOOPBACK CONTROL SECTION

The loopback control section is essentially a multiplexer which is capable of directing received data and clock to the transmitter section, or directing transmit input data and clock to the receiver outputs. This "looping" is controlled by two active low logic signals, $\overline{\text{LINELP}}$ and $\overline{\text{LOCALP}}$, respectively.

The bipolar violation output is held inactive when the circuits are in the Local Loopback mode.

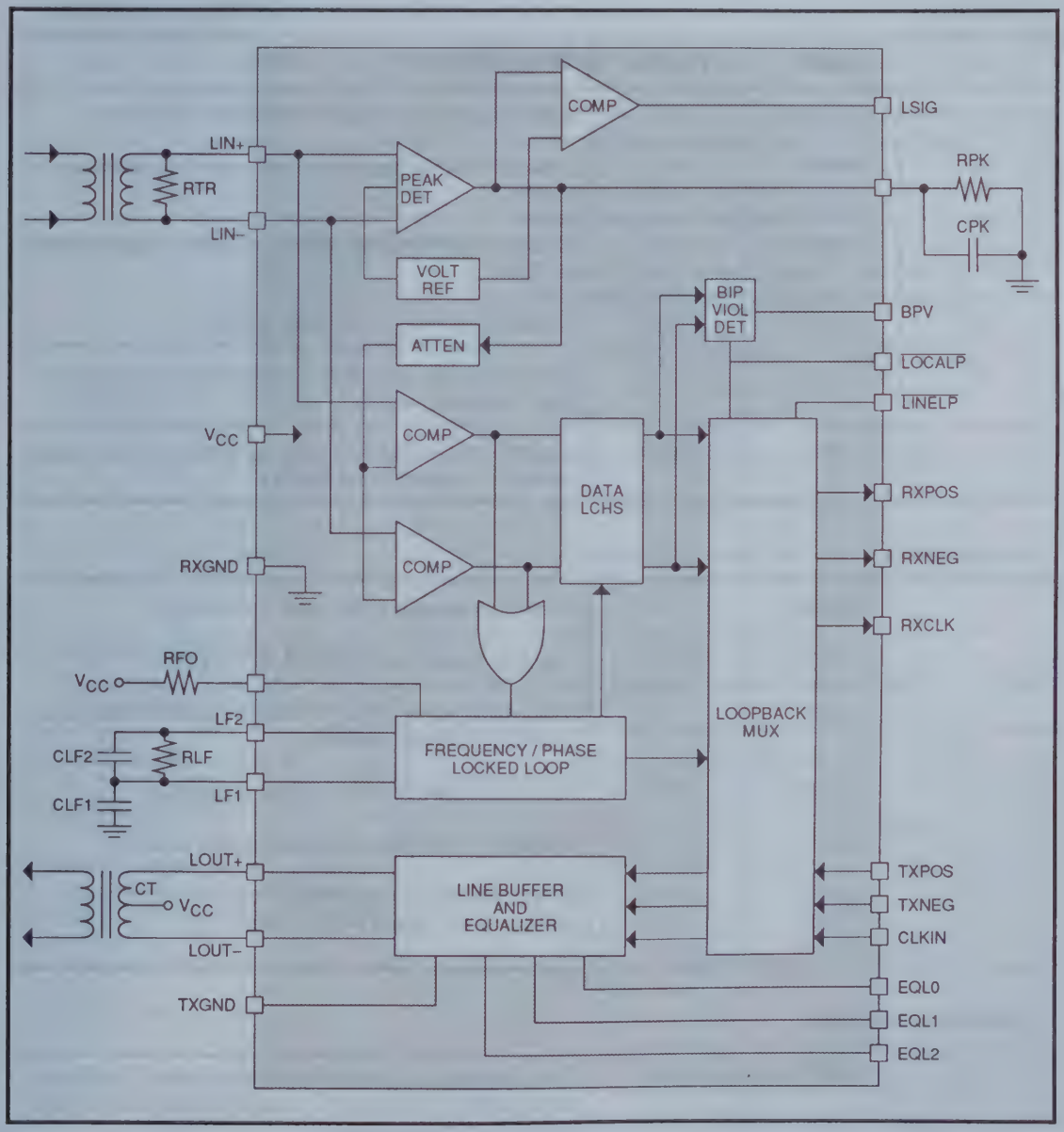


FIGURE 1: Functional Diagram

PIN DESCRIPTION

RECEIVER

I/O	LABEL	PIN NO.	DESCRIPTION
I	LIN+, LIN-	4, 5	Differential inputs, transformer-coupled from line.
O	RXPOS	8	Unipolar receiver output, active as result of positive pulse at inputs.
O	RXNEG	9	Unipolar receiver output, active as result of negative pulse at inputs.
O	RXCLK	10	Clock pulses recovered from line data.
O	LSIG	2	Loss-of-signal output indicating that input signal is less than threshold value.
O	BPV	11	Bipolar violation output, active as a result of successive pulses at inputs of same polarity.

TRANSMITTER

I	TXPOS	12	Unipolar transmitter data input, active high.
I	TXNEG	15	Unipolar transmitter data input, active high.
I	CLKIN	13	Transmitter clock input. Controls transmit pulse width. Transmit is active when low.
O	LOUT+	19	Output to transformer for positive data pulses.
O	LOUT-	21	Output to transformer for negative data pulses.
I	EQL0 EQL1 EQL2	17 16 18	Line equalizer control signals. Selected according to Table 1 for various cable lengths.

LOOPBACK CONTROL

I	$\overline{\text{LINELP}}$	14	Low level causes receiver recovered data and clock to be connected to the transmitter. Data and clock continue to be present at receiver outputs.
I	$\overline{\text{LOCALP}}$	7	Low level causes transmitter input data and clock to be connected to the receiver outputs. Input data continues to be transmitted.

PIN DESCRIPTION (continued)

EXTERNAL COMPONENT CONNECTION

I/O	LABEL	PIN NO.	DESCRIPTION
I	RFO	1	Resistor connected to Vcc to provide basic center frequency of receiver phase locked loop oscillator.
-	LF1 LF2	23 22	Resistor-capacitor loop filter network to RXGND to establish bandwidth of phase locked loop.
-	RCPK	3	Parallel resistor-capacitor network connected to RXGND to determine charge/discharge characteristics of peak detector.

POWER

-	Vcc	24	Positive supply terminal for receiver circuits.
-	RXGND	6	Ground terminal for receiver circuits.
-	TXGND	20	Ground terminal for transmitter driver circuits.

ABSOLUTE MAXIMUM RATINGS

(T_A = 0°C to 70°C, Vcc = 5V ± 5%, unless otherwise noted. Operation above absolute maximum ratings may permanently damage the device.)

PARAMETER	RATING	UNIT
Vcc, Supply Voltage	-0.5 to +7.0	V
Storage Temperature	-65 to 130	°C
Soldering Temperature (10 sec.)	260	°C
Voltage Applied to Logic Inputs	-0.5 to +7.0	V
Maximum Power Dissipation	800	mW
Junction Operating Temperature	0 to +130	°C

NOTE: All inputs and outputs are protected from static charge using built-in, industry standard protection devices and all outputs are short-circuit protected.

RECOMMENDED OPERATING CONDITIONS

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Ta	Ambient temperature		0		70	°C
Vcc	Power supply voltage		4.75		5.25	V
VIH	High-level input voltage		2.0			V
VIL	Low-level input voltage				0.8	V
IOH	High-level output current	LSIG pin only; VO = 1.5V	-7		-13	mA

EXTERNAL COMPONENTS (Refer to Figure 1 for location of components.)

RFO	Loop center frequency resistor	1% tolerance		6.04		KΩ
RLF	Loop filter resistor			12.0		KΩ
CLF1	Loop filter capacitor			0.022		µF
CLF2	Loop filter capacitor			430.0		pF
RPK	Peak-detector resistor			36.0		KΩ
CPK	Peak-detector capacitor		0.0015	0.015	0.15	µF
	Transmit line transformer	Refer to Table 3		---		---

D. C. ELECTRICAL CHARACTERISTICS

(T_A = 0°C to 70°C, Vcc = 5V ± 5%, unless otherwise specified.)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
ICC	Supply current	All outputs open		75	100	mA
IIH	High-level input current	VIH = 2.7V			20	µA
IIL	Low-level input current	VIL = 0.4V			-0.36	mA
VOH	High-level output voltage	IOH = -400 µA	2.7			V
VOL	Low-level output voltage	IOL = 4.0 mA; IOL = 2.0 mA, LSIG pin			0.4	V
RIN	Receiver input resistance		800	1000	1250	Ω

DYNAMIC CHARACTERISTICS AND TIMING, TRANSMITTER

(T_A = 0°C to 70°C, Vcc = 5V ± 5%, unless otherwise specified. Transmit pulse characteristics are obtained using a line transformer which has the characteristics shown in Table 3. Refer to Figure 2.)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
TTCF	Transmit clock repetition period			648		nsec
TTC	Transmit clock pulse width			324		nsec
TTCNT	Transmit clock negative transition time				10	nsec
TTCPT	Transmit clock positive transition time				10	nsec
TTPDS TTNDS	Transmit data set-up time		15			nsec
TTPDH TTNDH	Transmit data hold time		0			nsec
TTPL	Transmit positive line pulse width	See Note 1	TTC-5		TTC+5	nsec
TTNL	Transmit negative line pulse width	See Note 1	TTPL-5		TTPL+5	nsec
POL	Transmit line pulses power level	See Note 2				
	Transmit line pulses waveshape	See Notes 2 & 3				

Note 1: Measured at transformer with minimum line equalization

Note 2: Characteristics are in accordance with AT&T Compatibility Bulletin 119, Table 1, and Table 2 or Table 3, for line lengths and equalizer settings as shown in Table 1 of this document.

Note 3: Characteristics are in accordance with Table 2 for equalizer settings shown therein.

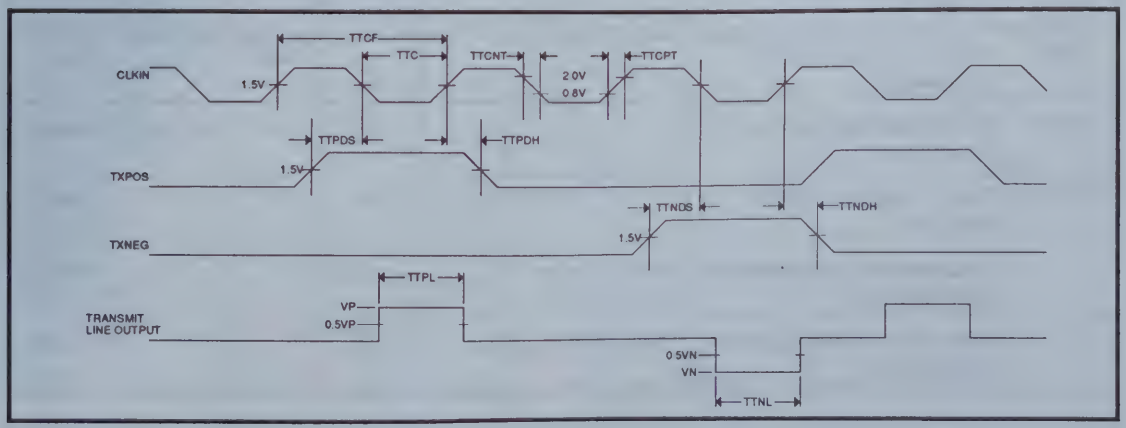


FIGURE 2: Transmit Waveforms

DYNAMIC CHARACTERISTICS AND TIMING, RECEIVER

(T_A = 0°C to 70°C, V_{CC} = 5V ± 5%, unless otherwise specified. External component values as specified in Recommended Operating Conditions; see Note 1. Refer to Figure 3.)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
VIN	Input signal voltage		±1.5		±3.7	Vpk
VLOS	Loss-of-signal indicating voltage		±0.5		±1.0	Vpk
TLOS	Loss-of-signal delay time	Timed from removal of input signal; See Note 2	0.7TPK		1.3TPK	sec
VDTH	Receive data detection threshold	Relative to peak amplitude	65		75	%
TSTAB	Receiver stabilization time	After application of input signal			5	msec
TRCF	Receive clock period			648		nsec
TRC	Receive clock pulse width			324		nsec
TRCPT	Receive clock positive transition time	C_L = 15 pF			15	nsec
TRCNT	Receive clock negative transition time	C_L = 15 pF			10	nsec
TRDP TRDN	Positive or negative receive data pulse width			648		nsec
TRDPS TRDNS	Receive data set-up time		290			nsec
TRDPH TRDNH	Receive data hold time		290			nsec
TRBV	Receive bipolar violation pulse width			648		nsec
TRBVS	Receive bipolar violation set-up time		290			nsec
TRBVH	Receive bipolar violation hold time		290			nsec
	Receive input jitter tolerance high frequency	sine, 10 KHz to 100 KHz	±100			nsec
	Receive input jitter tolerance low frequency	sine, 300 Hz or less	±4			µsec

DYNAMIC CHARACTERISTICS AND TIMING, RECEIVER (Continued)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
KD	Clock Recovery Phase Detector Gain	(All 1's Data Pattern)	62		75	µA/Rad
KO	Clock Recovery Phase Locked Oscillator Control Gain		0.15		0.20	Megrad/ sec. Volt
Note 1: Input signal is transformer coupled, and in accordance with AT&T Compatibility Bulletin 119, Table 1, and Table 2 or Table 3; also, as attenuated by 0 to 655 feet of ABAM* cable.						
Note 2: TPK = RPK x CPK x ln((VIN + 1.2V)/(VLOS + 1.2V))						
* ABAM is the trade name for 22-gauge twisted-pair cable manufactured by AT&T.						

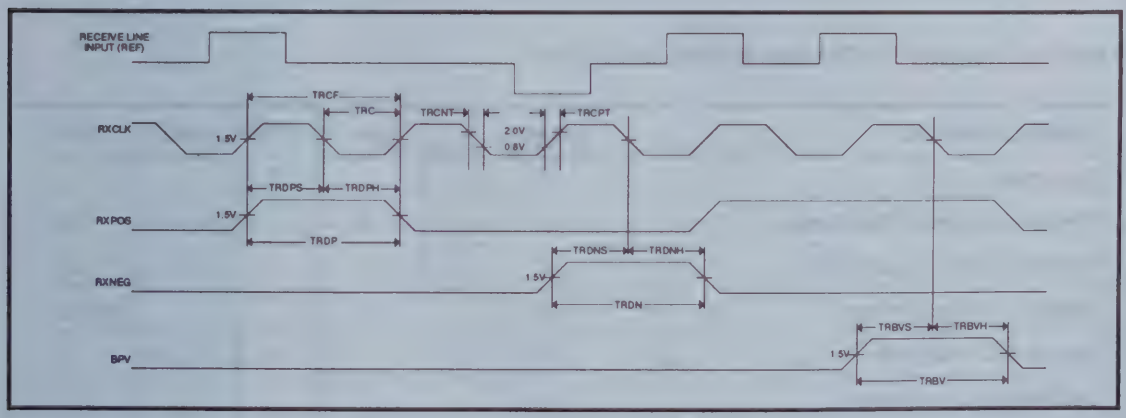


FIGURE 3: Receive Waveforms

TABLE 1: Equalizer Settings for Standard DSX-Level (3V-Peak Nominal) Pulses Versus ABAM Cable Length

CABLE LENGTH IN FEET	EQUALIZER SETTING		
	EQL0	EQL1	EQL2
0 to 50	0	0	0
51 to 131	1	0	0
131 to 262	0	1	0
262 to 393	1	1	0
393 to 524	0	0	1
524 to 655	1	0	1
Note: Equalizer settings may vary slightly at short line lengths.			

TABLE 2: Equalizer Settings for Non-DSX-Level (6V-Peak Nominal) Pulses

PULSE CHARACTERISTICS	EQUALIZER SETTING		
	EQL0	EQL1	EQL2
Rectangular 6.0 ± 0.6V pulse, 10% to 40% trailing edge overshoot	0	1	1
Rectangular 6.0 ± 0.6V pulse, less than 10% trailing edge overshoot	1	1	1
Note: Output waveform at transformer secondary; terminated in 100Ω load.			

TABLE 3: Transmit Line Transformer Characteristics

CHARACTERISTIC	SYMBOL	MIN	NOM	MAX	UNIT
Turns ratio	N		1CT:1		
Primary open circuit inductance	Lp	1.25			mH
Primary leakage inductance	L1			2.0	µH
Primary volt-time product	ET	10			V-µsec
Primary DC resistance	Rp			1.0	Ω
Secondary DC resistance	Rs			1.0	Ω
Effective primary distributed capacitance	C'			15	pF

TABLE 4: Recommended Transmit Line Transformers

MANUFACTURER	PART NO.
AIE Magnetics	318-0765
AT&T	2745 AG
Pan-Mag (Tamura Corporation of America)	PHT-019
Pulse Engineering	PE 64936

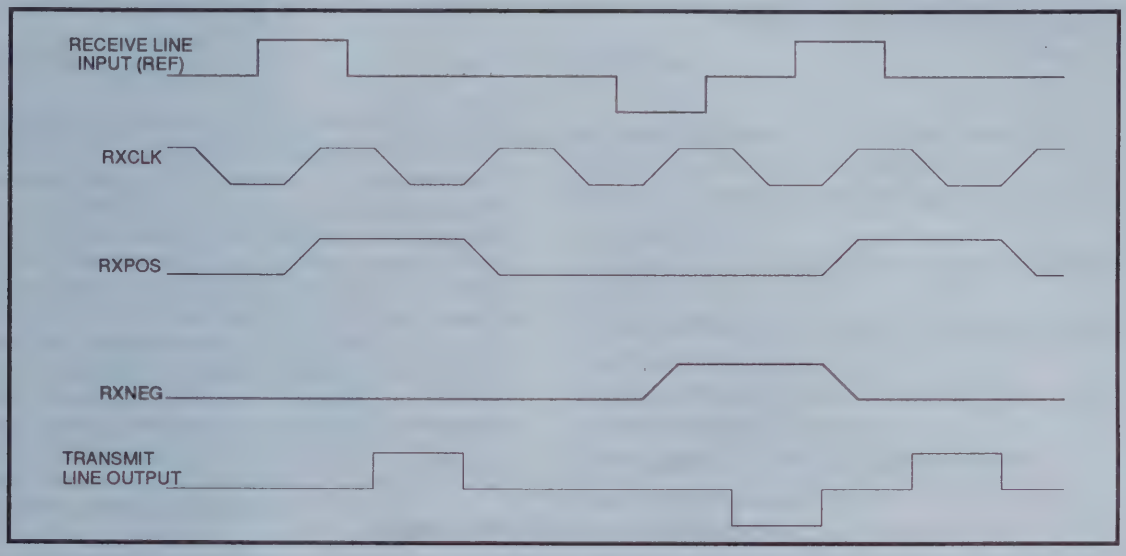


FIGURE 4: Line Loopback Waveforms

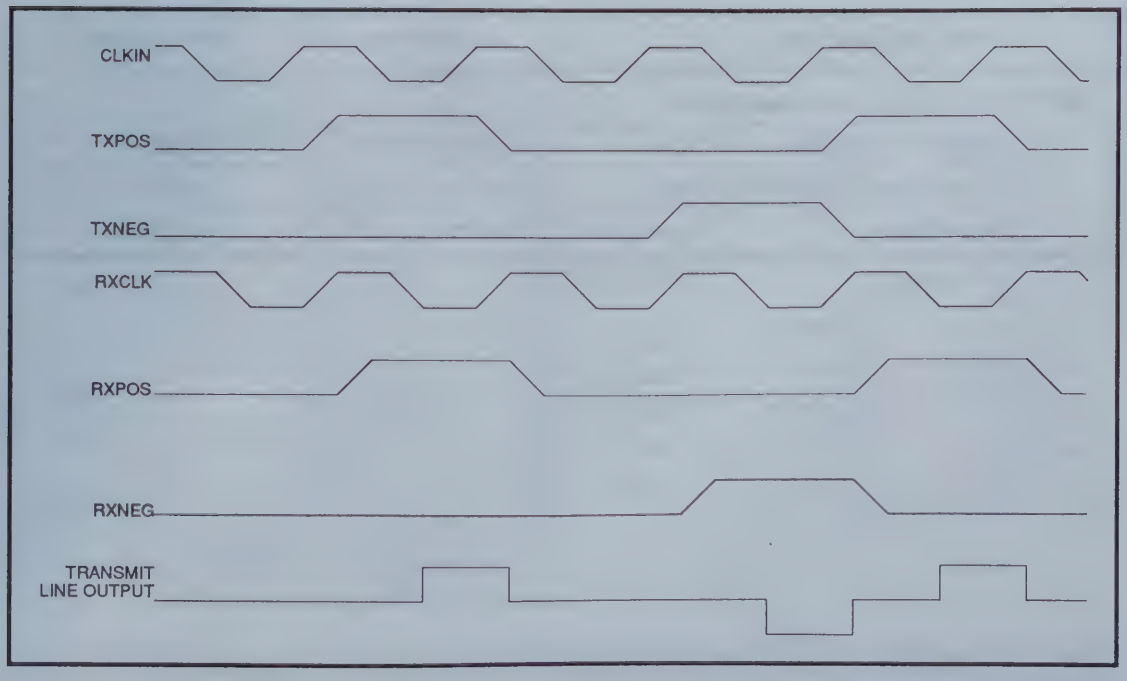
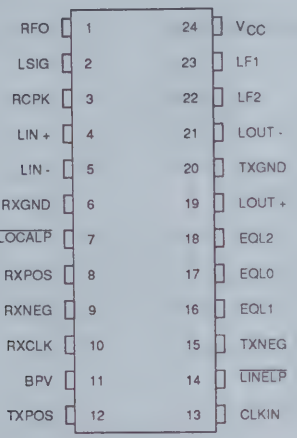


FIGURE 5: Local Loopback Waveforms

SSI 78P233
DS-1 Line Interface

PACKAGE PIN DESIGNATIONS
(TOP VIEW)



PIN DIAGRAM FOR ALL PACKAGES

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 78P233, DS-1 Line Interface - 24-Pin		
Standard Width Plastic DIP (600 mil)	SSI 78P233-CP	78P233-CP
Narrow Width Plastic DIP (300 mil)	SSI 78P233-CS	78P233-CS
Small Outline	SSI 78P233-CL	78P233-CL

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SSI 78P234
2048 KBit/s PCM Interface Unit

June, 1989

DESCRIPTION

The SSI 78P234 PCM Interface Unit is a bipolar integrated circuit which performs the functions of receiving and transmitting PCM signals in an Alternate-Mark-Inversion (AMI) format. The receiver accepts AMI-format line data and provides separated and synchronized TTL-level data and clock outputs. High-density bipolar three-encoded (HDB3) signals are passed through the chip transparently. The transmitter accepts TTL-level data and clock, typically HDB3-encoded, and produces AMI-format pulses of the appropriate shape for transmission. A loopback multiplexer is also provided that permits interchange of the signals between the sections. The SSI 78P234 requires a single 5V supply, and is available in both 20-pin DIP and small outline (SO) packages.

FEATURES

- High-performance, low-cost solution for 2048 KBit/s PCM interface applications
- Both transmit and receive circuitry in a compact, 20-pin package
- Compliant with CCITT recommendations G.703 and G.823
- Unique clock-recovery circuit, requires no crystals or tuned components
- Standard unipolar TTL-level clock and data ports for easy equipment interface
- Line-loopback and local-loopback control
- Loss-of-signal indication
- Available in SO or dual-in-line packages

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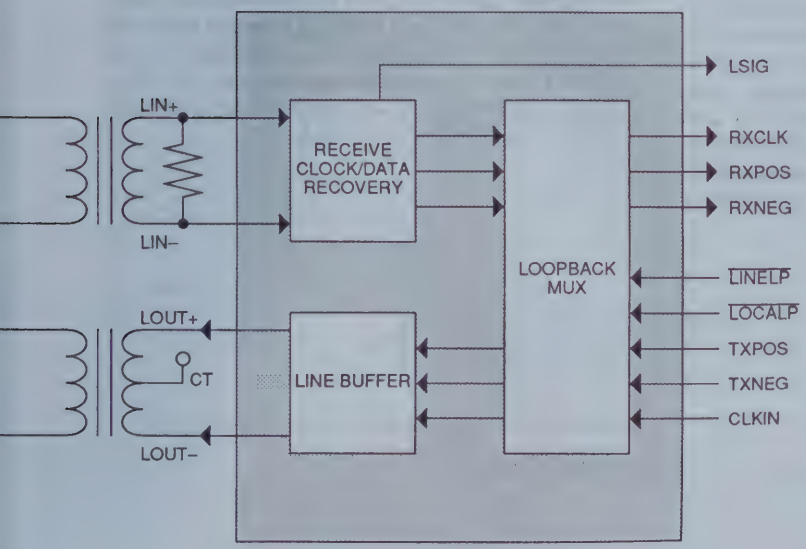
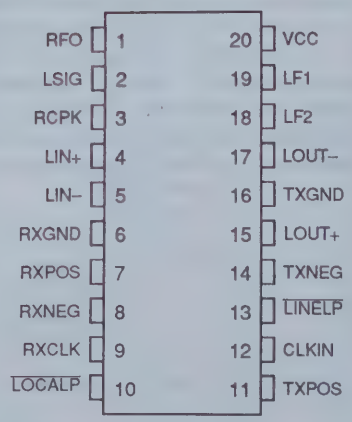
BLOCK DIAGRAM



PIN DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

FUNCTIONAL DESCRIPTION

The device consists of receiver and transmitter sections together with a "loopback" means which permits interchange of signals between the sections (see Figure 1).

RECEIVER

The receiver input is normally transformer-coupled to the source of encoded alternate polarity pulses. To provide a tracking threshold for amplitude-detecting these pulses, the signal is peak detected and a fixed percentage of the peak value is applied to the comparators which detect individual positive and negative pulses. An external R-C network is required to provide the proper storage of the peak reference value. Should the detected peak value fall below an acceptable level, the Loss of Signal (LSIG) output becomes active. This output may be used as a logical control signal or is able to drive a fault indicator LED directly.

Outputs of the data comparators are connected to the clock recovery circuits. The clock recovery system employs a unique phase-locked-oscillator loop which has an auxiliary frequency-sensitive acquisition loop which is active only when cycle-slipping occurs between the received signal rate and the internal oscillator. This system permits the loop to independently lock to the frequency and phase of the incoming data stream without the need for high-precision and/or adjustable oscillators or tuned circuits. Non-precision external components are required, however, to establish the oscillator center frequency and loop bandwidth. The phase-locked reference oscillator is employed to strobe the detected data into output latches and is also available as an output for externally synchronizing the data.

TRANSMITTER

The transmitter combines unipolar logical inputs with an input clock to provide positive and negative output pulses onto a transformer-coupled line. Note that the transmitter output pulse widths are determined by the input clock width, so that it must be carefully controlled to provide acceptable outputs.

The transmitter pulse selection logical function is arranged so that the simultaneous occurrence of both positive and negative transmit data inputs inhibits the output driver. Moreover, the driver has a current-limiting feature which protects the circuit in the event of a shorted load or inadvertent shorting of an output to the supply voltage.

LOOPBACK CONTROL SECTION

The loopback control section is essentially a multiplexer which is capable of directing received data and clock to the transmitter section, or directing transmit input data and clock to the receiver outputs. This "looping" is controlled by two active low logic signals, $\overline{\text{LINELP}}$ and $\overline{\text{LOCALP}}$, respectively.

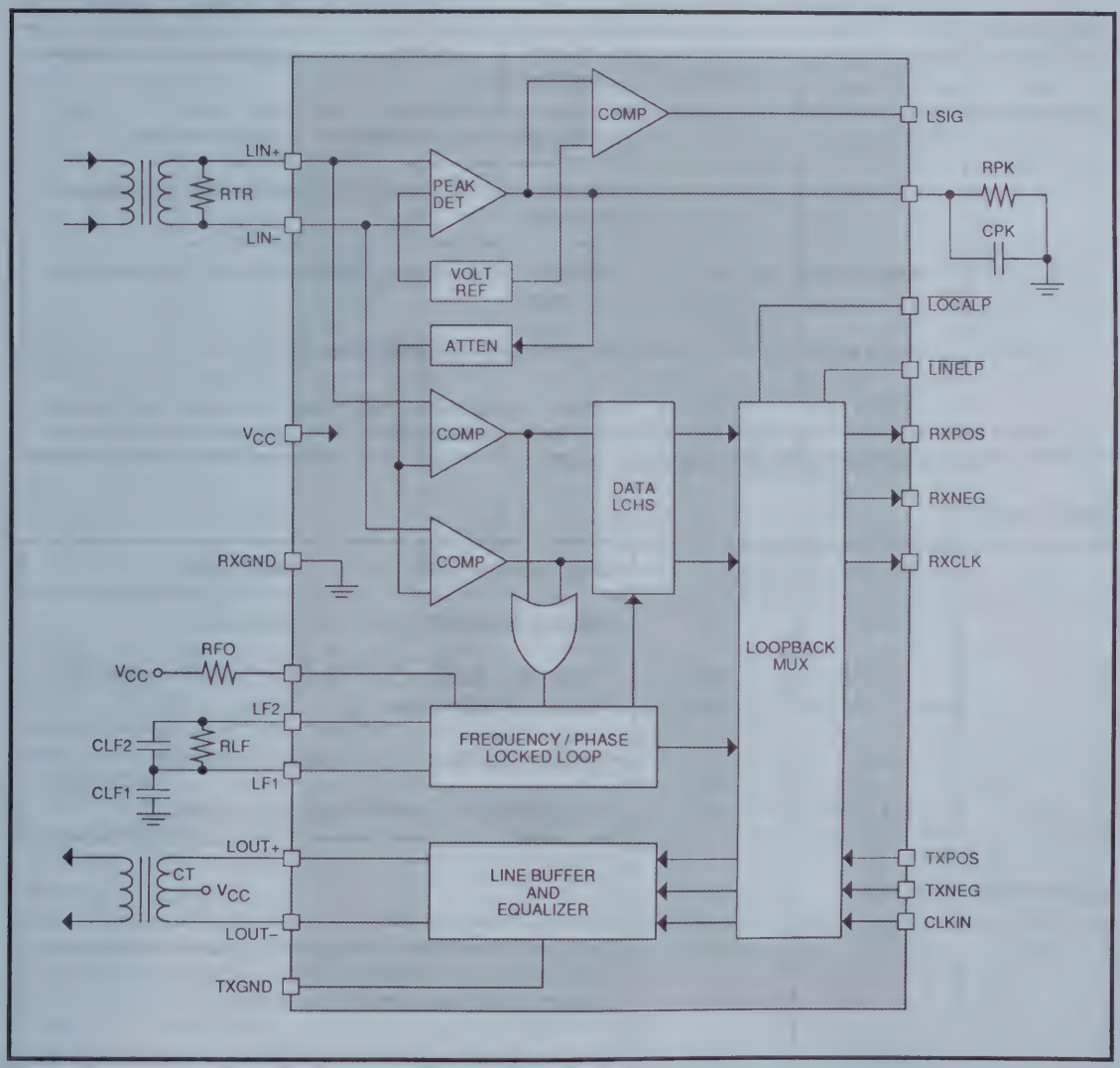


FIGURE 1: SSI 78P234 Functional Diagram

PIN DESCRIPTION

RECEIVER

I/O	LABEL	PIN NO.	DESCRIPTION
I	LIN+, LIN-	4, 5	Differential inputs, transformer-coupled from line.
O	RXPOS	7	Unipolar receiver output, active as result of positive pulse at inputs.
O	RXNEG	8	Unipolar receiver output, active as result of negative pulse at inputs.
O	RXCLK	9	Clock pulses recovered from line data.
O	LSIG	2	Loss-of-signal output indicating that input signal is less than threshold value.

TRANSMITTER

I	TXPOS	11	Unipolar transmitter data input, active high.
I	TXNEG	14	Unipolar transmitter data input, active high.
I	CLKIN	12	Transmitter clock input. Controls transmit pulse width. Transmit is active when low.
O	LOUT+	15	Output to transformer for positive data pulses.
O	LOUT-	17	Output to transformer for negative data pulses.

LOOPBACK CONTROL

I	$\overline{\text{LINELP}}$	13	Low level causes receiver recovered data and clock to be connected to the transmitter. Data and clock continue to be present at receiver outputs.
I	$\overline{\text{LOCALP}}$	10	Low level causes transmitter input data and clock to be connected to the receiver outputs. Input data continues to be transmitted.

PIN DESCRIPTION (Continued)

EXTERNAL COMPONENT CONNECTION

I/O	LABEL	PIN NO.	DESCRIPTION
I	RFO	1	Resistor connected to V_{CC} to provide basic center frequency of receiver phase locked loop oscillator.
-	LF1 LF2	19 18	Resistor-capacitor loop filter network to RXGND to establish bandwidth of phase locked loop.
-	RCPK	3	Parallel resistor-capacitor network connected to RXGND to determine charge/discharge characteristics of peak detector.

POWER

-	V_{CC}	20	Positive supply terminal for receiver circuits.
-	RXGND	6	Ground terminal for receiver circuits.
-	TXGND	16	Ground terminal for transmitter driver circuits.

ABSOLUTE MAXIMUM RATINGS

(T_A = 0°C to 70°C, V_{CC} = 5V ± 5%, unless otherwise noted. Operation above absolute maximum ratings may permanently damage the device.)

PARAMETER	RATING	UNIT
V_{CC}, Supply Voltage	-0.5 to +7.0	V
Storage Temperature	-65 to 130	°C
Soldering Temperature (10 sec.)	260	°C
Voltage Applied to Logic Inputs	-0.5 to +7.0	V
Maximum Power Dissipation	600	mW
Junction Operating Temperature	0 to +130	°C

NOTE: All inputs and outputs are protected from static charge using built-in, industry standard protection devices and all outputs are short-circuit protected.

RECOMMENDED OPERATING CONDITIONS

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Ta	Ambient temperature		0		70	°C
V_{CC}	Power supply voltage		4.75		5.25	V
VIH	High-level input voltage		2.0			V
VIL	Low-level input voltage				0.8	V
IOH	High-level output current	LSIG pin only; VO = 1.5V	-7		-13	mA

EXTERNAL COMPONENTS (Refer to Figure 1 for location of components.)

RFO	Loop center frequency resistor			6.04		KΩ
RLF	Loop filter resistor			10		KΩ
CLF1	Loop filter capacitor			0.015		µF
CLF2	Loop filter capacitor			200		pF
RPK	Peak-detector resistor			36		KΩ
CPK	Peak-detector capacitor		0.0015	0.015	0.15	µF
	Transmit line transformer	Refer to Table 1		---		---

D. C. ELECTRICAL CHARACTERISTICS

(T_A = 0°C to 70°C, V_{CC} = 5V ± 5%, unless otherwise specified.)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
ICC	Supply current	All outputs open			100	mA
IIH	High-level input current	VIH = 2.7V			20	µA
IIL	Low-level input current	VIL = 0.4V			-0.36	mA
VOH	High-level output voltage	IOH = -400µA	2.7			V
VOL	Low-level output voltage	IOL = 4.0mA; IOL = 2.0 mA, LSIG pin			0.4	V
RIN	Receiver input resistance		800		1250	Ω

DYNAMIC CHARACTERISTICS AND TIMING, TRANSMITTER

(T_A = 0°C to 70°C, V_{CC} = 5V ± 5%, unless otherwise specified. Transmit pulse characteristics are obtained using a line transformer which has the characteristics shown in Table 1, and with the appropriate resistive load. Refer to Figure 2.)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
TTCF	Transmit clock repetition period			488		nsec
TTC	Transmit clock pulse width			244		nsec
TTCNT	Transmit clock negative transition time				10	nsec
TTCPT	Transmit clock positive transition time				10	nsec
TTPDS TTNDS	Transmit data set-up time		15			nsec
TTPDH TTNDH	Transmit data hold time		0			nsec
TTPL	Transmit positive line pulse width	Measured at transformer	TTC-5		TTC+5	nsec
TTNL	Transmit negative line pulse width		TTPL-5		TTPL+5	nsec
	Transmit line pulses waveshape	See Note				

Note: Characteristics are in accordance with Table 6 and Figure 15 of Rec. G.703.

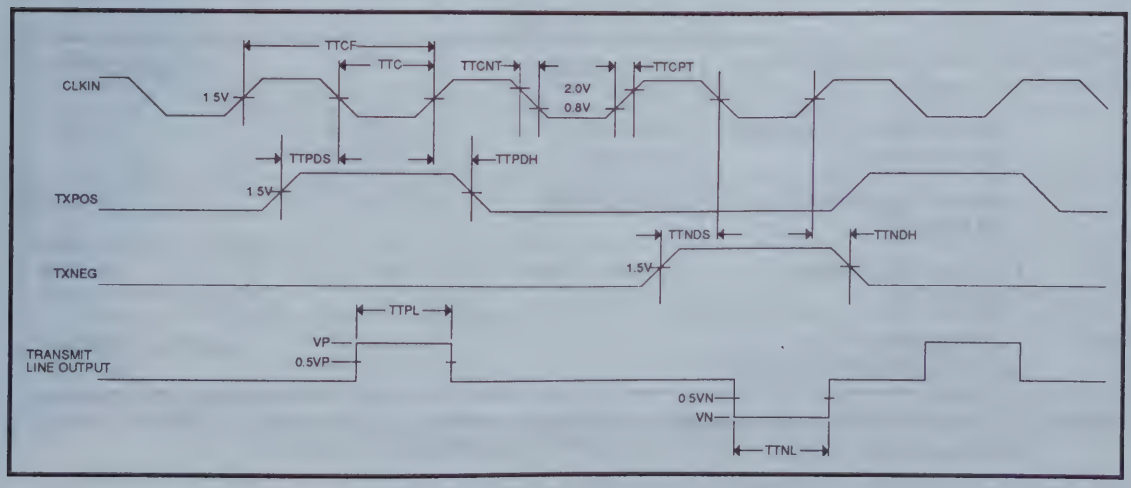


FIGURE 2: Transmit Waveforms

DYNAMIC CHARACTERISTICS AND TIMING, RECEIVER

(T_A = 0°C to 70°C, V_{CC} = 5V ± 5%, unless otherwise specified. External component values as specified in Recommended Operating Conditions; see Note 1. Refer to Figure 3.)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
VIN	Input signal voltage		±1.2		±3.9	Vpk
VLOS	Loss-of-signal indicating voltage		±0.5		±1.0	Vpk
TLOS	Loss-of-signal delay time	Timed from removal of input signal; See Note 2	0.7TPK		1.3TPK	sec
VDTH	Receive data detection threshold	Relative to peak amplitude	35		45	%
TSTAB	Receiver stabilization time	After application of input signal			5	msec
TRCF	Receive clock period			488		nsec
TRC	Receive clock pulse width			244		nsec
TRCPT	Receive clock positive transition time	C_L = 15pF			15	nsec
TRCNT	Receive clock negative transition time	C_L = 15pF			10	nsec
TRDP TRDN	Positive or negative receive data pulse width			488		nsec
TRDPS TRDNS	Receive data set-up time		210			nsec
TRDPH TRDNH	Receive data hold time		210			nsec
	Receive input jitter tolerance high frequency	sine, 18KHz to 100KHz	±100			nsec
	Receive input jitter tolerance low frequency	sine, 2.4 KHz	±750			nsec
KD	Clock Recovery Phase Detector Gain	(All 1's Data Pattern)	62		75	µA/Rad
KO	Clock Recovery Phase Locked Oscillator Control Gain		0.40		0.55	Megrad/ sec. Volt

Note 1: Input signal is transformer coupled. In accordance with Paragraph 6.3 of Rec. G.703 and Table 2 of Rec. G.823.

Note 2: TPK = RPK x CPK x ln((VIN + 1.2v)/(VLOS + 1.2v))

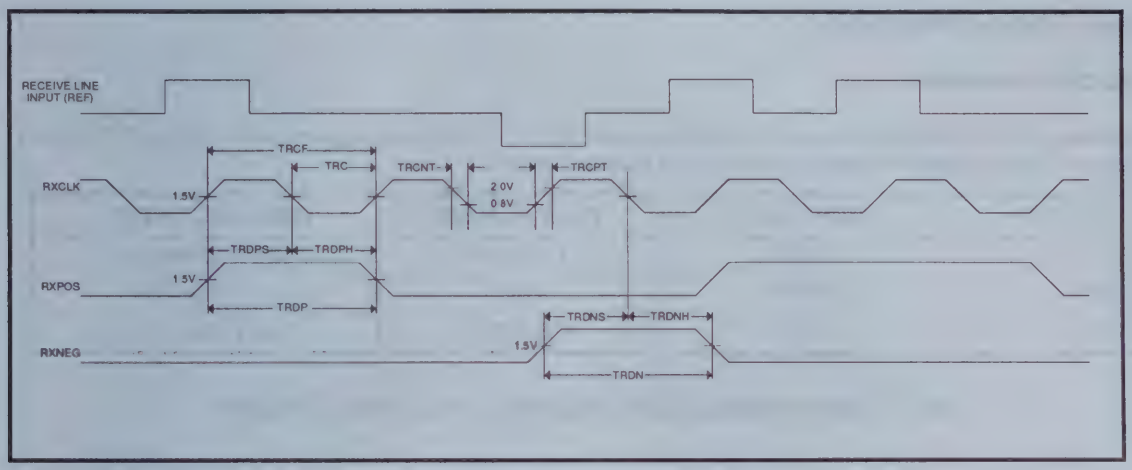


FIGURE 3: Receive Waveforms

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LINE TRANSFORMERS

The SSI 78P234 is designed to connect to 75Ω coaxial or 120Ω symmetrical pair cabling. The transmitter must meet output pulse characteristics as specified by the CCITT (Table 6 of Rec. G.703) for each of these transmission media. It is important to choose a transformer that meets the specifications shown in Table 1 (below) to assure compliance with these requirements.

CHARACTERISTIC		SYMBOL	MIN	NOM	MAX	UNIT
Turns ratio	75Ω coax	N		2.53CT:1		
	120Ω twisted pair			2CT:1		
Primary open circuit inductance		Lp	3			mH
Primary leakage inductance		L1			4.0	µH
Primary volt-time product		ET	5			V-µsec
Primary DC resistance		Rp			2.5	Ω
Interwinding Capacitance		C_w			25	pF

TABLE 1: Transmit Line Transformer Characteristics

LINE TRANSFORMERS (cont.)

75Ω Coax Connection

Approximate turns ratios for connection to 75Ω coax are: 2.53 CT:1 for the transmitter and 1:1.26 (no CT) for the receiver. Some recommended transformers are listed in Table 2.

RCV/XMIT	TURNS RATIO	PART NUMBER	MANUFACTURER
XMIT	2.53CT:1	PE 64945	Pulse Engineering
XMIT	2.66CT:1	11816	Schott Corporation
RCV	1:1.26	PE 64949	Pulse Engineering

TABLE 2: Recommended Line Transformers for 75Ω Coax Connection

120Ω Symmetrical Pair Connection

Connection to 120Ω symmetrical pair requires a 2CT:1 ratio for the transmitter and 1:1 (no CT) on the receiver. Some recommendations are listed below.

RCV/XMIT	TURNS RATIO	PART NUMBER	MANUFACTURER
XMIT	2CT:1	1323	BH
XMIT	2CT:1	G52J12C	Pan-Mag
XMIT	2CT:1	11815	Schott Corporation
XMIT	1:1:1	PE 64931	Pulse Engineering
RCV	1:1	PE 64934	Pulse Engineering
RCV	1:1:1	G52J111P	Pan-Mag

TABLE 3: Recommended Line Transformers for 120Ω Symmetrical Pair Connection

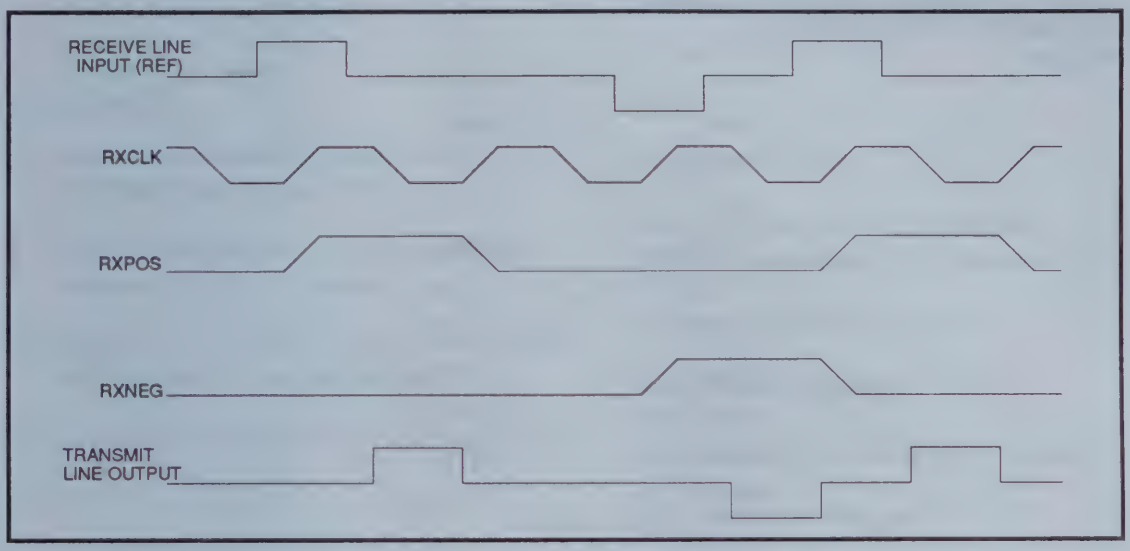


FIGURE 4: Line Loopback Waveforms

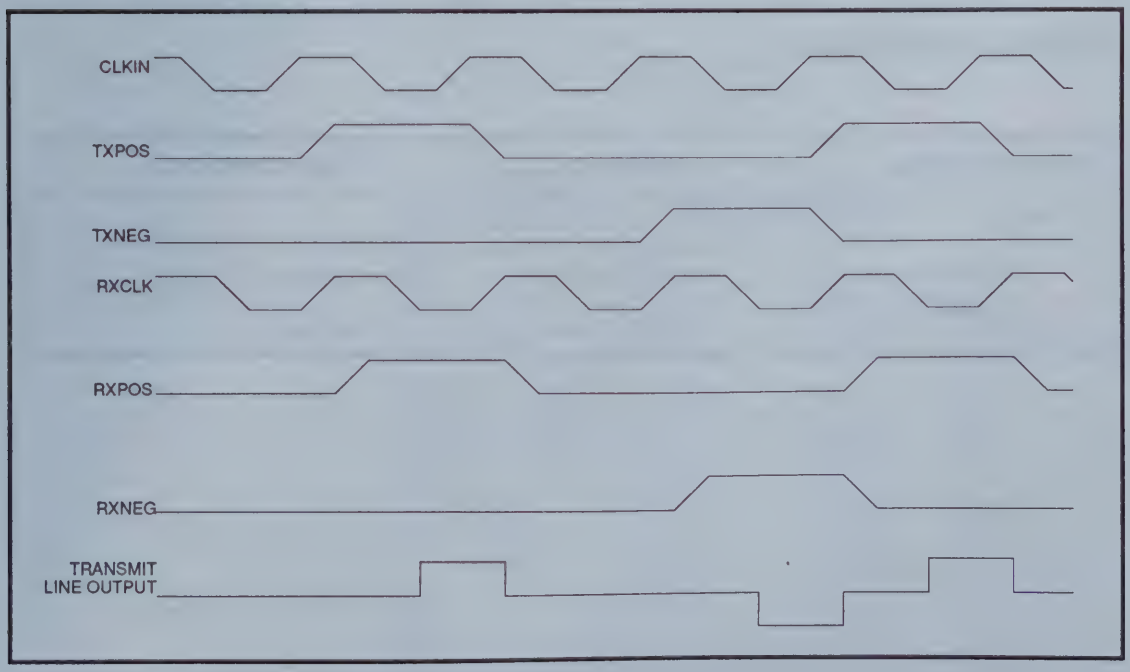
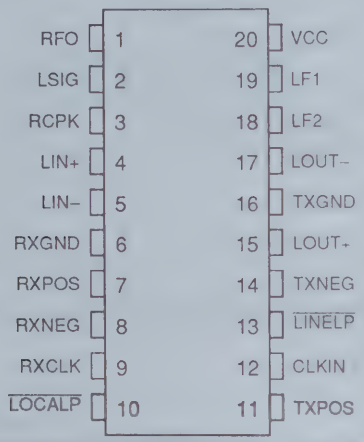


FIGURE 5: Local Loopback Waveforms

SSI 78P234
2048 KBit/s
PCM Interface Unit

PACKAGE PIN DESIGNATIONS
(TOP VIEW)



20-Pin DIP, SO

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PACKAGE MARK
SSI 78P234		
20-Pin Plastic DIP	SSI 78P234-CP	78P234-CP
20-Pin SO	SSI 78P234-CL	78P234-CL

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silicon systems®

SSI 78P236
DS-3 Line Interface

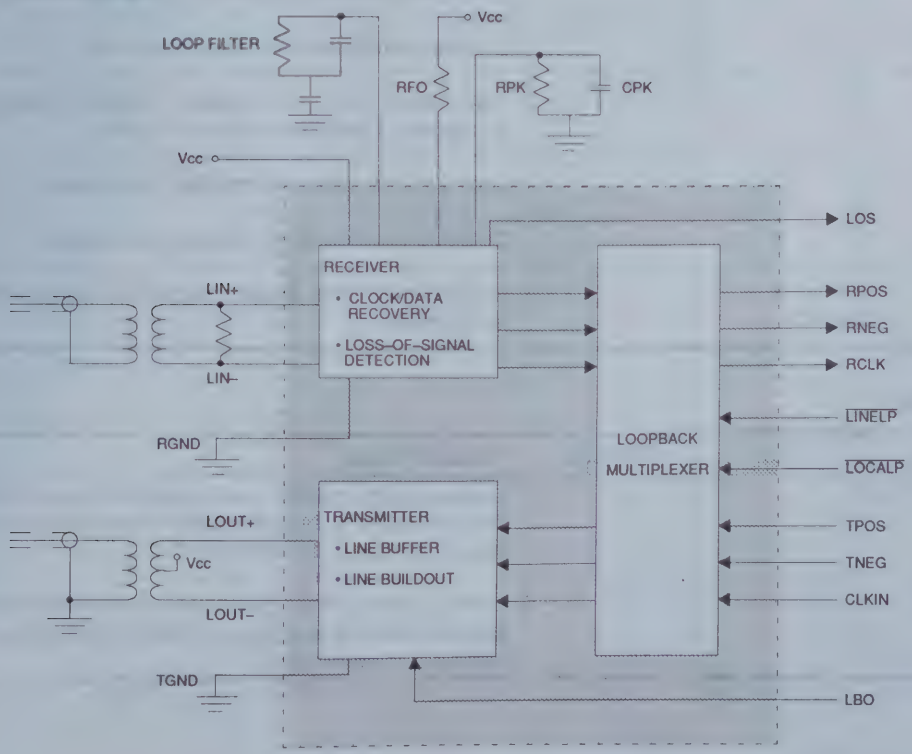
Advance Information

Available Q1, 1990 July, 1989

FEATURES

- Single chip transmit and receive interface for DS-3 (44.736 Mbit/s) applications
- Unique clock recovery circuit, requires no crystals or tuned components
- Selectable transmit line buildout to accommodate varying line lengths
- Standard unipolar POS and NEG data and CLK ports
- CMOS logic interface
- Compliant with AT&T Compatibility Bulletin 119 and Bellcore Technical Reference 000009
- Line and local loopback control
- Loss of signal indication
- Available in DIP or surface mount packages
- Single 5 volt power supply

BLOCK DIAGRAM



5

CAUTION: Use handling procedures necessary for a static sensitive component.

PIN DESCRIPTION

RECEIVER

LABEL	I/O	PIN NO.	DESCRIPTION
LIN+, LIN-	I		Differential inputs, transformer-coupled from line.
RPOS	O		Unipolar receiver output, active as result of positive pulse at inputs.
RNEG	O		Unipolar receiver output, active as result of negative pulse at inputs.
RCLK	O		Clock pulses recovered from line data.
LOS	O		Loss of signal output indicating that input signal is less than threshold value.

TRANSMITTER

TPOS	I		Unipolar transmitter data input, active high.
TNEG	I		Unipolar transmitter data input, active high.
CLKIN	I		Transmitter clock input. Negative transition initiates output data pulse. Controls transmit pulse width.
LOUT+	O		Output to transformer for positive data pulses.
LOUT-	O		Output to transformer for negative data pulses.
LBO	I		Line buildout control. Selected for shorter cable lengths (to be specified).

CONTROL

LABEL	I/O	PIN NO.	DESCRIPTION
$\overline{\text{LOCALP}}$	I		Local loopback control. Low level causes transmitter input data and clock to be connected to the receiver outputs. Input continues to be transmitted.
$\overline{\text{LINELP}}$	I		Line loopback control. Low level causes receiver input data and clock to be connected to the transmitter outputs. Input continues to be received.

EXTERNAL COMPONENT CONNECTION

LABEL	I/O	PIN NO.	DESCRIPTION
RFO	I		Resistor connected to Vcc to provide basic center frequency of receiver phase locked loop oscillator.
LF	-		Resistor-capacitor loop filter network to RXGND to establish bandwidth of phase locked loop.
RCPK	-		Parallel resistor-capacitor network connected to RXGND to determine charge/discharge characteristics of peak detector.

POWER

Vcc	-		Positive supply terminal for receiver circuits.
RGND	-		Ground terminal for receiver circuits.
TGND	-		Ground terminal for transmitter driver circuits.

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NOTES:

Section 6

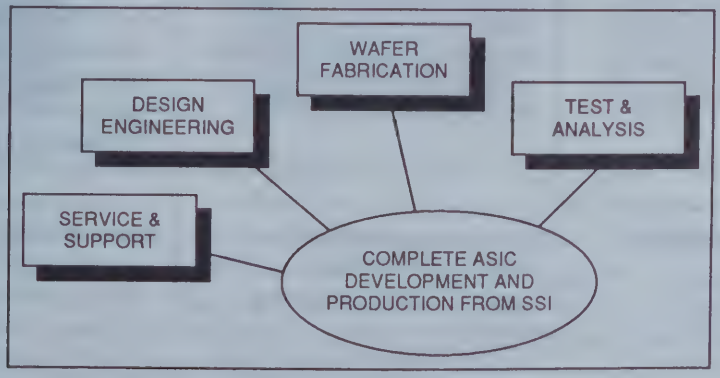
CUSTOM/ SEMICUSTOM CAPABILITIES

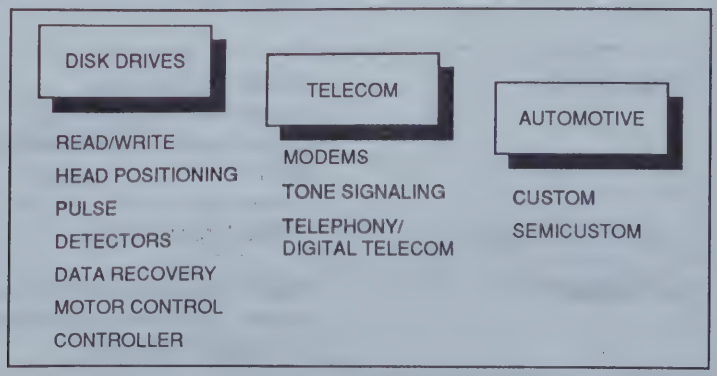
SILICON SYSTEMS LEADS THE WAY DEVELOPING MIXED-SIGNAL CUSTOM/SEMICUSTOM PRODUCTS

Silicon Systems is committed to leadership in the development of high-performance, mixed-signal custom/semicustom application-specific integrated circuits (ASICs).

Silicon Systems offers innovative designs for digital, analog, and mixed analog/digital ICs; a versatile range of CMOS and bipolar processes; quick-turn design methodologies supported by advanced and integrated design automation tools; specialized manufacturing facilities; comprehensive test, quality assurance, and prototype assembly programs; and, of course, greater than 15 years of IC design experience. SSi's efforts pay off by dramatically reducing the time (and cost) it takes to deliver the most optimized custom/semicustom ICs available.

Whether a customer's application falls in SSi's specialty areas of communications, microperipherals, automotive, or other areas, SSi's technical capabilities turn designs around faster and minimize a product's time to market for the competitive advantage.





BROAD RANGE OF ANALOG AND DIGITAL DESIGN EXPERIENCE

With a broad base of experience, systems knowledge, and applications expertise, SSi's designers provide creative IC solutions in both CMOS and bipolar process technologies for analog, digital, and mixed-signal applications.

In CMOS, SSi has designed digital products ranging from FIFOs to complex hard-disk drive controllers. Combined analog/digital products range from cross-point switches to complete, single-chip 2400 BPS modems.

In bipolar, SSi's design expertise focuses on applications requiring high-speed ECL logic combined with high-performance analog circuitry. Bipolar products range from low-noise amps to very sophisticated data separators that employ patented phase locked loops.

TECHNIQUE	APPLICATION	SSi-DESIGNED EXAMPLES
CMOS Signal Processing	For analog continuous time and sampled data (switched-capacitor implementation) and Digital Signal Processing (DSP) applications. Low-power capability also allows inclusion of ROMs, RAMs, and other analog/digital subsystems.	-K224 complete single-chip 2400 BPS modem -C301 single-chip telephone headset amplifier -14.4 KBit modem -Direct-broadcast satellite descrambler -Motor controllers -Hi-resolution analog data acquisition
Bipolar Signal Processing	For high-performance, low noise, wideband signal acquisition and processing applications. Offers TTL and/or ECL logic interfaces with high current drive.	-Sub 1 nV/$\sqrt{Hz}$ HDD R/W amplifiers -AGC, pulse detection amplifiers -High-speed data separators -Wideband transceivers -PLLs (Phase Locked Loops) -Optical signal processing
Digital CMOS	For ASIC controllers, sequencers and data path applications with on-board ROM, RAM, and PLA sub-systems. Offers standard TTL and/or CMOS logic interfaces.	-Hard disk drive controllers -SCSI interface controllers -UARTs -Protocol controllers -Digital signal processors
Digital Bipolar	High-speed logic and interface circuitry. Offers standard logic or custom interfaces.	-Encoders and decoders -High-speed digital transceivers

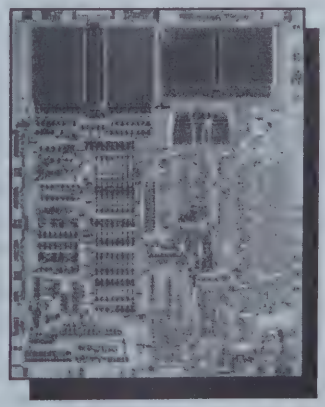
FULL ANALOG AND DIGITAL INTEGRATION ON THE SAME CHIP

Silicon Systems leads its competition in the design of complete systems on a chip which combine complex analog and digital functions. The total system solution approach allows designers to satisfy their application, cost, and performance objectives.

Custom mixed-signal Bipolar low-noise read/write IC

Standard Bipolar mixed-signal, high-performance data separator

Standard product single-chip 2400 BPS modem with switched capacitor filters and RISC DSP



"DESIGN-FOR-TESTABILITY" AND TEST SUPPORT

SSi employs design-for-testability methodologies, such as built-in test modes that allow direct testing of internal subsystems. SSi uses highly specialized equipment, test programs and test procedures for combined analog/digital designs to ensure delivery of high-quality product. To determine product reliability under extreme conditions, products are tested in-house by a wide variety of advanced analog or digital testers including:

- LTX (TS88/DX90) testers
- Eagle (LSI-4) testers
- Sentry 7 and Sentry 20 digital test systems

These testers are supported by:

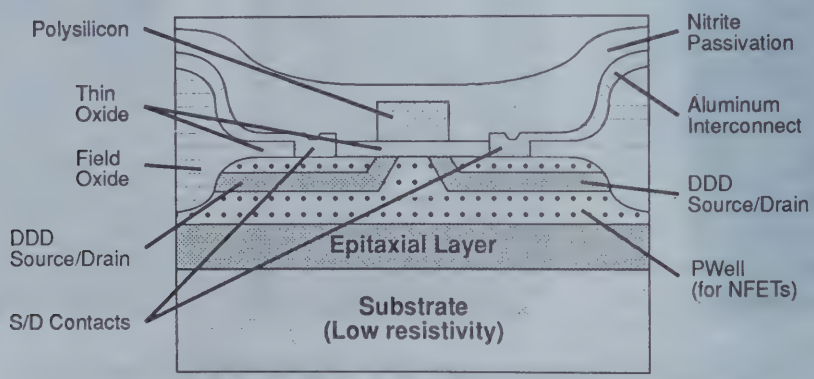
- Automatic handlers (Trigon PLCC, Symtek SOIC, and MCT and Daymarc handlers)
- Burn-in sockets, temperature chambers, Aehr burn-in ovens, and Highly Accelerated Stress Test (HAST)

CMOS TECHNOLOGIES...

SSi's state-of-the-art CMOS processes have allowed the company to become the leading supplier of systems-oriented, mixed analog/digital ASICs.

The "CH" process features a unique source/drain structure for higher voltage (12–volt) applications. Poly-poly capacitors support filtering and data conversion (A/D and D/A) applications. An epitaxial substrate provides latch-up protection for ASICs subject to adverse environments (such as motor control applications). And special poly resistors allow continuous time filters (for anti-aliasing functions) to be combined with sampled data, switched-capacitor filters, increasing the level of ASIC integration and lowering overall system manufacturing costs.

CH CMOS PROCESS TRANSISTOR



CMOS PROCESS CHART

PROCESS	TYPE/FEATURES	PRODUCTION	NEW DESIGNS	GATE SIZE (microns)	DIGITAL	ANALOG	INTERCONNECT LAYERS: PITCH (microns)	APPLICATION VOLTAGE
CB	High Voltage Metal Gate	Yes	No	7.2	Yes	Yes	Metal 1 (12.5)	18V
CF	Supports SSi 6600 Array Family only	Yes	No	4.0	Yes	Yes	Metal 1 (10.0) Poly 1 (8.0)	7V
CE	Digital CMOS, Supports Controller Group	Yes	Yes	2.0	Yes	No	Metal 1 (4.6) Metal 2 (6.0) Poly 1 (4.8)	5V
CD	Silicon Gate CMOS, High ohms/square Poly Option, Epi Substrate Available	Yes	Yes	3.5	Yes	Yes	Metal 1 (8.8) Poly 1 (5.8) Poly 2 (6.4)	12V
CH	Silicon Gate CMOS, Same Features as CD Plus Plasma (Dry) Metal Etch	Yes	Yes	3.5	Yes	Yes	Metal 1 (6.4) Poly 1 (5.8) Poly 2 (6.4)	12V
CG	Dual Poly, Dual Metal Silicon Gate	Development	Yes	1.5	Yes	Yes	Metal 1 (5.0) Metal 2 (7.6) Poly 1 (3.6) Poly 2 (5.0)	5V

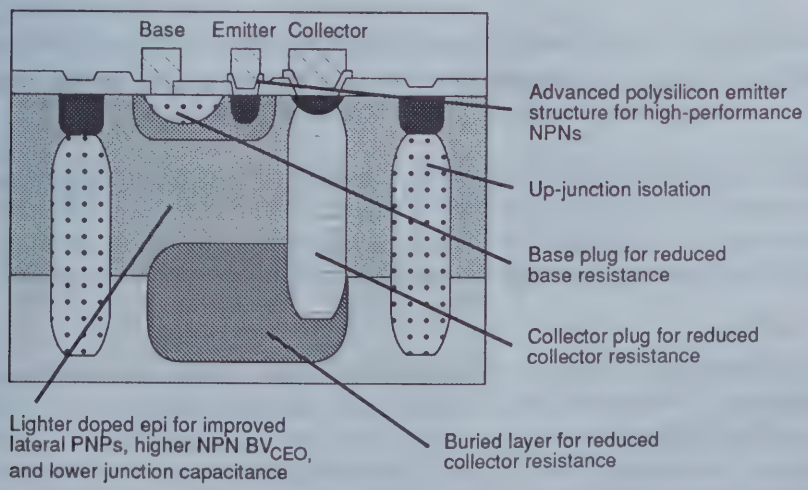
The "CG" process addresses 5-volt applications and features 1.5-micron gates and two layers of metal interconnect for high-performance digital circuitry, along with the dual poly layers required for analog circuitry. In addition to full-custom standard and customer-proprietary designs, both the "CH" and "CG" processes support a family of combined analog/digital CMOS arrays.

AND BIPOLAR TECHNOLOGIES

SSi's leading analog/digital bipolar technology is "BK," which supports the development of a wide variety of high-performance, combined analog/digital ASICs. In addition to full-custom standard and customer-proprietary designs, the "BK" process supports a family of advanced bipolar analog/digital arrays.

"BK" features a high-performance NPN (3 GHz F_T) with an operating capability of 12 BV_{CEO}. This process utilizes an advanced polysilicon emitter structure as well as base and collector plugs to reduce parasitic resistances for high-performance applications. Other key features include metal-nitride-poly capacitors, aluminum Schottky diodes, and improved lateral PNPs through the use of lighter doped epi.

BK BIPOLAR PROCESS NPN TRANSISTOR


Base
Emitter
Collector
Advanced polysilicon emitter structure for high-performance NPNs
Up-junction isolation
Base plug for reduced base resistance
Collector plug for reduced collector resistance
Lighter doped epi for improved lateral PNPs, higher NPN BVCEO, and lower junction capacitance
Buried layer for reduced collector resistance

BIPOLAR PROCESS CHART

PROCESS	TYPE/FEATURES	PRODUCTION	NEW DESIGNS	Emitter SIZE (microns)	DIGITAL	ANALOG	NPN F_T	INTERCONNECT LAYERS: PITCH (microns)	BV_{CEO} (volts)
BC	"Standard" Cut Emitter Process	Yes	No	6.0	Yes	Yes	1 GHZ	Metal 1 (14.0) Metal 2 (24.0)	12
BJ	High-Performance Polysilicon Emitter Structure	Yes	Yes	3.0	Yes	Yes	3 GHZ	Metal 1 (9.0) Metal 2 (14.0)	9
BK	Base and Collector Plugs, Improved Lateral PNPs	Yes	Yes	2.5	Yes	Yes	3 GHZ	Metal 1 (9.0) Metal 2 (14.0)	12

INTEGRATED DESIGN METHODOLOGY—THE IDM™ ADVANTAGE

Silicon Systems has spent almost 10 years developing its Integrated Design Methodology (IDM™). IDM consists of an interlocking set of design methods supported by a single Computer-Aided Engineering (CAE) and Computer-Aided Design (CAD) system. As IDM supports analog and digital designs in any of SSi's CMOS and bipolar technologies, it offers the tremendous advantage of flexibility.

COMPARE FULL-CUSTOM TO SEMICUSTOM DESIGN

IDM is based on two major design approaches: full-custom and semicustom.

Full-custom design is a "handcrafted" approach used to produce the most compact, high-performance design possible. Two approaches for full-custom physical design are possible: either composite or symbolic. In composite design, every process mask layer is drawn down to the process minimums. This yields the densest, highest-performance designs but is the most time-consuming approach. Symbolic design utilizes correct-by-construction, stick-like, process symbols, such as resistors, capacitors, and wires. Symbolic design is significantly more productive than composite and supports a higher level of circuit verification for greater design accuracy.

Semicustom design is an "automated" approach used to produce the most timely and cost-efficient designs possible. Two approaches are possible: either automatically placed-and-routed library components, including standard cells, or prefabricated array components.

SSi's analog and digital standard cells are pre-characterized, library-maintained circuits that are automatically placed and routed to generate a layout. The automatic place-and-route software also utilizes macro cell assemblers to route full-custom circuitry. The standard cell approach requires minimal layout effort, leading to lower development cost and a higher first article success rate.

SSi's mixed-signal arrays are bipolar and CMOS families of integrated circuits which are ninety percent prefabricated. The base arrays utilize a three-tile, three-segment structure each of which is targeted for a specific design application, i.e., analog, digital, and reference. The three segments forming the array core are separated by interconnect "highways" capable of handling both analog and digital signal busses. The core, in turn, is enclosed by a periphery of predefined I/O functions.

Array customization is achieved by the definition and interconnection of metal and poly-Si layers. SSi mixed-signal arrays provide a systems designer with fast prototype cycle times, lower integration costs, and the ability to migrate to either standard cell or custom integration with a minimum perturbation in design production.

CHOOSE THE OPTIMUM DESIGN APPROACH BASED ON TRADE-OFFS

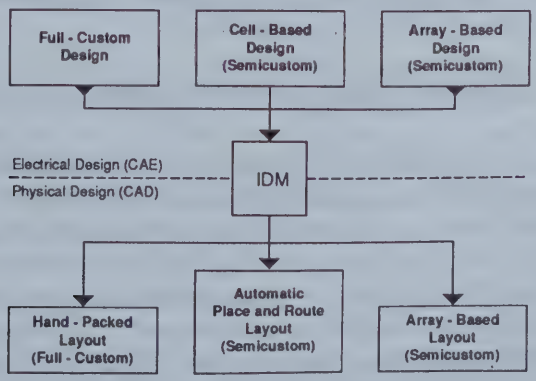
Each IDM design approach offers unique cost, time, and performance tradeoffs.

CUSTOM/SEMICUSTOM TRADE - OFFS				
	Full - Custom		Semicustom	
	Composite Design	Symbolic Design	Cell - Based Design	Array - Based Design
Design Parameters				
Cost (Non-Recurring Expense)	1.0	.50 - .80	.40 - .70	.20 - .40
Time (Schedule)	1.0	.50 - .70	.40 - .60	.20 - .40
Production Parameters				
Piece Price (Production Cost)	1.0	1.2 - 1.4	1.5 - 2.0	2.0 - 2.5
Die Size (Silicon Area)	1.0	1.1 - 1.2	1.3 - 1.6	1.6 - 2.0

NOTE: All comparisons are normalized to a composite-level design.

MIX FULL-CUSTOM AND SEMICUSTOM DESIGN ON A SINGLE CHIP

Due to the interlocking nature of SSi's design approaches, full-custom and semicustom design can be mixed on the electrical and/or physical design of any given IC.

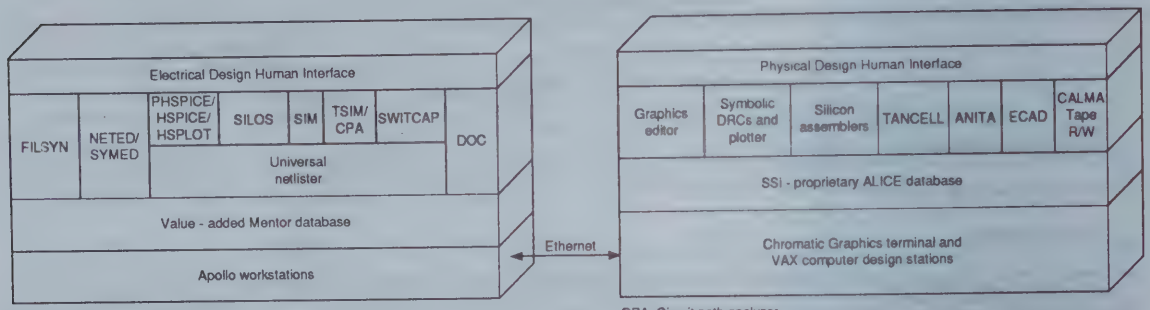

Full - Custom Design
Cell - Based Design (Semicustom)
Array - Based Design (Semicustom)
Electrical Design (CAE)
Physical Design (CAD)
IDM
Hand - Packed Layout (Full - Custom)
Automatic Place and Route Layout (Semicustom)
Array - Based Layout (Semicustom)

CONVERT SEMI-CUSTOM DESIGN INTO FULL-CUSTOM DESIGN

With its unique integrated design automation system, SSi can easily convert a semicustom design into full-custom circuitry. This capability allows SSi's customers to reduce production costs by converting an area-inefficient semicustom design into a high-performance full-custom design.

SOPHISTICATED DESIGN AUTOMATION TOOLS

The IDM™ design automation system, with proprietary and SSi-enhanced vendor software, addresses both the electrical and physical phases of design.



FILSYN: Filter circuit synthesizer
NETED/SYMED: Schematic editors
PHSPICE: HSPICE pre-processor
HSPICE: A/D circuit
HSPLOT: HSPICE graphic plotter
SILOS: Logic and fault simulator
SIM: Digital logic simulator
TSIM: Timing simulation preprocessor

CPA: Circuit path analyzer
SWITCAP: Switched-capacitor simulator
DOC: Document editor
TANCELL: Automatic placer and router
ANITA: Automated network intertrace algorithm
ECAD: Design rules checks and pattern generation
ALICE: Automated layout for IC engineering

ELECTRICAL DESIGN

Electrical design is done on Mentor Graphics/Apollo engineering workstations with SSi-enhanced software that provides schematic capture, simulation, synthesis, and documentation tools. This software is supported by libraries of pre-designed cells and components. Due to our integrated CAE environment, there is no distinction between any schematic capture, simulation, or synthesis capabilities for full- or semicustom design approaches.

ANALOG AND DIGITAL SIMULATION

Simulation ensures that we meet the customer's performance specification before converting the design into silicon. Circuit simulation, an important key to SSi's design methodology, allows us to accurately simulate the performance numbers of our technologies. For circuit simulation, we use Meta-Software's HSPICE™ with a proprietary analog CMOS model that accurately predicts output impedance and other analog parameters over a wide range of operating conditions and device sizes. The HSPICE environment includes a fully hierarchical netlister, a preprocessor called PHSPICE, and a Meta-Software graphic plotter called HSPLOT™. For the analog simulation of switched capacitors, we use Columbia University's SWITCAP™.

For digital simulation, we use a proprietary version of SimuCad's SILOS™ that performs gate and switch-level, zero-delay, functional logic and fault simulation. To analyze delays with a timing-based logic simulation, we use a combination of TSIM™ (developed on Meta-Software's Circuit Path Finder™) and SILOS.

DEVICE MODELING AND CHARACTERIZATION LABORATORY

Highly-accurate circuit simulation models and parameters are developed in SSi's state-of-the-art Device Modeling and Characterization (DMC) laboratory. With capabilities including precision AC measurement, RS1 statistical analysis, and worst-case modeling, the DMC lab provides complete device model data for our processes.

PHYSICAL DESIGN

Physical design is done on Chromatics Graphics terminal/VAX computer design stations. Our proprietary, VAX-based program called ALICE™ (Automated Layout for Integrated Circuit Engineering) with other SSi-enhanced vendor software is used for graphical editing, digitizing, design rules checking (DRC), circuit tracing, and pattern generation (PG).

AUTOMATIC PLACE AND ROUTE SOFTWARE

SSi's cell-based automatic place-and-route capability, which is based on Tangent's TANCELL™, performs physical design far more rapidly than can be done by hand. Extensive proprietary software, developed to complement TANCELL, supports hierarchical routing, parameter passing, library creation and maintenance, and CMOS switched-capacitor analog macro generation directly from full-custom design. A random-logic digital macro assembler is in development. This flexible place-and-route environment supports floorplanning, automatic chip construction, and the mix and match of custom cells, standard cells, and compiled cells—all of which are used to reduce design development time.

AUTOMATIC CIRCUIT TRACE AND VERIFICATION SOFTWARE

Using a proprietary circuit-trace program called ANITA™, we compare the completed IC layout database automatically to the Mentor schematic database to ensure that the layout implementation matches the schematic design exactly. When this trace program is applied to CMOS and bipolar mixed analog/digital designs, it performs a more detailed trace than is available through commercial layout-versus-schematic (LVS) packages. ANITA allows SSi to dramatically reduce design errors and minimize the time to product introduction.

DESIGN AUTOMATION BENEFITS

The proprietary IDM Design Automation system gives Silicon Systems the flexibility to create increasingly complex ASIC designs for our customers while dramatically reducing design schedules, costs, and errors.

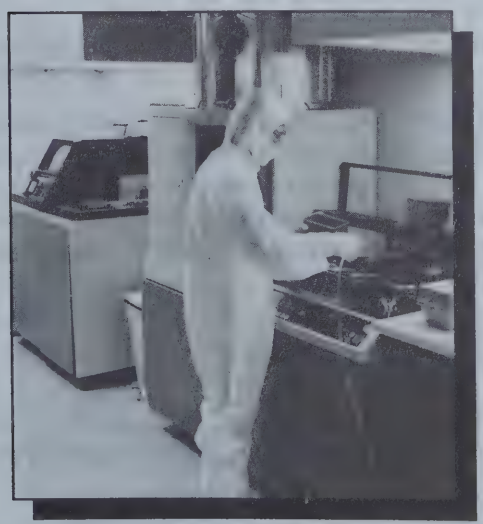
MANUFACTURING SUPPORTS BOTH CMOS AND BIPOLAR TECHNOLOGIES

Silicon Systems is known in the ASIC industry for its commitment to producing standard and custom ASICs using a broad range of CMOS and bipolar process technologies.

SSi continually invests in quality and capacity improvements to ensure that the company's wafer fabrication, test, and assembly capabilities meet the latest manufacturing requirements. For special functional capabilities (i.e., increased speed, bandwidths, response times, etc.), SSi's 4-inch wafer fabrication facilities use sophisticated process techniques such as:

- Stepper and projection photolithography for high resolution.
- Positive resist and dry plasma etch for smaller feature size and minimal undercutting.
- And high-current ion implantation and automated sputtering, which are used to improve productivity.

SSi can also meet a wide spectrum of assembly and packaging needs. Quick-turn, low-volume assembly for prototypes is done in SSi's Tustin facility. High-volume production of plastic packages in any of DIP, PLCC, or SO configurations is done in Silicon Systems' Singapore Technology Center.



COMPUTER-AIDED MANUFACTURING WITH PROMIS ™ FOR RAPID DELIVERY OF RELIABLE ICs

Committed to Computer-Aided Manufacturing (CAM), Silicon Systems has invested in extensive computer resources. To handle the vast amounts of data required for manufacturing, monitoring, and statistical process control, SSi uses the Process and Management Information System (PROMIS™). The PROMIS system:

- manages inventory information,
- tracks wafers in process,
- monitors the clean room environment, and
- performs statistical process control.

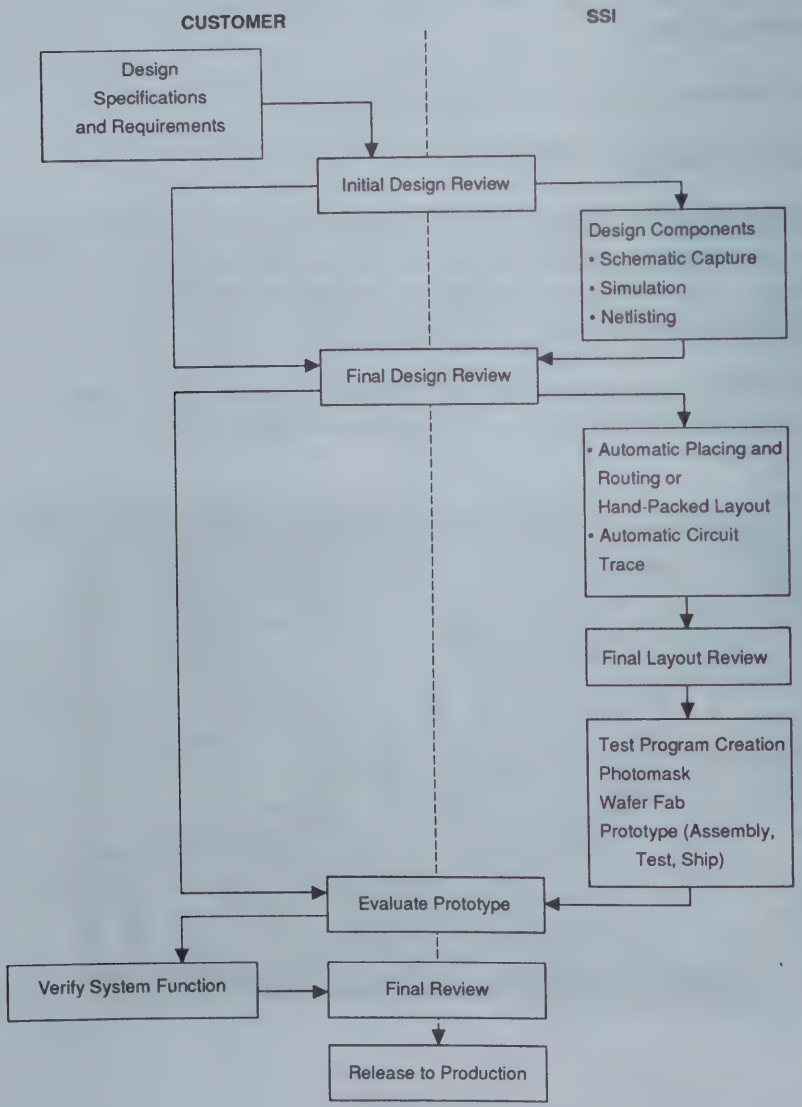
PROMIS provides computer-controlled (i.e., paperless) facilities, which reduces sources of contamination in the wafer fab clean rooms. SSi's wafer fab is a class "50" environment with class "10" work surfaces. Cleanliness is maintained through the service chase approach, which channels a minimum of 5 air exchanges per minute.

PROMIS allows Silicon Systems to deliver reliable ICs rapidly, thus allowing customers to introduce products to the marketplace on schedule and within budget.

SSi WORKS WITH CUSTOMERS TO CREATE THE BEST IC SOLUTION

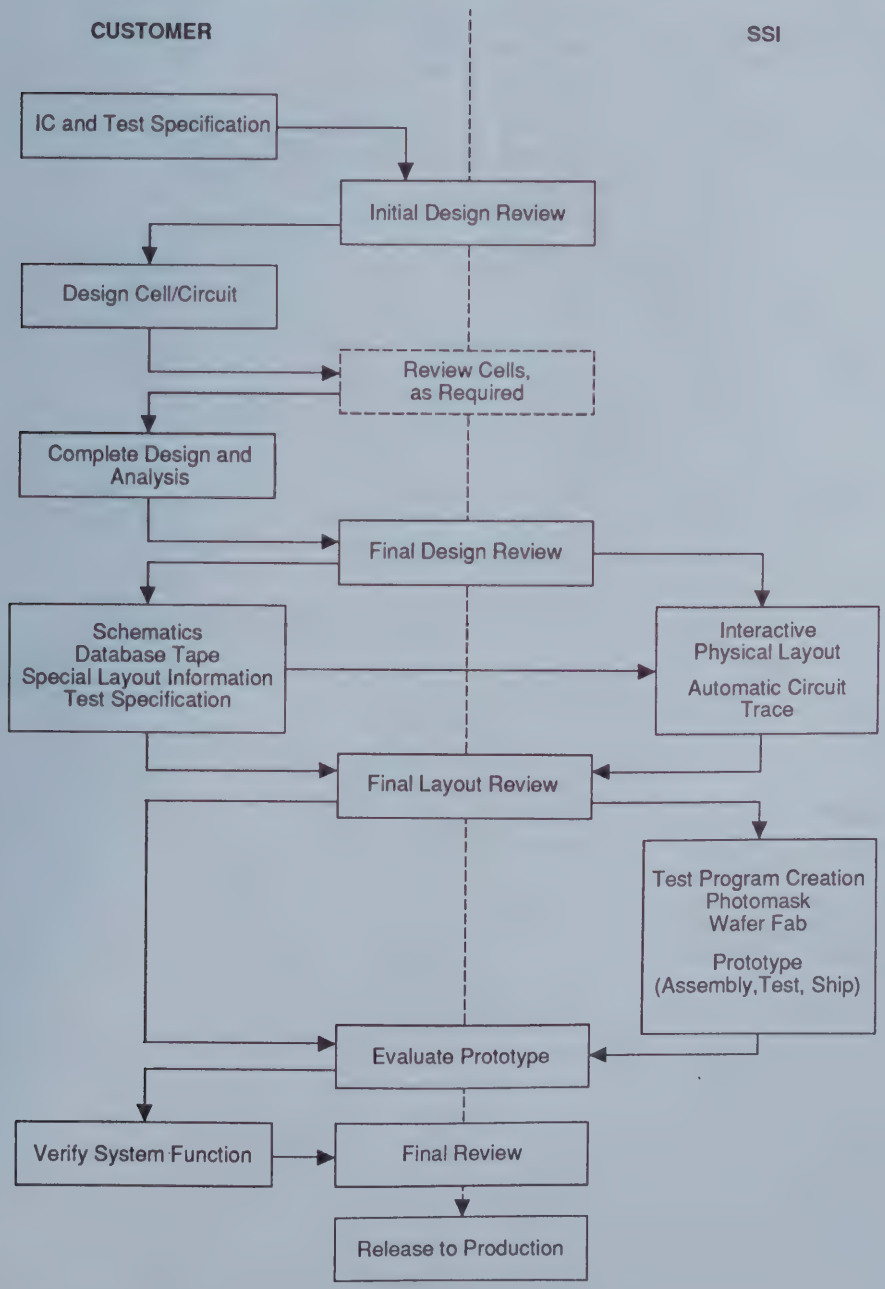
SSi has three IC design centers located in Tustin, California; Grass Valley, California; and Singapore. An additional center in Silicon Valley will open by late 1988. Any of these design centers can accept a functional specification and complete the entire design task using either a full-custom or a cell-based approach.

CUSTOMER INTERFACE FOR FULL-CUSTOM AND CELL-BASED DESIGNS



Or, a customer can complete most of the design, using array technology, and utilize SSi's expertise for physical layout.

CUSTOMER INTERFACE FOR ARRAY-BASED DESIGNS



NOTES:

Section 7

QUALITY ASSURANCE AND RELIABILITY

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CARMELO J. SANTORO
Chairman, President & CEO

SECTION 1

A MESSAGE FROM SILICON SYSTEMS' PRESIDENT AND CEO

Quality is the secret to long term success. It literally overshadows the short term emphasis on price, delivery, or any other measure of performance.

At Silicon Systems, we have based our quality philosophy on the development of a "state of mind" in each employee, related to job performance and to its reflection in the overall level of quality and reliability of our product.

You won't hear very many cliches about quality in our environment. But we do strive for "zero defects" for "just in time service" and for "doing it right the first time." We think constant reminders of tired phrases can serve more as an irritant than a stimulant. Our quality ethic is based on setting examples for others and by intuitive "high quality" job performance propogating the quality ethic throughout the organization to each employee.

To be sure, we have programs related to quality and reliability. They are the subject of this section. We are dedicated to process control, overall product reliability and outstanding outgoing quality. Rapid analysis of failures and returns providing responsive service to our customers also generates quick solutions to our own problems. We believe that the high levels which we achieve in quality, reliability and service are directly attributable to belief in the basic tenets of quality within our corporate culture.

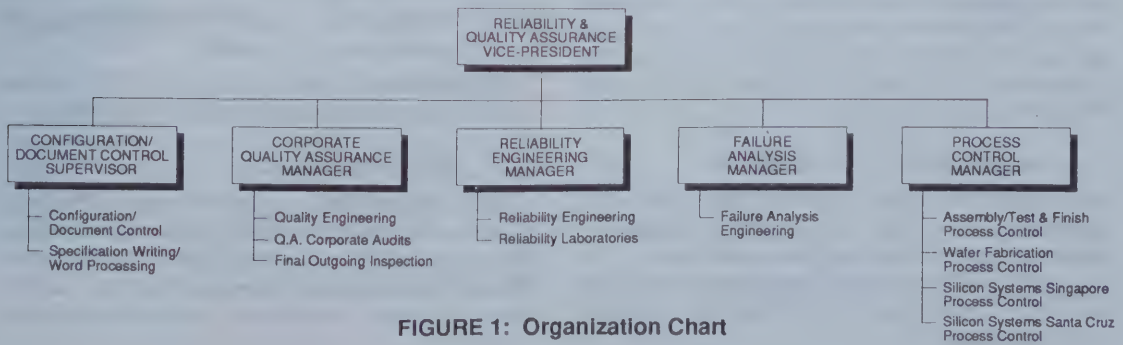


FIGURE 1: Organization Chart

Quality Assurance and Reliability

1.1 INTRODUCTION

Silicon Systems' management philosophy is the manufacture of a quality product consistent with company policy and customer requirements. It is the goal of the Quality Assurance and Reliability departments to ensure that these requirements are met. Included in this section is Silicon Systems' ongoing program for controlling and improving the quality of devices manufactured.

The data clearly illustrates that Silicon Systems is working diligently to maintain its position as a leader in the industry. The use of highly specialized equipment, test programs and test procedures allows us to determine product reliability under extreme conditions.

Quality is built into Silicon Systems' parts from rigid incoming inspection of piece parts and materials to stringent outgoing quality verification. The assembly process flow is encompassed by an elaborate system of test and inspection gates and in-line monitors. These gates and monitors ensure a step-by-step adherence to prescribed procedure.

In addition Silicon Systems is also incorporating statistical process control into our manufacturing operations. This approach of studying and improving the quality of processes and reduction of variation in products and services by the use of statistical problem solving techniques, analytical controls and quantitative methods ensures that Silicon Systems' products maintain a high level of quality and reliability. Our quality organization is committed to working closely with you to provide continuously improved incoming quality levels.

1.2 QUALITY ASSURANCE AND RELIABILITY

The quality of a semiconductor device is defined by its conformance to specification; the reliability of a semiconductor device is defined by how well it continues to conform to specification over time while under stress. This relationship between quality and reliability requires a program that encompasses both. Included in this section are outlines of our process control program and our PPM (part-per-million) program. These programs assure conformance to specification throughout the manufacturing process.

1.2.1 ORGANIZATION PHILOSOPHY

To facilitate the close cooperation and coordinating required of the Quality and Reliability functions, a combined organization has been established. This organization must have access to and support from the top of the organization. The R&QA organization is shown in Figure 1.

SECTION 2: QUALITY ASSURANCE

2.1 QUALITY PROGRAM

Quality Assurance has the ultimate responsibility for the reliable performance of our products. This is accomplished through the administration of formal systems which assure that our products meet the requirements of customer purchase orders and specifications for design, from raw material through finished product.

Quality Assurance supports formal qualifications of suppliers, material, processes, and products; administration of system and production monitors to assure that our products do meet the desired specifications; and the liaison between Silicon Systems and the customer for all product-related problems.

It is the practice of Silicon Systems to have the Quality and Reliability Program encompass all of its activities, starting with a strong commitment of support for the program from the corporate level. and continuing with customer support after the product has been shipped.

Silicon Systems firmly believes that quality must be "built into" all of its products by ensuring that employees are trained in the quality philosophy of the company. Some of the features built into Silicon Systems Quality Program include:

1. Structured training programs directed at Wafer Fabrication, Test, and Process Control personnel.
2. Stringent in-process inspection, gates and monitors.
3. Total evaluation of designs, materials, and processing procedures.
4. Stringent electrical testing (100% and QA AQL testing).
5. Ongoing reliability monitors and process verifications.
6. Real time use of statistical process control methodology.
7. Corporate level audits of manufacturing, subcontractors, and suppliers.

These structured quality methods result in products which deliver superior performance in the field.

2.2 PROCESS CONTROL

Silicon Systems' process control program is designed to provide continuous visibility of the performance of manufacturing processes and ensure that corrective action is taken before problems develop. The principal areas of process control which assess the quality of

processed product against quality standards are incoming materials inspection and process control monitoring.

2.2.1 INCOMING INSPECTIONS

Incoming inspection plays a very important role in Silicon Systems' quality program. Small deviations from material specifications can transverse the entire production cycle before being detected by outgoing quality control. By paying strict attention to quality at this early stage, the possibility of failures occurring further down the line is greatly minimized.

2.2.2 IN-PROCESS INSPECTIONS

Every major manufacturing setup is followed by an appropriate in-process quality control inspection gate. Silicon Systems has established inspection gates in areas such as Wafer Fabrication, Wafer Probe, Assembly, And Final Test areas.

In addition to these established gates, Silicon Systems also has established monitors during various stages in the manufacturing process. It is this built-in quality that ensures failure-free shipment of Silicon Systems' products.

Quality control monitors have been placed though-out the manufacturing flow, so that data may be collected and analyzed to verify the results of intermediate manufacturing steps. This data is used to determine quality trends or long term changes in the quality of specific operations. A general description of the product flow and QC inspection points are shown in Figure 2.

2.3 PPM PROGRAM

The main purpose of employing a PPM program is to eliminate defects. The action portion of this program is accomplished in three stages:

1. Identify all defects by failure mode.
2. Identify defect causes and initiate corrective action.
3. Measure results and set improved goals.

The data generated from an established PPM program is statistically compiled as a ratio of units rejected/tested. This ratio is then expressed in terms of parts per million (PPM) with a confidence limit attached. The eventual reported PPM result therefore allows proper significance to be attached to every defect found. The final aim or goal is to achieve and maintain zero defects.

Based on significantly large volumes of PPM data and an established five-year strategic plan identifying industry-wide competitive PPM goals, Silicon Systems has progressively achieved excellent quality standards and will continue to measure the result and therefore improve on PPM standards as set by the industry.

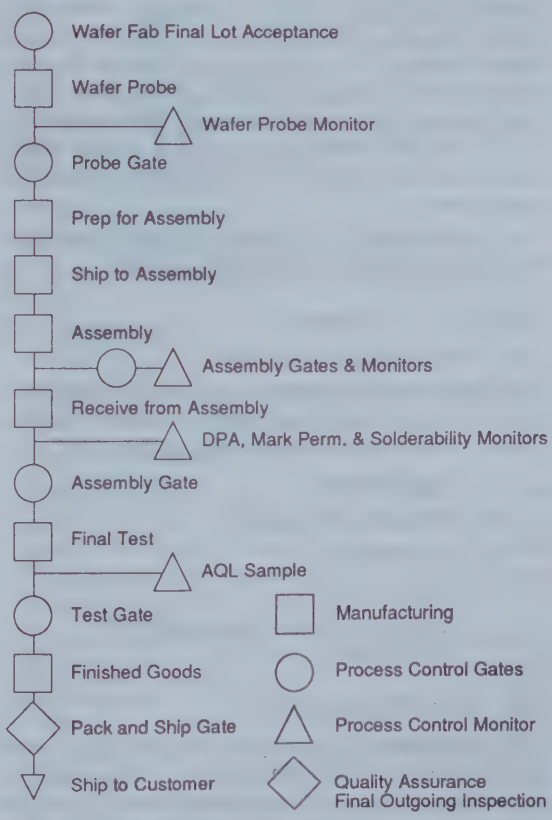


FIGURE 2
Process Control Gates and Monitors

7

2.4 COMPUTER AIDED MANUFACTURING CONTROL

Computer Aided Manufacturing (CAM) requires the identification, control, collection and dissemination of vast amounts of data for logistics control. Silicon Systems used this type of computerized system for statistical process control and manufacturing monitoring. PROMIS (Process Management and Information Systems) displays document control-released recipes, processes, and procedures, tracks work-in-process, contains accurate inventory information, allows continuous recording of facilities, data, contains performance analysis capabilities, and much more. PROMIS allows for a paperless facility, which assists in keeping contamination out of the wafer fab clean room.

The configuration of PROMIS has been tailored to meet the requirements of Silicon Systems.

SECTION 3: RELIABILITY

3.1 RELIABILITY PROGRAM

Silicon Systems has defined various programs that will continuously characterize product reliability levels. These programs are categorically described as:

1. Qualifications
2. Production monitors
3. Evaluations
4. Failure analysis
5. Data collection and presentation for improvement projects

3.2 QUALIFICATIONS

The application of this program ensures that all new product designs, processes, and packaging meet the absolute maximum rated design and worst case end use criteria. The large database generated by means of the accelerated stress testing result in a maximum confidence for determining the final use in the production environment.

3.3 PRODUCTION MONITORS

This program has been established to randomly select from production a statistically significant sample and subject it to the maximum stress test levels to determine useful life of the product in a field use environment.

This section shows reliability methods that are in use at Silicon Systems. The importance of production monitors at Silicon Systems does, in effect assure continued reliability.

3.4 EVALUATIONS

The evaluation program at Silicon System is an ongoing program that will continue defining standards which cover the reliability assessment of the circuit portion, process parameters, and packaging of a new product. This program continuously provides performance characteristics of the products that are part of the improvement projects at Silicon Systems.

3.5 FAILURE ANALYSIS

The failure analysis program is an integral part of the Reliability Department at Silicon Systems. Being aware of the low defect density requirements in the industry along with the needed competitive edge, Silicon Systems has formed a highly technical and sophisticated failure analysis laboratory. This laboratory provides visual analysis, electrical reject mode analysis, and both destructive and non-destructive data to aid the engineers in their corrective action for improvement programs, and to help our customers implement improved field use design. This may include metallurgical, optical, chemical, electrical and SEM with X-ray dispersive analysis as needed.

Conclusively, this in-house testing and analysis allows Silicon Systems to monitor all aspects of manufacturing to ensure that a product of highest quality is shipped to our customers.

3.6 DATA COLLECTION & PRESENTATION FOR IMPROVEMENT PROJECTS

Data is collected from each of the above programs and summarized for ease of understanding among all engineering disciplines in the company. This data facilitates improvement and provides our customers an opportunity to review our product performance.

3.7 RELIABILITY METHODS

The Reliability Program utilizes various stress tests that are presently being used to define performance levels of our products. Many of these stress test are per MIL-STD. 883C as shown in Table 3.

TEST	CONDITIONS	PURPOSE OF EVALUATION
Biased temperature/humidity	85°C/85° %RH	Resistance to high humidity with bias
High temperature operating life (HTOL)	Mil 883C, Method 1005	Resistance to electrical and thermal stress
Highly accelerated stress test (HAST)	SSi Method	Evaluates package integrity
Steam pressure	121°C/15PSI	Resistance to high humidity
Temperature cycling	Mil 883C, Method 1010	Resistance to thermal excursion (air)
Thermal shock	Mil 883C, Method 1011	Resistance to thermal excursion (liquid)
Salt atmosphere	Mil 883C, Method 1009	Resistance to corrosive environment
Constant acceleration	Mil 883C, Method 2001	Resistance to constant acceleration
Mechanical shock	Mil 883C, Method 2002	Resistance to mechanical shocks
Solderability	Mil 883C, Method 2003	Evaluates solderability of leads
Lead integrity	Mil 883C, Method 2004	Evaluates lead integrity before board assembly
Vibration, variable frequency	Mil 883C, Method 2007	Resistance to vibration
Thermal resistance	SSi Method	Evaluates thermal dissipation
Electrostatic damage	Method 3015	Evaluates ESD susceptability
Latch-up	SSi Method	Evaluates latch-up susceptibility
Seal fine and gross leak	Mil Std 883C, Method 1014	Evaluates hermeticity of sealed packages

TABLE 3: Reliability Stress Tests

3.8 RELIABILITY PREDICTION METHODOLOGY

It has been known in reliability engineering principles that the failure rate of a group of devices as a function of time will follow a life curve as shown below:

The bathtub curve above, implies that the useful life of the product extends until some basic design limitation is experience. At SSi the Arrhenius model is used to extrapolate a failure rate at an accelerated temperature test condition to a normal use temperature condition.

The model basically states $R = Ae^{-Ea/KT}$

where R = Reaction rate

A = Constant

E_a = Activation energy (eV)

K = Boltzmann's constant 8.63×10^{-5} eV/°K

T = Absolute temperature (°K)

SECTION 4: ELECTROSTATIC DISCHARGE PROGRAM

4.1 ESD PREVENTION

Silicon Systems recognizes that procedures for the protection of Electrostatic Discharge (ESD) sensitive devices from damage by electrical transients and static electricity must be incorporated throughout all operations which come in contact with these devices.

Silicon Systems' quality program incorporates various protection measures for the control of ESD. Some of these preventive measures include handling of parts at static safe-guarded workstations; the wearing of wrist straps during all handling operation; the use of conductive lab coats in all test areas and areas which handle parts; and the packaging of components in conductive and anti-static containers.

NOTES:

Section 8

PACKAGING/ ORDERING INFORMATION

Silicon Systems
Packaging Index

DUAL-IN-LINE PACKAGE (DIP)	PINS	PAGE NO.
Plastic	8, 14, 16 & 18	8-5
	20, 22, 24 & 24S	8-6
	28, 32 & 40	8-7
Ceramic	8, 14, 16 & 18	8-8
	22, 24 & 28	8-9
SURFACE MOUNTED DEVICES (SMD)		
PLCC (Quad)	28, 32 & 44	8-10
	52 & 68	8-11
Quad (Fine Pitch)	52 & 100	8-12
Small Outline (SOIC)	8, 14 & 16 SON*	8-13
	16, 18, 20, 24 & 28 SOL**	8-14
	34 & 36 SOL**	8-15
	32 SOW***	8-15
Flatpack	10, 24, 28 & 32	8-16

*SON is a 150 mil width package.
**SOL is a 300 mil width package.
***SOW is a 400 mil width package.

Silicon Systems
Packaging Matrix

Package Type	8	10	14	16	18	20	22	24	28	32	34	36	40	44	52	68	100
Plastic DIP																	
300 mil	X		X	X	X	X		S									
400 mil							X										
600 mil								X	X	X			X				
Cerdip																	
300 mil	X		X	X	X	X											
400 mil							X										
600 mil								X	X				X				
Side Braze																	
300 mil	X		X	X	X	X		S									
400 mil							X										
600 mil								X	X				X				
Small Outline																	
150 mil	X		X	X													
300 mil				X		X		X	X		X	X					
400 mil										X							
Flatpack		X	X					X	X	X							
Chip Carrier				X		X			X								
Plastic Quad									X	X				X	X	X	
Ceramic Quad									X					X		X	
QFP															X		X

8

Silicon Systems
Communications Products
Package Types

DEVICE TYPE	PACKAGE TYPE			
	P S* Plastic	D Cerdip	H PLCC	N L W Small Outline
SSI 73D2404	28, 28, 40		28, 44, 44	
SSI 73K212	22 & 28		28	
SSI 73K212L	22 & 28		28	
SSI 73K221	22 & 28		28	
SSI 73K221L	22 & 28		28	
SSI 73K222	22 & 28		28	
SSI 73K222L	22 & 28		28	
SSI 73K222U	40		44	
SSI 73K224	28		32, 44	
SSI 73K224L	28		32, 44	
SSI 73K322	22 & 28		28	
SSI 73K322L	22 & 28		28	
SSI 73M214	28		28	
SSI 73M223	16			
SSI 73M3522	16			
SSI 73M450	40		44	
SSI 73M450F	40		44	
SSI 73M450L	40		40	
SSI 73M450LF	40		40	
SSI 75T201	22			

*Narrow

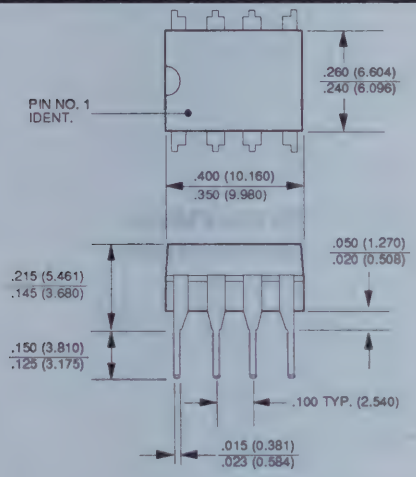
(Continued)

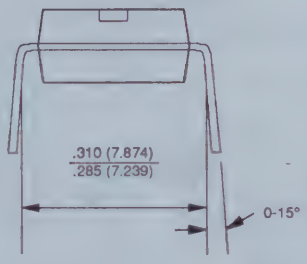
DEVICE TYPE	PACKAGE TYPE			
	P S* Plastic	D Cerdip	H PLCC	N L W Small Outline
SSI 75T202	18			
SSI 75T203	18			
SSI 75T204	14			16L
SSI 75T2089	22			
SSI 75T2090	22			
SSI 75T2091	28		28	
SSI 75T957	22			24L
SSI 75T980	8			16L
SSI 75T981	22			
SSI 75T982	22			
SSI 78A093A	40		44	
SSI 78A093B	40		44	
SSI 78A207	20			
SSI 78A400	16			18L
SSI 78A420	22			
SSI 78P233	24 & 24S			24L
SSI 78P234	20			20L

*Narrow

Silicon Systems
Standard Product Marketing
Number Definition

Package Information
(Plastic DIP)





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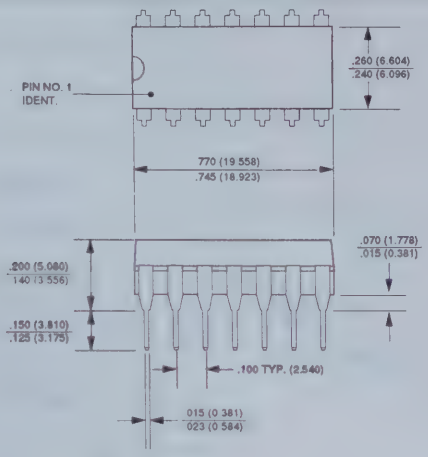

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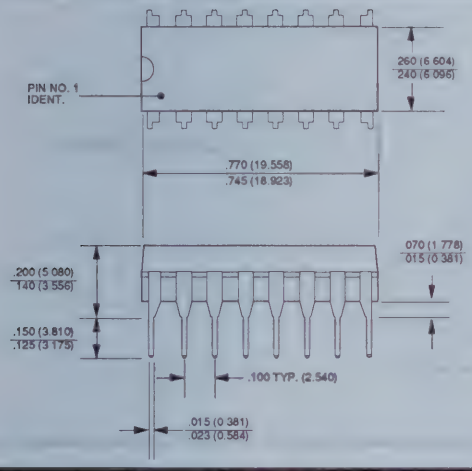

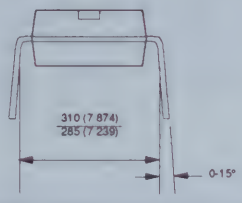

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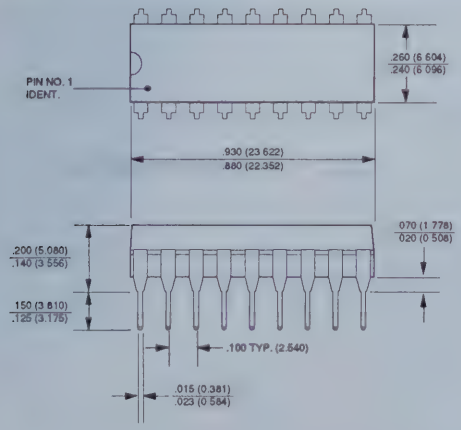

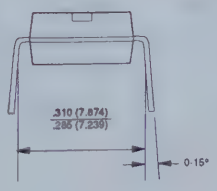

18-Pin Plastic

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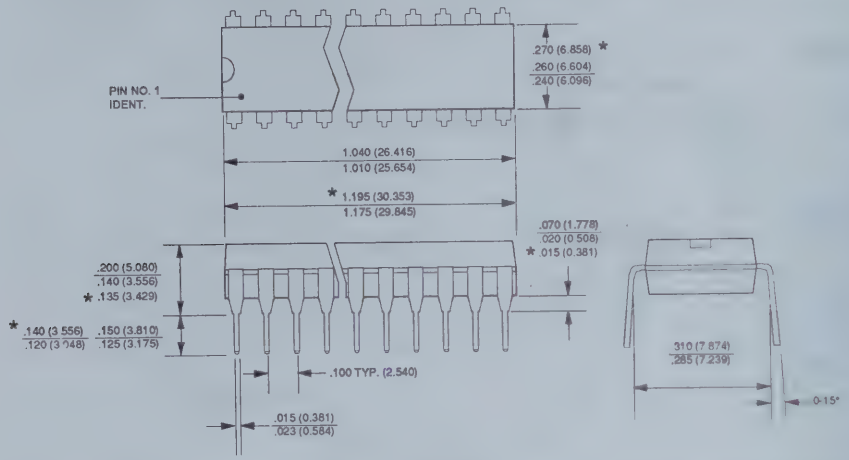
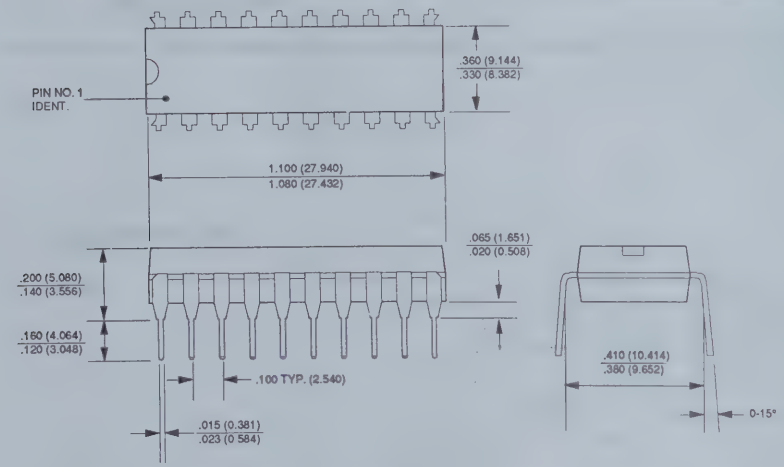


20 Pin Plastic
***24S Pin Plastic**



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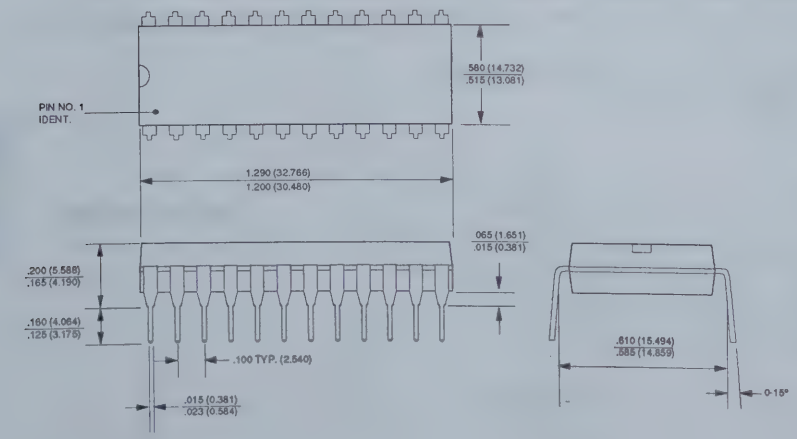

24-Pin Plastic

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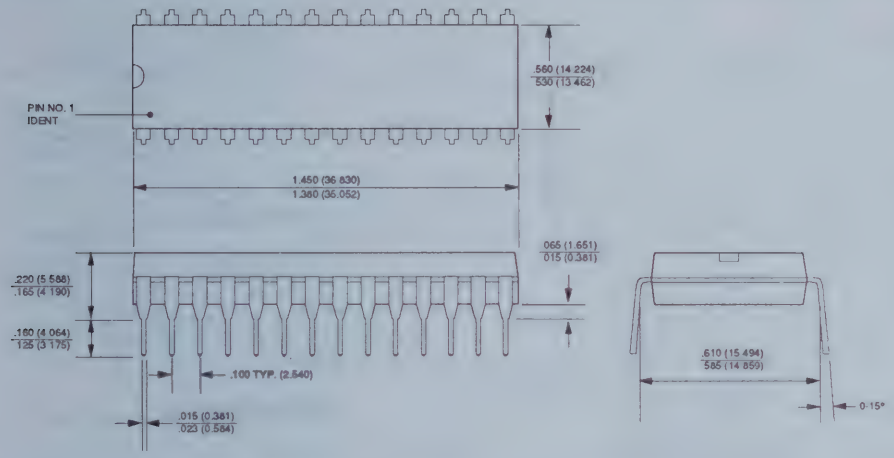

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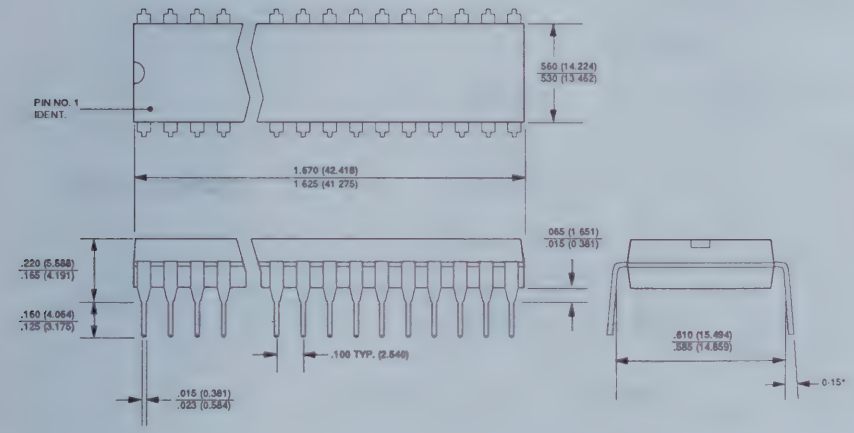

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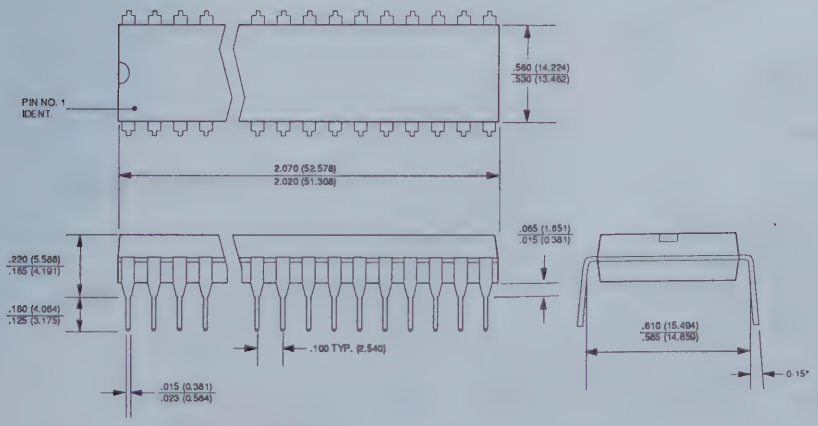

40-Pin Plastic

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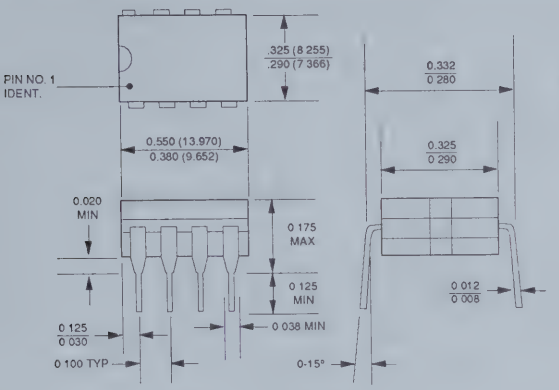
Package Information (Cerdip)



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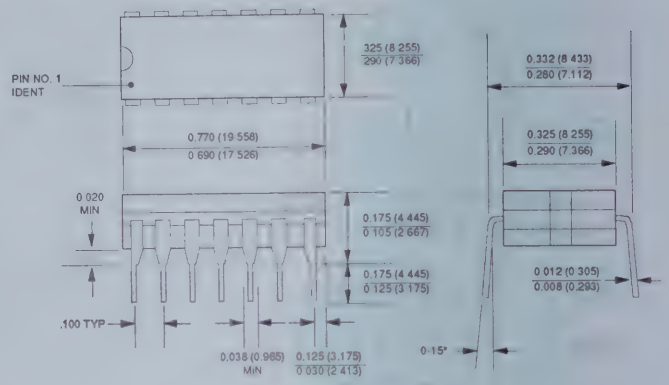

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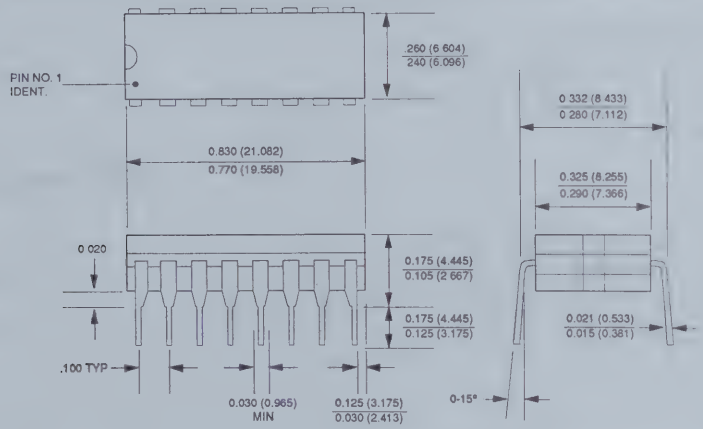

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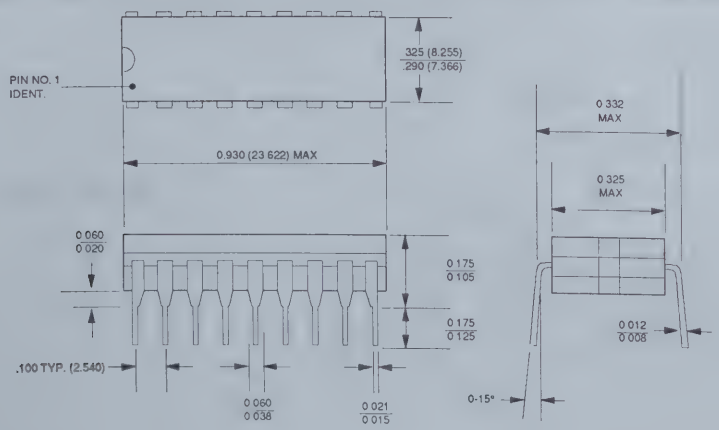

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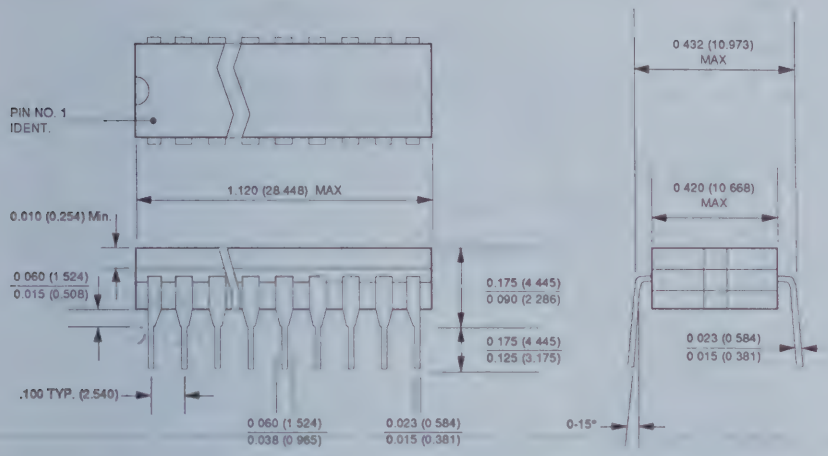

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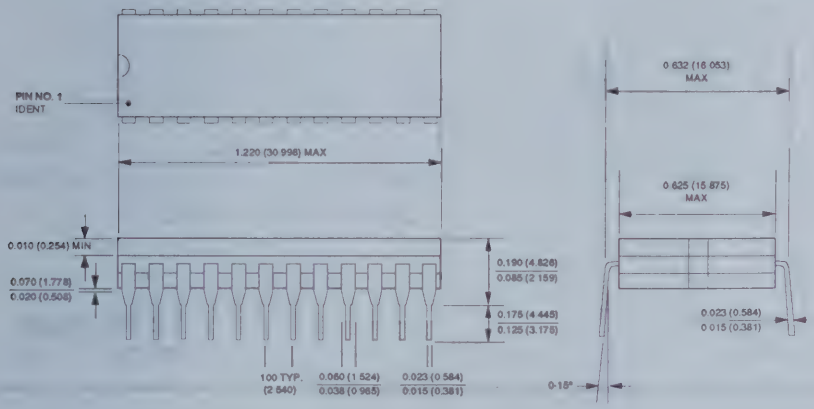

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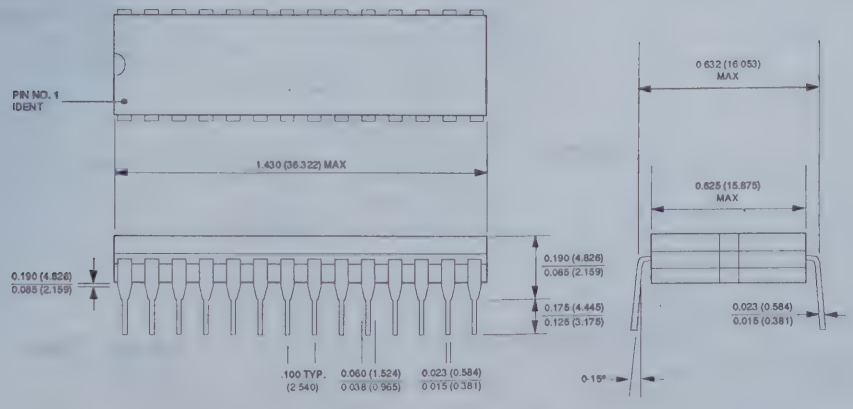
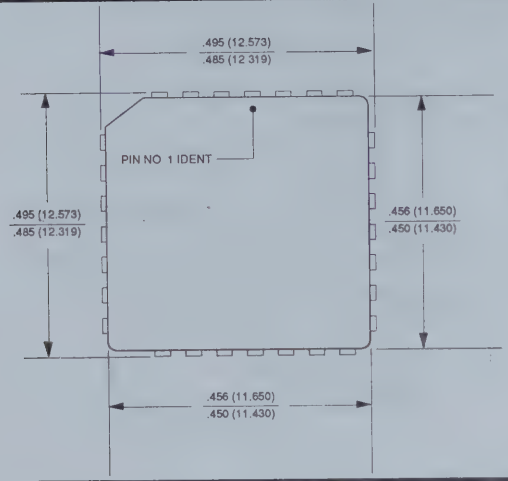
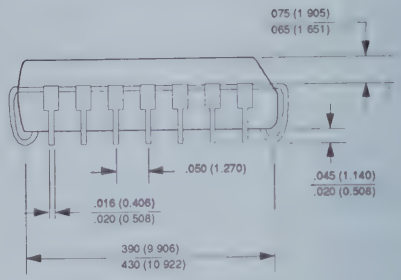


28-Pin Cerdip

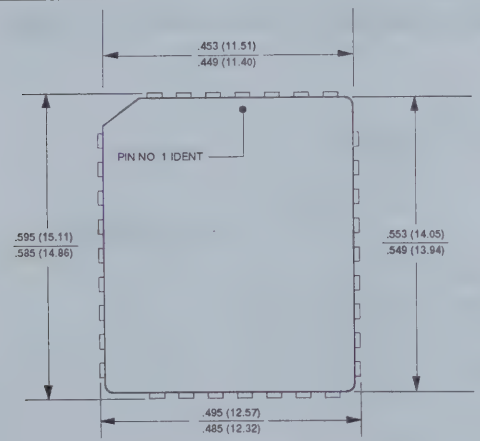
8

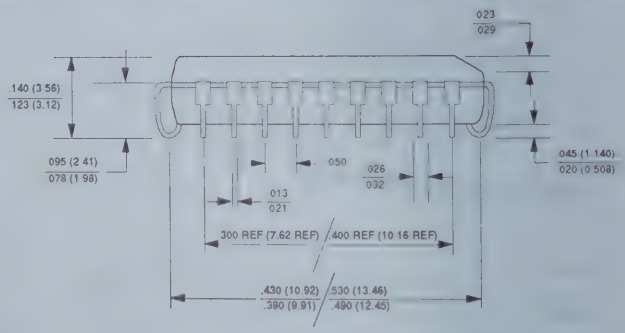
Package Information
PLCC (Quad)



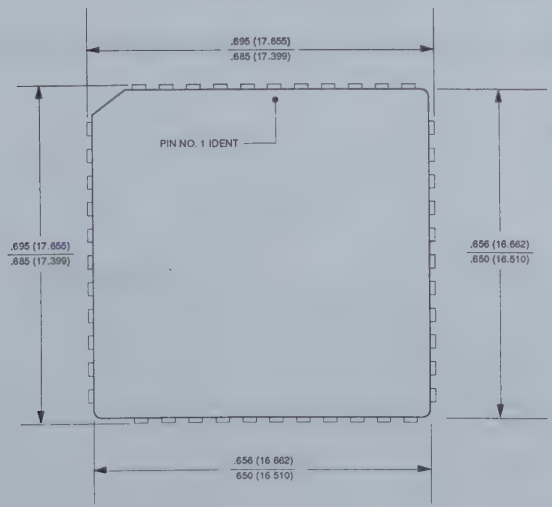


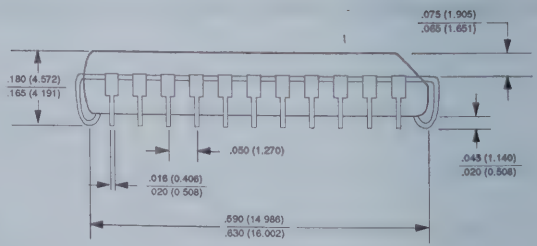
28-Pin Quad PLCC





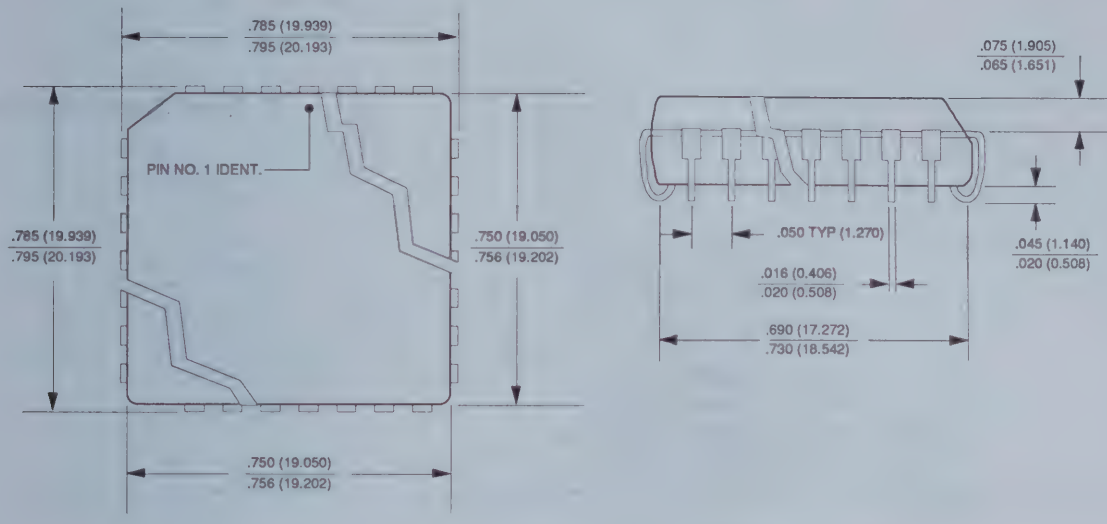
32-Pin Quad PLCC



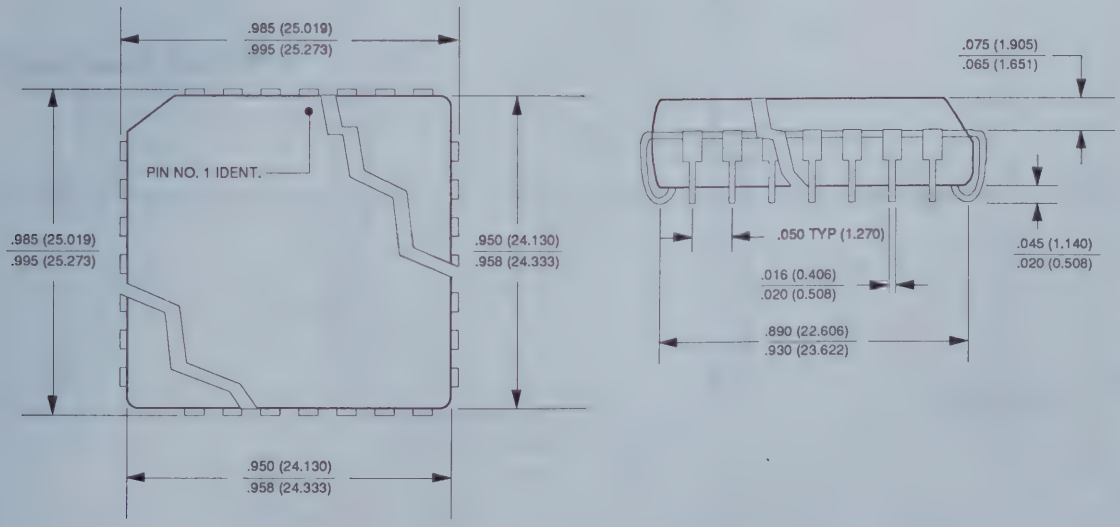


44-Pin Quad PLCC

Package Information
PLCC (Quad)



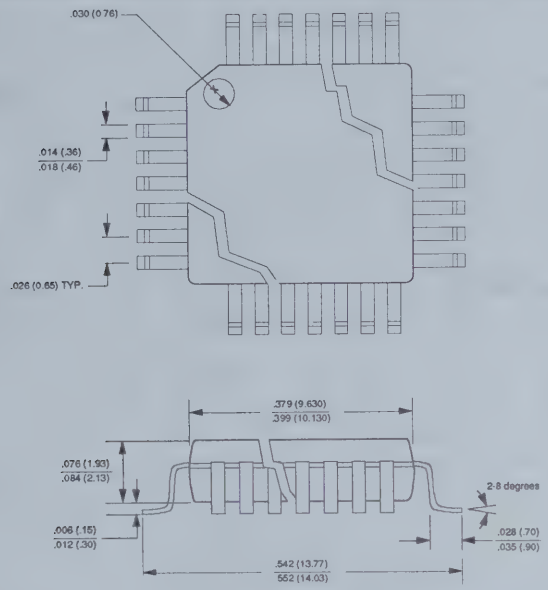
52-Pin Quad PLCC



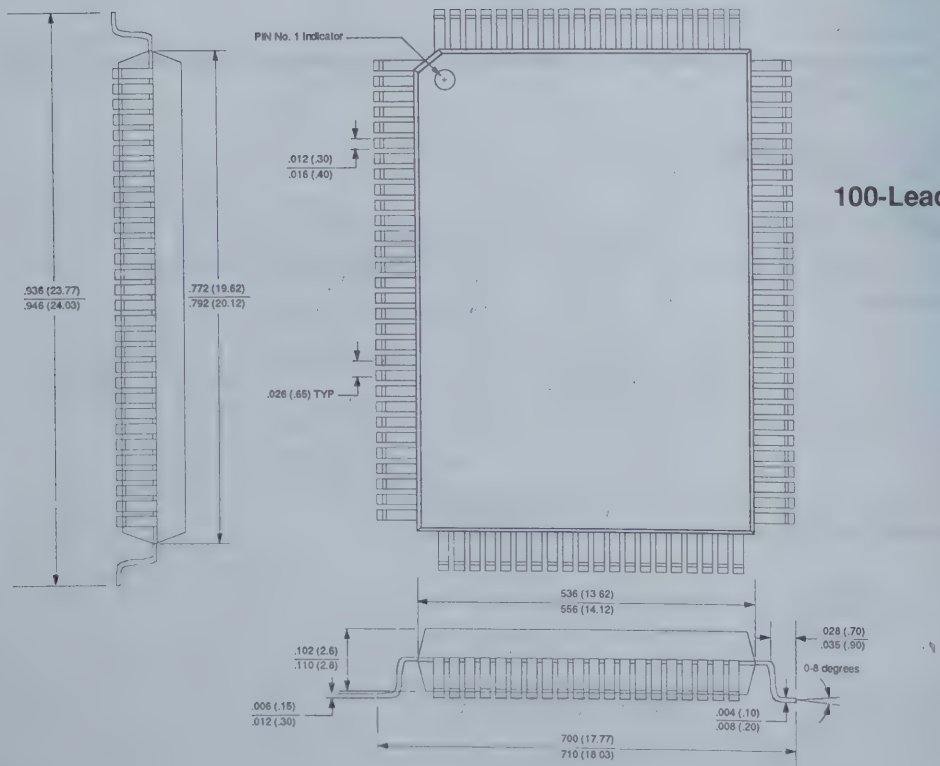
68-Pin Quad PLCC

8

Package Information
Quad (Fine Pitch)



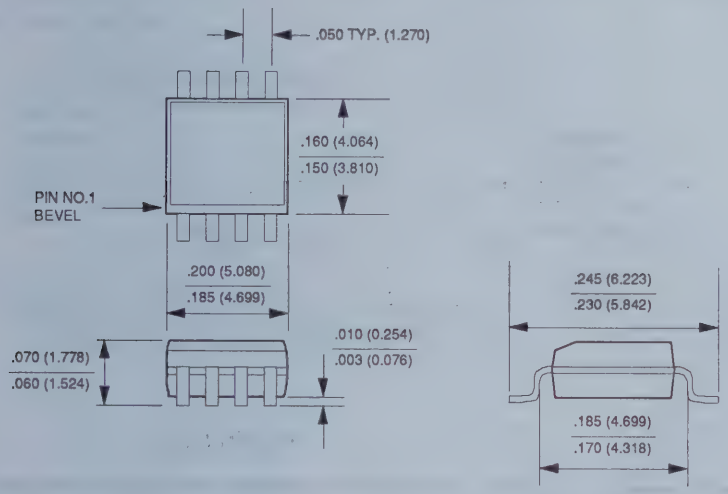
52-Lead Quad Fine Pitch



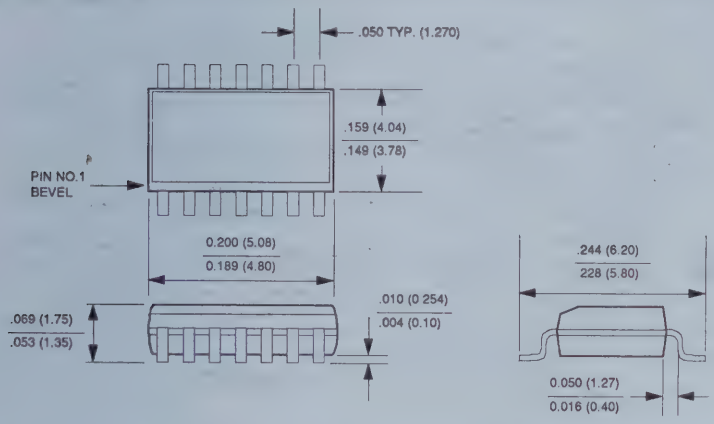
100-Lead Quad Fine Pitch

Package Information
(SON)

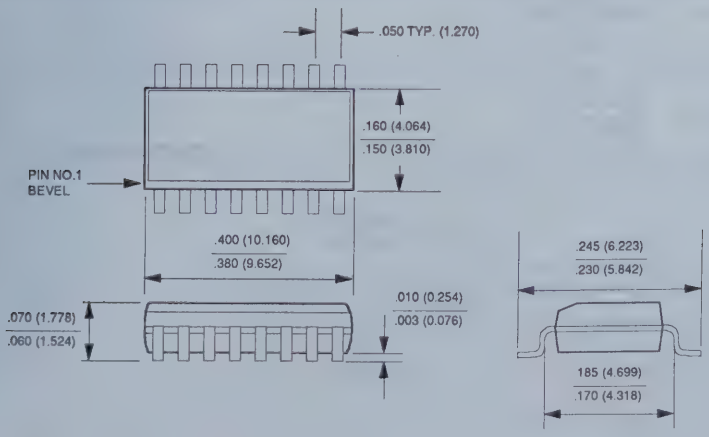
8-Pin SON



14-Pin SON



16-Pin SON



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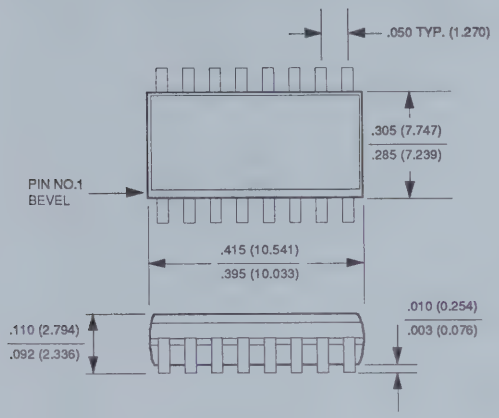
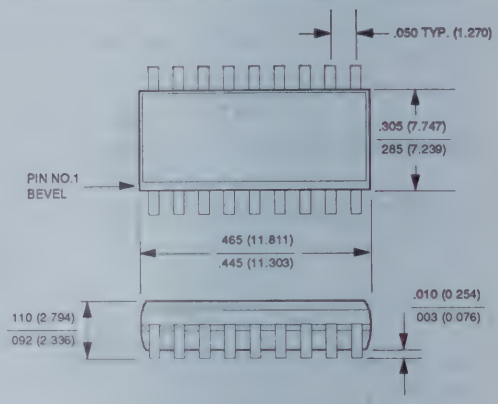
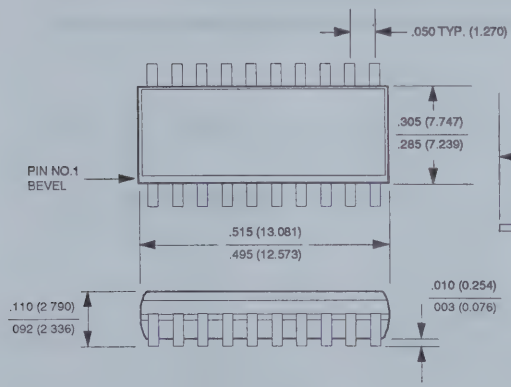
Package Information
(SOL)



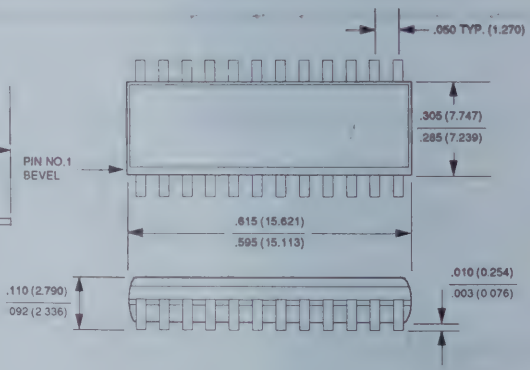
16-Pin SOL



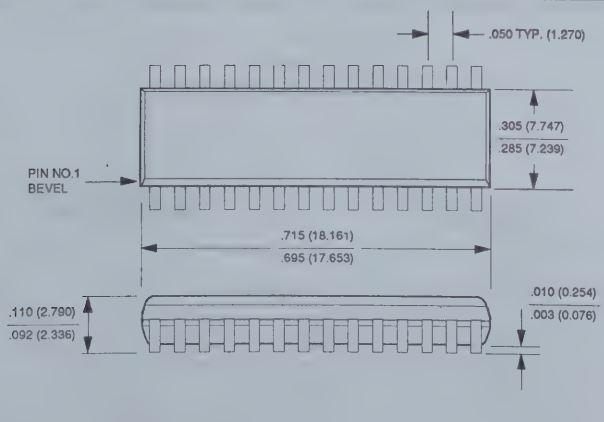
18-Pin SOL



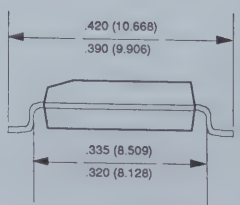
20-Pin SOL



24-Pin SOL

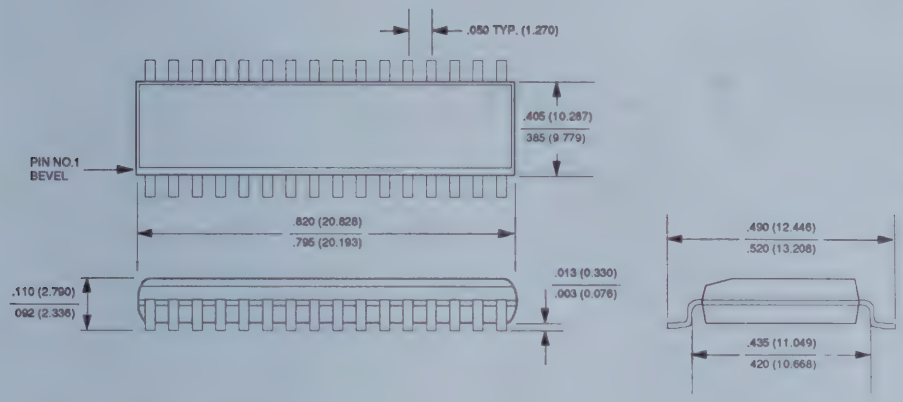


28-Pin SOL

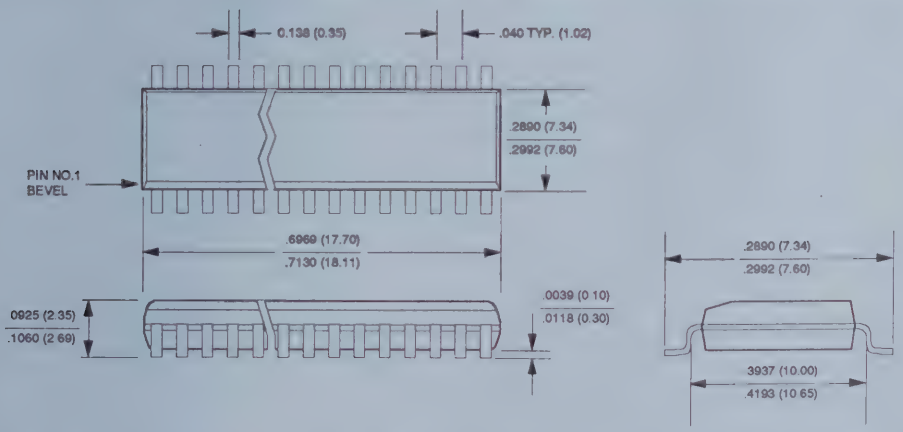


Package Information (SOL/SOW)

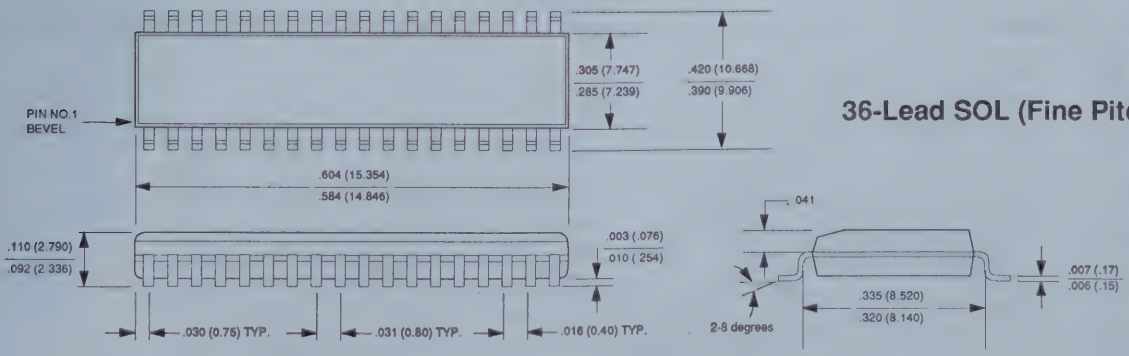
32-Pin SOW



34-Pin SOL

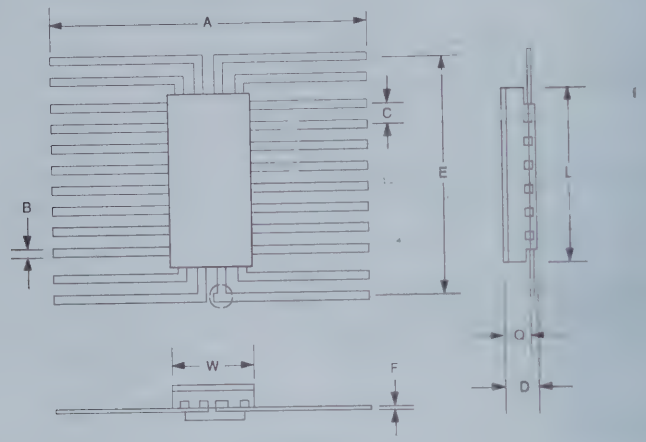


36-Lead SOL (Fine Pitch)

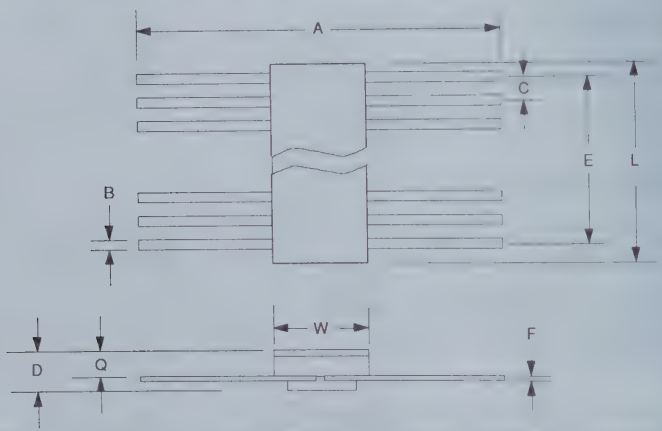


8

Package Information (Flatpack)



Flatpack
24-Leads



Flatpack
10, 28, 32-Leads

Pkg. Type	Lead Cnt.	A	B	C	D	E	F	L	Q	W
F	10	.900	.015 / .019	.045 / .055	.090 max	.200 typ	.004 / .007	.250 / .260	.074 typ	.250 / .260
F	24	.900	.015 / .019	.050 typ	.087 max	.567 typ	.004 / .007	.391 / .405	.075 typ	.264 / .276
F	28	1.150	.015 / .019	.045 / .055	.092 max	.645 / .655	.004 / .007	.712 / .728	.085 / .078	.492 / .508
F	32	1.150	.015 / .019	.045 / .055	.092 max	.745 / .755	.004 / .007	.812 / .828	.085 / .078	.492 / .508

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